MEMORY
DATABOOK

NATIONAL
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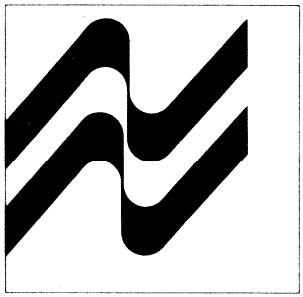

MEMORY
DATABOOK

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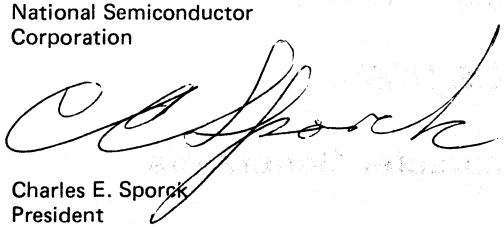
President's Message

Dear Customer:

The exciting future of memory applications is limited only by our collective abilities to make use of the continuing stream of rapid technological advances. Annual consumption of semiconductor memory components has already surpassed a half billion dollars per year and will cross the one billion dollar level within the next three years. Years ago National established the reputation as a high volume supplier of high quality, cost-effective components for the complete range of discretes, linears, optoelectronics, transducers, A/D and D/A, hybrids and large scale integrated memory, microprocessor, and logic arrays. We are pleased to continue our expansion of this broad product line to include the memories you will require in the future. Our world-wide network of factory representatives, local stocking distributors, and field applications engineers is at your service to help meet your needs — just give any of them a call.

We appreciate your interest in National's products and services, and look forward to supplying your present and future requirements.

National Semiconductor
Corporation



Charles E. Sporck
President

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RAM Cross Reference Guide

BIPOLAR RAMs

OTHER SOURCE	NATIONAL
AMD	
AM27S00C	DM74S200
AM27S00M	DM54S200
AM27S01C	DM74S206
AM27S01M	DM54S206
AM27LS02C	DM74LS289
AM27LS02M	DM54LS289
AM72LS03C	DM74LS189
AM27LS03M	DM54LS189
AM27S02C	DM74S289
AM27S02M	DM54S289
AM27S03C	DM74S189
AM27S03M	DM54S189
AM3101	DM8589
AM3101A	DM74S289
AM31L01C	DM74LS289
AM31L01M	DM54LS289
Fairchild	
93403C	DM74S289
93411C	DM74S206
93411M	DM54S206
93421C	DM74S200
93421M	DM54S200
Intel	
3101	DM8589
3101A	DM74S289
M3101	DM7589
M3101A	DM54S289
3106	DM74S200
3106A	DM74S200
3107	DM74S206
3107A	DM74S206
Intersil	
IM5501C	DM7589
IM5501M	DM8589
IM5523C	DM74S200
IM5523M	DM54S200
IM5533C	DM74S206
IM5533M	DM54S206

OTHER SOURCE	NATIONAL
MMI	
5530	DM54S206
5531	DM54S200
5560	DM54S289
5561	DM54S189
6530	DM74S206
6531	DM74S200
6560	DM74S289
6561	DM74S189
L5560	DM54LS289
L5561	DM54LS189
L6560	DM74LS289
L6561	DM74LS189
Signetics	
N8225	DM8589
N82S06	DM74S200
N82S07	DM74S206
N82S16	DM74S200
N82S17	DM74S206
N82S21	DM86S21
N82S25	DM74S289
N82S116	DM74S200
N82S117	DM74S206
S82S06	DM54S200
S82S07	DM54S206
S82S16	DM54S200
S82S17	DM54S206
S82S25	DM54S289
Texas Instruments	
SN5489	DM7589
SN7489	DM8589
SN54S189	DM54S189
SN54S201	DM54S200
SN54S289	DM54S289
SN54S301	DM54S206
SN74S189	DM74S189
SN74S201	DM74S200
SN74S289	DM74S289
SN74S301	DM74S206

MOS RAMs

OTHER SOURCE	NATIONAL
AMD	
AM1101A	MM1101A
AM1101A1	MM1101A1
AM1101A1M	MM4250
AM9060C	MM5280-5
AM9060D	MM5280
AM9060E	MM5280
AM9101B	MM2101A*
AM9101C	MM2101A-2*
AM9101D	MM2101A-2*
AM9102	MM2102A-6
AM91L02	MM2102A-6L
AM9102A	MM2102A-4
AM91L02A	MM2102A-4L
AM9102B	MM2102A
AM91L02B	MM2102A-L
AM9102C	MM2102A-2
AM91L02C	MM2102A-2L
AM9102D	MM2102A-2
AM9102E	MM2102A-1
AM9111B	MM2111A*
AM9111C	MM2111A-2*
AM9111D	MM2111A-2*
AM9112B	MM2112A*
AM9112C	MM2112A-2*
AM9112D	MM2112A-2*
AMS	
AMS7270	MM5270
AMS7270-5	MM5270-5
AMS7271	MM5271
AMS7280	MM5280
AMS7280-5	MM5280-5
Fairchild	
21L02	MM2102A-6L
2102-1	MM2102A-4
21L02A	MM2102A-4L
21L02B	MM2102A-L
2102F	MM2102A
2102F2	MM2102A-2

OTHER SOURCE	NATIONAL
Intel	
1101A	MM1101A
1101A1	MM1101A-1
2101A	MM2101A*
2101A-2	MM2101A-2*
2101A-4	MM2101A-4*
2101	MM5269
2102A	MM2102A
2102A-2	MM2102A-2
2102A-4	MM2102A-4
2102AL	MM2102AL
2102AL-2	MM2102AL-2
2102AL-4	MM2102AL-4
2107B	MM5280
2107B-4	MM5280-5
2111A	MM2111A*
2111A-2	MM2111A-2*
2111A-4	MM2111A-4*
2112A	MM2112A*
2112A-2	MM2112A-2*
2112A-4	MM2112A-4*
2114	MM2114
Mostek	
MK4116-3	MM5290-3
MK4116-4	MM5290-4
MMI	
2170	MM5270
2171	MM5271
2180	MM5280
Signetics	
21F02	MM2102A
21F02-2	MM2102A-2
21F02-4	MM2102A-4
21L02-1	MM2102A-L
21L02-3	MM2102A-2L
2501	MM1101A1
2680	MM5280
2680-1	MM5280-5
2613	MM5257
2614	MM2114

OTHER SOURCE	NATIONAL
Texas Instruments	
TMS4033	MM2102A-4
TMS4039	
TMS4039-2	MM2101A-4
TMS4042-2	MM2101A-4
TMS4043-2	MM2112A-4
TMS4060	MM5280-5
TMS4060-1	MM5280
TMS4060-2	MM5280

CMOS RAMs

Intersil	
IM6551	MM74C920
IM6508	MM74C929
IM6518	MM74C930

*Available 4th quarter 1978

All parts are pin compatible. Check National data sheets for specification details.

SIZE AND ORGANIZATION	OUTPUT	NATIONAL MIL/COM	AMD M = MIL C = COM	F.S.C. M = MIL C = COM	INTEL M = MIL P = COM	INTERSIL M = MIL P = COM	MMI MIL/COM	SIGNETICS S = MIL N = COM	T.I. MIL/COM
64-Bit (16 x 4)	OC	DM7589/DM8589	AM3101		3101	IM5501		8225	SN5489/7489
	TS	DM7599/DM8599							
High Speed 64-Bit (16 x 4)	OC	DM54S289/DM74S289	AM27S02	93403	3101A		5560/6560	82S25	SN54S289/74S289
	TS	DM54S189/DM74S189	AM27S03				5561/6561		SN54S189/74S189
Low Power 64-Bit (16 x 4)	OC	DM54LS289/DM74LS289	AM27LS02				L5560/L6560		
	TS	DM54LS189/DM74LS189	AM27LS03				L5561/L6561		
File Reg. (16 x 4)	TS	DM75S68/DM85S68							
256-Bit (256 x 1)	OC	DM54S206/DM74S206	AM27S01	93411 93411A	3107 3107A	IM5533A	5530/6530	82S07 82S17 82S117	SN54S301/74S301
	TS	DM54S200/DM74S200	AM27S00	93421 93421A	3106 3106A	IM5523A	5531/6531	82S06 82S16 82S116	SN54200/74200 SN54S200/74S200 SN54S201/74S201

SIZE AND ORGANIZATION	OUTPUT	NATIONAL MIL/COM	AMD M = MIL C = COM	FAIRCHILD M = MIL C = COM	HARRIS 2 = MIL 5 = COM	INTEL M = MIL P = COM	INTERSIL M = MIL C = COM	M.M.I. MIL/COM –1 = SCHOTTKY	SIGNETICS S = MIL N = COM	T.I. MIL/COM
256-Bit (32 x 8) 16-Pin	OC	DM54S188/DM74S188	AM27S08		HM1-7602 HM1-8256		IM5600	5330/6330	8223 82S23	SN54188A/74188A SN54S188/74S188
	TS	DM54S288/DM74S288	AM27S09		HM1-7603		IM5610	5331/6331	82S123	SN54S288/74S288
1024-Bit (256 x 4) 16-Pin	OC	DM54S387/DM74S387	AM27S10	93417 93416	HM1-7610 HM1-1024A	3601-1 3601	IM5603	5300/6300	82S126	SN54S387/74S387
	TS	DM54S287/DM74S287	AM27S11	93427 93426	HM1-7611 HM1-1024	3621	IM5623	5301/6301	82S129	SN54S287/74S287
2048-Bit (512 x 4) 16-Pin	OC	DM54S570/DM74S570		93436	HM1-7620	3602	IM5604	5305/6305	82S130	
	TS	DM54S571/DM74S571		93446	HM1-7621	3622	IM5624	5306/6306	82S131	
4096-Bit (512 x 8) 24-Pin	OC	DM54S475/DM74S475		93438	HM1-7640	3604	IM5605	5340/6340	82S140	SN54S475/74S475
	TS	DM54S474/DM74S474		93448	HM1-7641	3624	IM5625	5341/6341	82S141	SN54S474/74S474
4096-Bit (512 x 8) 20-Pin	OC	DM54S473/DM74S473						5348/6348		SN54S473/74S473
	TS	DM54S472/DM74S472						5349/6349		SN54S472/74S472
4096-Bit (1024 x 4) 18-Pin	OC	DM54S572/DM74S572*		93452	HM1-7642	3605		5352/6352	82S136	
	TS	DM54S573/DM74S573*		93453	HM1-7643	3625		5353/6353	82S137	

Note: All manufacturer's PROMs program differently.
*Future products

TOTAL BITS	PART NUMBER		ORGANIZATION	NUMBER OF PINS	TEMPERATURE RANGE	MAXIMUM ADDRESS ACCESS (t_{AA})	MAXIMUM SUPPLY CURRENT (I_{CC})
	PROM	ROM					
256	DM54S188		32 x 8 OC	16	−55°C to +125°C	45	110
	DM74S188		32 x 8 OC	16	0°C to +70°C	35	110
	DM54S288		32 x 8 TS	16	−55°C to +125°C	45	110
	DM74S288		32 x 8 TS	16	0°C to +70°C	35	110
1024	DM54S387	DM54S187	256 x 4 OC	16	−55°C to +125°C	60	130
	DM74S387	DM74S187	256 x 4 OC	16	0°C to +70°C	50	130
	DM54S287	DM75S97	256 x 4 TS	16	−55°C to +125°C	60	130
	DM74S287	DM85S97	256 x 4 TS	16	0°C to +70°C	50	130
2048	DM54S570	DM54S270	512 x 4 OC	16	−55°C to +125°C	65	130
	DM74S570	DM74S270	512 x 4 OC	16	0°C to +70°C	55	130
	DM54S571	DM54S370	512 x 4 TS	16	−55°C to +125°C	65	130
	DM74S571	DM74S370	512 x 4 TS	16	0°C to +70°C	55	130
4096	DM54S572		1k x 4 OC	18	−55°C to +125°C	75	140
	DM74S572		1k x 4 OC	18	0°C to +70°C	60	140
	DM54S573		1k x 4 TS	18	−55°C to +125°C	75	140
	DM74S573		1k x 4 TS	18	0°C to +70°C	60	140
4096	DM54S475	DM77S95	512 x 8 OC	24	−55°C to +125°C	75	170
	DM74S475	DM87S95	512 x 8 OC	24	0°C to +70°C	65	170
	DM54S474	DM77S96	512 x 8 TS	24	−55°C to +125°C	75	170
	DM74S474	DM87S96	512 x 8 TS	24	0°C to +70°C	65	170
8192		DM75S29	1k x 8 OC	24	−55°C to +125°C	90	160
		DM85S29	1k x 8 OC	24	0°C to +70°C	70	160
		DM75S28	1k x 8 TS	24	−55°C to +125°C	90	160
		DM85S28	1k x 8 TS	24	0°C to +70°C	70	160
4096	DM54S473		512 x 8 OC	20	−55°C to +125°C	75	155
	DM74S473		512 x 8 OC	20	0°C to +70°C	60	155
	DM54S472		512 x 8 TS	20	−55°C to +125°C	75	155
	DM74S472		512 x 8 TS	20	0°C to +70°C	60	155

Note. All PROMS are direct equivalents to their respective ROMS.

Size	Organization	Part Number	Type	Operation	Maximum Supply Current	Maximum Access Time	Supply Voltage (V)	Temperature Range (°C)	Package	In Production	Future
64	16 x 4	DM5489	TTL	Static	120 mA	80 ns	5	−55 to +125	16-Pin	•	
		DM7489	TTL	Static	120 mA	60 ns	5	0 to +70	16-Pin	•	
		DM54LS189	TTL	Static	29 mA	100 ns	5	−55 to +125	16-Pin	•	
		DM74LS189	TTL	Static	29 mA	80 ns	5	0 to +70	16-Pin	•	
		DM54S189	TTL	Static	110 mA	50 ns	5	−55 to +125	16-Pin	•	
		DM74S189	TTL	Static	110 mA	35 ns	5	0 to +70	16-Pin	•	
		DM54LS289	TTL	Static	29 mA	110 ns	5	−55 to +125	16-Pin	•	
		DM74LS289	TTL	Static	29 mA	90 ns	5	0 to +70	16-Pin	•	
		DM54S289	TTL	Static	105 mA	50 ns	5	−55 to +125	16-Pin	•	
		DM74S289	TTL	Static	105 mA	35 ns	5	0 to +70	16-Pin	•	
		DM85S68	TTL	Static	100 mA	40 ns	5	0 to +70	18-Pin	•	
		DM7599	TTL	Static	120 mA	70 ns	5	−55 to +125	16-Pin	•	
		DM8599	TTL	Static	120 mA	50 ns	5	0 to +70	16-Pin	•	
		MM54C89	CMOS	Static	300 μA	280 ns	3 to 15	−55 to +125	16-Pin	•	
		MM74C89	CMOS	Static	300 μA	280 ns	3 to 15	−40 to +85	16-Pin	•	
256	256 x 1	DM54S200	TTL	Static	130 mA	70 ns	5	−55 to +125	16-Pin	•	
		DM74S200	TTL	Static	130 mA	50 ns	5	0 to +70	16-Pin	•	
		DM54S206	TTL	Static	130 mA	80 ns	5	−55 to +125	16-Pin	•	
		DM74S206	TTL	Static	130 mA	60 ns	5	0 to +70	16-Pin	•	
		MM1101A	PMOS	Static	49 mA	1.5 μs	5 to −9	0 to +70	16-Pin	•	
		MM1101A-1	PMOS	Static	49 mA	1 μs	5 to −9	0 to +70	16-Pin	•	
		MM1101A-2	PMOS	Static	49 mA	500 ns	5 to −9	0 to +70	16-Pin	•	
		MM4250	PMOS	Static	49 mA	650 ns	5 to −9	−55 to +125	16-Pin	•	
		MM54C200	CMOS	Static	600 μA	400 ns	3 to 15	−55 to +125	16-Pin	•	
		MM74C200	CMOS	Static	600 μA	400 ns	3 to 15	−40 to +85	16-Pin	•	
	64 x 4	MM54C910	CMOS	Static	5 mA	860 ns	5	−55 to +125	18-Pin	•	
		MM74C910	CMOS	Static	4 mA	700 ns	5	−40 to +85	18-Pin	•	
1024	1024 x 1	MM2102A	NMOS	Static	50 mA	350 ns	5	0 to +70	16-Pin	•	
		MM2102A-L	NMOS	Static	33 mA	350 ns	5	0 to +70	16-Pin	•	
		MM2102A-2	NMOS	Static	50 mA	250 ns	5	0 to +70	16-Pin	•	
		MM2102A-2L	NMOS	Static	33 mA	250 ns	5	0 to +70	16-Pin	•	
		MM2102A-4	NMOS	Static	50 mA	450 ns	5	0 to +70	16-Pin	•	
		MM2102A-4L	NMOS	Static	33 mA	450 ns	5	0 to +70	16-Pin	•	
		MM2102A-6	NMOS	Static	50 mA	650 ns	5	0 to +70	16-Pin	•	
		MM2102A-6L	NMOS	Static	33 mA	650 ns	5	0 to +70	16-Pin	•	

Size	Organization	Part Number	Type	Operation	Maximum Supply Current	Maximum Access Time	Supply Voltage (V)	Temperature Range (°C)	Package	In Production	Future
1024	1024 x 1	MM54C929	CMOS	Static	4 mA	265 ns	5	−55 to +125	16-Pin	•	
		MM74C929	CMOS	Static	4 mA	240 ns	5	−40 to +85	16-Pin	•	
		MM74C929-3	CMOS	Static	4 mA	315 ns	5	−40 to +85	16-Pin	•	
		MM54C930	CMOS	Static	4 mA	265 ns	5	−55 to +125	18-Pin	•	
		MM74C930	CMOS	Static	4 mA	240 ns	5	−40 to +85	18-Pin	•	
		MM74C930-3	CMOS	Static	4 mA	315 ns	5	−40 to +85	18-Pin	•	
	256 x 4	MM2101A	NMOS	Static	55 mA	350 ns	5	0 to +70	22-Pin	•	
		MM2101A-L	NMOS	Static	44 mA	350 ns	5	0 to +70	22-Pin	•	
		MM2101A-2	NMOS	Static	55 mA	250 ns	5	0 to +70	22-Pin	•	
		MM2101A-4	NMOS	Static	55 mA	450 ns	5	0 to +70	22-Pin	•	
		MM2101A-4L	NMOS	Static	44 mA	450 ns	5	0 to +70	22-Pin	•	
		MM2101A-6	NMOS	Static	55 mA	650 ns	5	0 to +70	22-Pin	•	
		MM2101A-6L	NMOS	Static	44 mA	650 ns	5	0 to +70	22-Pin	•	
		MM2111A	NMOS	Static	55 mA	350 ns	5	0 to +70	18-Pin	•	
		MM2111A-L	NMOS	Static	44 mA	350 ns	5	0 to +70	18-Pin	•	
		MM2111A-2	NMOS	Static	55 mA	250 ns	5	0 to +70	18-Pin	•	
		MM2111A-4	NMOS	Static	55 mA	450 ns	5	0 to +70	18-Pin	•	
		MM2111A-4L	NMOS	Static	44 mA	450 ns	5	0 to +70	18-Pin	•	
		MM2111A-6	NMOS	Static	55 mA	650 ns	5	0 to +70	18-Pin	•	
		MM2111A-6L	NMOS	Static	44 mA	650 ns	5	0 to +70	18-Pin	•	
		MM2112A	NMOS	Static	55 mA	350 ns	5	0 to +70	16-Pin	•	
		MM2112A-L	NMOS	Static	44 mA	350 ns	5	0 to +70	16-Pin	•	
		MM2112A-2	NMOS	Static	55 mA	250 ns	5	0 to +70	16-Pin	•	
		MM2112A-4	NMOS	Static	55 mA	450 ns	5	0 to +70	16-Pin	•	
		MM2112A-4L	NMOS	Static	44 mA	450 ns	5	0 to +70	16-Pin	•	
		MM2112A-6	NMOS	Static	55 mA	650 ns	5	0 to +70	16-Pin	•	
		MM2112A-6L	NMOS	Static	44 mA	650 ns	5	0 to +70	16-Pin	•	
		MM54C920	CMOS	Static	4 mA	275 ns	5	−55 to +125	22-Pin	•	
		MM74C920	CMOS	Static	4 mA	250 ns	5	−40 to +85	22-Pin	•	
		MM74C920-3	CMOS	Static	3 mA	325 ns	5	0 to +70	22-Pin	•	
		MM54C921	CMOS	Static	4 mA	275 ns	5	−55 to +125	18-Pin	•	
		MM74C921	CMOS	Static	4 mA	250 ns	5	−40 to +85	18-Pin	•	
		MM74C921-3	CMOS	Static	3 mA	325 ns	5	0 to +70	18-Pin	•	

Size	Organization	Part Number	Type	Operation	Maximum Supply Current	Maximum Access Time	Supply Voltage (V)	Temperature Range (°C)	Package	In Production	Future
4096	1024 x 4	MM2114	NMOS	Static	90 mA	450 ns	5	0 to +70	18-Pin	•	
		MM2114L	NMOS	Static	65 mA	450 ns	5	0 to +70	18-Pin	•	
		MM2114-2	NMOS	Static	90 mA	200 ns	5	0 to +70	18-Pin	•	
		MM2114-2L	NMOS	Static	65 mA	200 ns	5	0 to +70	18-Pin	•	
		MM2114-3	NMOS	Static	90 mA	300 ns	5	0 to +70	18-Pin	•	
		MM2114-3L	NMOS	Static	65 mA	300 ns	5	0 to +70	18-Pin	•	
	4096 x 1	MM5257	NMOS	Static	90 mA	450 ns	5	0 to +70	18-Pin	•	
		MM5257-L	NMOS	Static	65 mA	450 ns	5	0 to +70	18-Pin	•	
		MM5257-2	NMOS	Static	90 mA	200 ns	5	0 to +70	18-Pin	•	
		MM5257-2L	NMOS	Static	65 mA	200 ns	5	0 to +70	18-Pin	•	
		MM5257-3	NMOS	Static	90 mA	300 ns	5	0 to +70	18-Pin	•	
		MM5757-3L	NMOS	Static	65 mA	300 ns	5	0 to +70	18-Pin	•	
		MM5257-6	NMOS	Static	90 mA	650 ns	5	0 to +70	18-Pin	•	
		MM5257-6L	NMOS	Static	65 mA	650 ns	5	0 to +70	18-Pin	•	
		MM4270	NMOS	Dynamic	60 mA	270 ns	−5, +12	−55 to +85	18-Pin	•	
		MM5270	NMOS	Dynamic	60 mA	200 ns	−5, +12	0 to +70	18-Pin	•	
		MM5270-5	NMOS	Dynamic	60 mA	270 ns	−5, +12	0 to +70	18-Pin	•	
		MM5271	NMOS	Dynamic	60 mA	250 ns	−5, +12	0 to +70	18-Pin	•	
		MM4280	NMOS	Dynamic	60 mA	270 ns	±5, +12	−55 to +85	22-Pin	•	
		MM5280	NMOS	Dynamic	60 mA	200 ns	±5, +12	0 to +70	22-Pin	•	
		MM5280-5	NMOS	Dynamic	60 mA	270 ns	±5, +12	0 to +70	22-Pin	•	
		MM5280-055	NMOS	Dynamic	60 mA	270 ns	±5, +12	0 to +55	22-Pin	•	
8192	8192 x 1	MM5298A-2	NMOS	Dynamic	40 mA	150 ns	±5, +12	0 to +70	16-Pin		•
		MM5298A-3	NMOS	Dynamic	40 mA	200 ns	±5, +12	0 to +70	16-Pin	•	
		MM5298A-4	NMOS	Dynamic	40 mA	250 ns	±5, +12	0 to +70	16-Pin	•	
		MM5298B-2	NMOS	Dynamic	40 mA	150 ns	±5, +12	0 to +70	16-Pin		•
		MM5298B-3	NMOS	Dynamic	40 mA	200 ns	±5, +12	0 to +70	16-Pin	•	
		MM5298B-4	NMOS	Dynamic	40 mA	250 ns	±5, +12	0 to +70	16-Pin	•	
16,384	16,384 x 1	MM5290-2	NMOS	Dynamic	40 mA	150 ns	±5, +12	0 to +70	16-Pin		•
		MM5290-3	NMOS	Dynamic	40 mA	200 ns	±5, +12	0 to +70	16-Pin	•	
		MM5290-4	NMOS	Dynamic	40 mA	250 ns	±5, +12	0 to +70	16-Pin	•	

TOTAL BITS	NO. PINS	PART NUMBER		ORGANIZATION	TYPICAL ACCESS IN ns	POWER SUPPLIES	LOGIC SPEC. (NOTE 2)
		−55°C TO +125°C	0°C TO +70°C				
1024	16	MM4210	MM5210	256 x 4	500	±12	Negative
	16	MM4211	MM5211	256 x 4	700	+5, −12	Negative
	24	MM4220	MM5220	256 x 4	500	±12	Negative
	24	MM4221	MM5221	256 x 4	700	+5, −12	Negative
2048	24	MM4213	MM5213	512 x 4	600	+5, −12	Positive
	24	MM4230	MM5230	512 x 4	500	±12	Negative
	24	MM4231	MM5231	512 x 4	640	+5, −12	Negative
	24	MM4243	MM5243	512 x 4	1000	+5, −12	Positive
4096	24	MM4232	MM5232	1024 x 4	800	+5, −12	Positive
1024	24	MM4220	MM5220	128 x 8	500	±12	Negative
	24	MM4221	MM5221	128 x 8	700	+5, −12	Negative
2048	24		MM1742	256 x 8	1000	+5, −9	Positive
	24	MM4213	MM5213	256 x 8	600	+5, −12	Positive
	24	MM4230	MM5230	256 x 8	500	±12	Negative
	24	MM4231	MM5231	256 x 8	640	+5, −12	Negative
	24	MM4243	MM5243	256 x 8	1000	+5, −12	Positive
4096	24	MM4214	MM5214	512 x 8	800	+5, −12	Positive
	24	MM4232	MM5232	512 x 8	800	+5, −12	Positive
	24	MM4233	MM5233	512 x 8	800	+5, −12	Positive
	24	MM4244	MM5244	512 x 8	750	+5, −12	Positive
16,384	24		MM2316A	2048 x 8	300	+5	Positive
	24		MM52116 (MM2316E)	2048 x 8	300	+5	Positive
32,768	24		MM52132	4096 x 8	300	+5	Positive
65,536	24		MM52164	8192 x 8	300	+5	Positive
	28		MM5235	8192 x 8	600	+5	Positive
3072	28	MM4229	MM5229	256 x 12	1000	+5, −12	Positive
12,288		MM4212	MM5212	1024 x 12	3500	+5, −12	Positive
		MM4215	MM5215	1024 x 12	1000	±12	Negative

Note 1: See NSC Memory Data Book for standard programs. All ROM's may be custom programmed.

Note 2: Devices are electrically specified with the following logic definitions. Positive logic: a logic "1" is the most positive logic voltage level. Negative logic: a logic "1" is the most negative logic voltage level.

CODE CONVERTER

PART NUMBER		ORGANIZATION	CONVERSION
BASIC NUMBER*	ALPHA DESIGNATOR		
MM4220/MM5220	AE	128 x 8	ASCII-7 → Hollerith
	AP		BCDIC → ASCII-7
	BL		Baudot → ASCII-7
	BM		Sine Look Up Table
	BN		Arctangent Look Up Table
	DF		Quick Brown Fox Generator
			BCD → ASCII-7 and
			BCD → 5-Bit Baudot
	EK		BCDIC → EBCDIC and
			ASCII-6 → EBCDIC
	LR		BCDIC → ASCII-7 and
			ASCII-7 → BCDIC
MM4221/MM5221	RQ	128 x 8	ASCII-7 → EIA RS-244A and EIA RS-244A → ASCII-7
	RR		ASCII-7 → EBCDIC
	TM		Baudot → ASCII-7 and
			ASCII-7 → Baudot
MM4230/MM5230	BO	256 x 8	Hollerith → ASCII-8
	FE		Selectric → EBCDIC and
			EBCDIC → Selectric
	JT		BCDIC → EBCDIC
			EBCDIC → BCDIC
	KP		ASCII-7 → Selectric and
			Selectric → ASCII-7
	QW		Hollerith → ASCII-8
	QX		EBCDIC → ASCII-8
	QY		ASCII-8 → EBCDIC
	RS		Binary to Modulo N
			Divider

CODE CONVERTER (Continued)

PART NUMBER		ORGANIZATION	CONVERSION
BASIC NUMBER*	ALPHA DESIGNATOR		
MM4231/MM5231	RP	256 x 8	EBCDIC → ASCII-7
MM4232/MM5232	AEI	512 x 8	Sine Look Up Tables. (These 3 may be Combined to Give Varying Resolution and Accuracy)
	AEJ		
	AEK		

CHARACTER GENERATOR

PART NUMBER		NO. OF CHARACTERS	FONT	SCAN	TYPE OF CHARACTERS
BASIC NUMBER	ALPHA DESIGNATOR				
MM5240	AA	64	8 x 5	Horizontal	ASCII-7 Graphic
	AE				ASCII-7 Lower Case Graphic with Control Symbols
	ABU				Hollerith Graphic
	ABZ				EBCDIC-8 Graphic
	ACA				IBM EBCDIC Graphic
MM5241	ABL	64	6 x 8	Vertical	ASCII-7 Graphic
	ABV				ECMA-7 (Scandinavian)
	ABW				ECMA-7 (German)
	ABX				ECMA-7 (General European)
	ABY				ECMA-7 (Spanish)
DM8678**	BWF	64	7 x 9	Horizontal	Upper Case Block
	BTK		7 x 9		Upper Case Script
	CAB		5 x 7		Upper Case Block
	CAD		7 x 9		Kata Kana
	CAE		7 x 9		Shifted Lower Case Block
	CAH		5 x 7		Shifted Lower Case Block
	CAS		7 x 9		IBM 3741 Selectric
MM52116	FDW	128	5 x 7	Horizontal	Upper/Lower Case Block
MM52116	FDX	128	7 x 9	Horizontal	Standard ASCII Character Set

*Part numbers with a 4 prefix are for −55°C to +125°C temperature range and with a 5 prefix are for 0°C to +70°C temperature range

**This bipolar (TTL) device performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing in a 16-pin package with 5V operation at 16 MHz clock rate

Section 1

MOS RAMs

1

MOS static and dynamic read/write memory devices constitute the majority of semiconductor memory worldwide consumption. National plays a leadership role in this area as a major supplier of products included in this section. For example, the MM5280N-055 was the first 4k dynamic RAM offered at a published price of 0.06 cents per bit (lower in high volume). In addition to the devices included here, National is developing more advanced higher density, higher speed RAMs for future equipment designs. Contact your local National representative for further assistance.

National Semiconductor

MOS RAMs

MM1101, MM11011, MM1101A, MM1101A1, MM1101A2, MM4250 256-Bit (256 × 1) Static RAMs

general description

The MM1101 family of fully decoded 256 word x 1-bit random access memories are monolithic MOS integrated circuits using silicon gate low threshold technology to achieve bipolar compatibility. They are static, require no clocks, and hold information indefinitely, subject to the integrity of the power supply voltages.

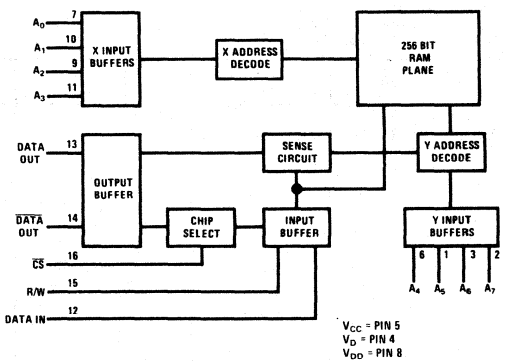
features

- Fast access times — MM1101A2 500 ns max; MM11011, MM1101A1 1.0 μs max; MM1101, MM1101A 1.5 μs max; MM4250 650 ns max
- Improved speed/power product — MM1101A2 1/3 of 1101A
- Low power operation — 1.5 mW/bit
- Fewer system components - bipolar compatible input and output
- Second source flexibility - MM1101, MM1101A MM11011, MM1101A1 second sources available
- TRI-STATE™ output - wired OR capability
- Specified ambient temperature 0°C to +70°C for MM1101 family; −55°C to +125°C for MM4250

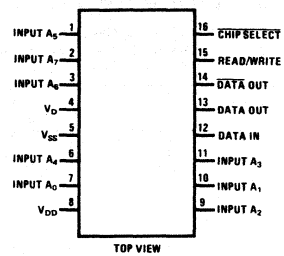
applications

- High speed buffer memories
- Local memory store

block and connection diagrams



Dual-In-Line Package



Order Number MM1101D, MM1101AD, MM1101A1D, MM1101A2D, MM11011D or MM4250D
See NS Package D16C

Order Number MM1101N, MM1101AN, MM1101A1N, MM1101A2N or MM11011N
See NS Package N16A

absolute maximum ratings

All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{SS}	+0.3V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{SS}	−16V
Power Dissipation at Room Temperature	700 mW
Operating Temperature	
MM1101 Family	0°C to +70°C ambient
MM4250	−55°C to +125°C ambient
Storage Temperature	−66°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

dc characteristics

T_A = 0°C to +70°C for MM1101 Family, T_A = −55°C to +125°C for MM4250;
V_{SS} = +5V ±5%, V_D = V_{DD} = −9V ±5% for MM4250, MM1101A, MM1101A1, MM1101A2;
V_{SS} = +5V ±5%, V_D = −10V ±5%, V_{DD} = −7V ±5%, for MM1101, MM11011 (unless otherwise specified).

SYMBOL		TEST	CONDITIONS	MM1101 FAMILY MIN	MM1101 FAMILY TYP	MM1101 FAMILY MAX	MM4250 MIN	MM4250 TYP	MM4250 MAX	UNITS
	I_{LI}	Input Load Current (All Input Pins)	V_{IN} = 0.0		0.001	0.5			1.0	µA
	I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, CS = V_{SS} − 2.0V		0.001	0.5			1.0	µA
MM4250	I_{DD}	Power Supply Current, V_{DD}	T_A = 25°C, Continuous Operation		13.0	19.0		13.0	19.0	mA
MM1101A	I_{DD}	Power Supply Current, V_{DD}	T_A = 0°C, Continuous Operation			25.0			25.0	mA
MM1101A1 MM1101A2	I_D	Power Supply Current, V_D	T_A = 25°C, I_{DL} = 0.0 mA		12.0	18.0		12.0	18.0	mA
	I_D	Power Supply Current, V_D	T_A = 0°C			24.0			24.0	mA
	V_{IL}	Input LOW Voltage		V_{SS} − 10		V_{SS} − 4.2	V_{SS} − 10		V_{SS} − 4.2	V
	V_{IH}	Input HIGH Voltage		V_{SS} − 2.0		V_{SS} + 0.3	V_{SS} − 2.0		V_{SS} + 0.3	V
	I_{OL}	Output Sink Current	V_{OUT} = +0.45V, T_A = 25°C	3.0	8.0		3.0	8.0		mA
	I_{OL}	Output Sink Current	V_{OUT} = +0.45V, T_A = 70°C	2.0			2.0			mA
	I_{CF}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		6.0	13.0		6.0	13.0	mA
	I_{OH}	Output Source Current	V_{OUT} = 0.0V, T_A = +25°C	−3.0	−8.0		−3.0	−8.0		mA
	I_{OH}	Output Source Current	V_{OUT} = 0.0V, T_A = +70°C	−2.0	−7.0		−2.0	−7.0		mA
	V_{OH}	Output HIGH Voltage	I_{OH} = −100 µA	3.5	4.9		3.5	4.9		V
	C_{IN}	Input Capacitance (Note 3) (All Input Pins)	V_{IN} = V_{SS}, f = 1 MHz		7.0	10.0		7.0	10.0	pF
	C_{OUT}	Output Capacitance	V_{OUT} = V_{SS}, f = 1 MHz		7.0	10.0		7.0	10.0	pF
	C_V	V_D Power Supply Capacitance	V_D = V_{SS}, f = 1 MHz		20.0	35.0		20.0	35.0	pF
MM1101	I_{DD}	Power Supply Current, V_{DD}	T_A = 25°C, Continuous Operation		14.0	18.0				mA
MM11011	I_D	Power Supply Current, V_D	T_A = 25°C, I_{OL} = 0.0 mA		17.0	20.0				mA

ac characteristics

T_A = 0°C to +70°C for MM1101 Family, T_A = −55°C to +125°C for MM4250;
V_{SS} = +5V ±5%, V_D = V_{DD} = −9V ±5% for MM4250, MM1101A, MM1101A1, MM1101A2;
V_{SS} = +5V ±5%, V_D = −10V ±5%, V_{DD} = −7V ±5%, for MM1101, MM11011 (unless otherwise specified).

SYMBOL	TEST	MIN	TYP (Note 2)	MAX	UNITS
t_{rc}	Read Cycle MM1101, MM1101A	1.5			µs
	MM11011, MM1101A1	1.0			µs
	MM1101A2	500.0			ns
	MM4250	650.0			ns
t_{ac}	Address to Chip Select Delay				
	MM1101, MM1101A,			1.2 (Note 4)	µs
	MM11011, MM1101A1			0.7 (Note 4)	µs
	MM1101A			0.2 (Note 4)	µs
	MM4250			0.35 (Note 4)	µs
t_a	Access Time MM1101, MM1101A		0.85	1.5	µs
	MM11011, MM1101A1		0.65	1.0	µs
	MM1101A2		400.0	500.0	ns
	MM4250		400.0	650.0	ns
t_{oh}	Previous Read Data Valid	50.0			ns

Note 1: All voltage measurements are referenced to ground.
Note 2: Typical values are at T_A = +25°C and nominal supply voltages.
Note 3: Capacitances are measured periodically only.
Note 4: Maximum value for t_{ac} measured at minimum read cycle.

ac characteristics (con't)

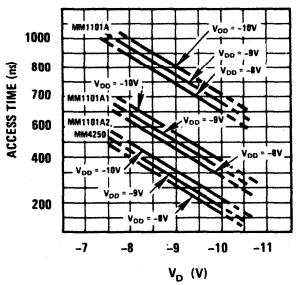
WRITE CYCLE (MM1101, MM11011, MM1101A, MM1101A1, MM1101A2)

SYMBOL	TEST	MIN	TYP (Note 2)	MAX	UNITS
t_{WC}	Write Cycle	0.8			μs
t_{WD}	Address to Write Pulse Delay	0.3			μs
t_{WP}	Write Pulse Width	0.4			μs
t_{DW}	Data Set up Time	0.3			μs
t_{DH}	Data Hold Time	0.1			μs
WRITE CYCLE (MM4250)					
t_{wc}	Write Cycle	1.0			μs
t_{wd}	Address to Write Pulse Delay	0.35			μs
t_{wp}	Write Pulse Width	0.50			μs
t_{dw}	Data Set-up Time	0.35			μs
t_{dh}	Data Hold Time	0.15			μs
CHIP SELECT AND DESELECT (MM1101, MM11011, MM1101A, MM1101A1, MM1101A2, MM4250)					
t_{CW}	Chip Select Pulse Width	0.4			μs
t_{CS}	Access Time Through Chip Select Input		0.2	0.3	μs
t_{CD}	Chip Deselect Time		0.1	0.3	μs

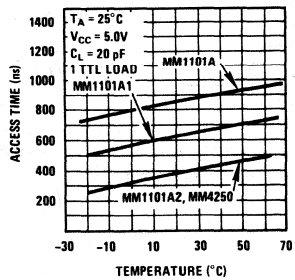
Note 1: All voltage measurements are referenced to ground.
Note 2: Typical values are at T_A = +25°C and nominal supply voltages.
Note 3: Capacitances are measured periodically only.
Note 4: Maximum value for t_{ac} measured at minimum read cycle.

typical performance characteristics

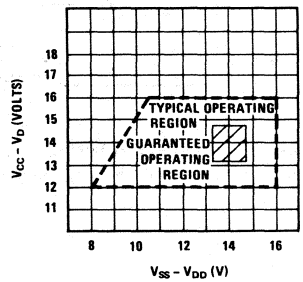
Typical Access Time vs Voltage



Typical Access Time vs Temperature

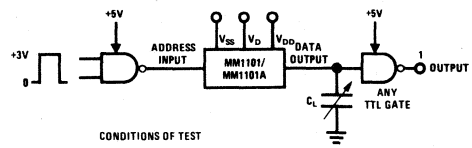


MM1101A, MM1101A1, MM1101A2, MM4250 Operating Region



ac test circuit

Test Setup for MM1101A and MM1101A Speed Measurement

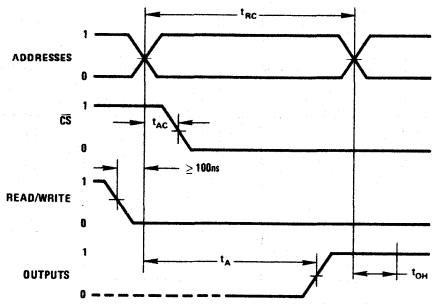


CONDITIONS OF TEST

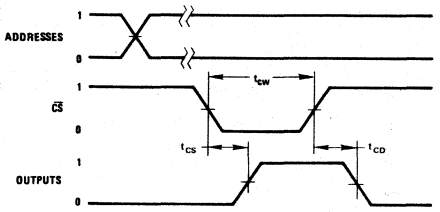
Input pulse amplitudes: 0V to +5.0V.
Input pulse rise and fall times ≤ 10 ns.
Speed measurements are referenced to the 1.5V level (unless otherwise noted); at the output of the TTL gate (t_{pd} ≥ 10 ns) C_L ≥ 20 pF.

switching time waveforms

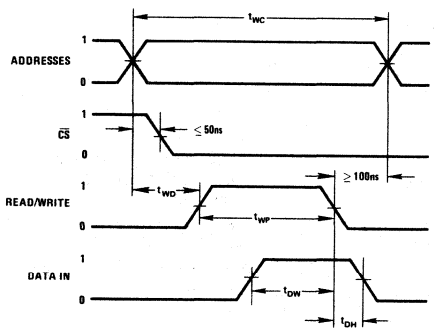
Read Cycle



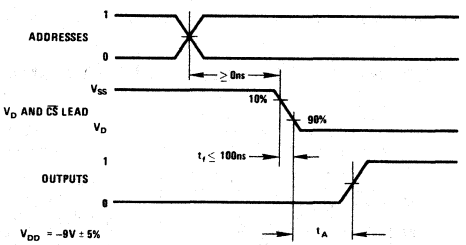
Chip Select and Deselect



Write Cycle



Power Switching For Reduced Power Applications



Note 1: All inputs of the MM1101A accept standard TTL outputs with V_{CC} = +5.0V ±5%.
Note 2: Maximum value for t_{AC} measured at minimum read cycle.

National Semiconductor

MOS RAMs

MM2101A, MM2101AL Family 1024-Bit (256 × 4) Static RAMs

General Description

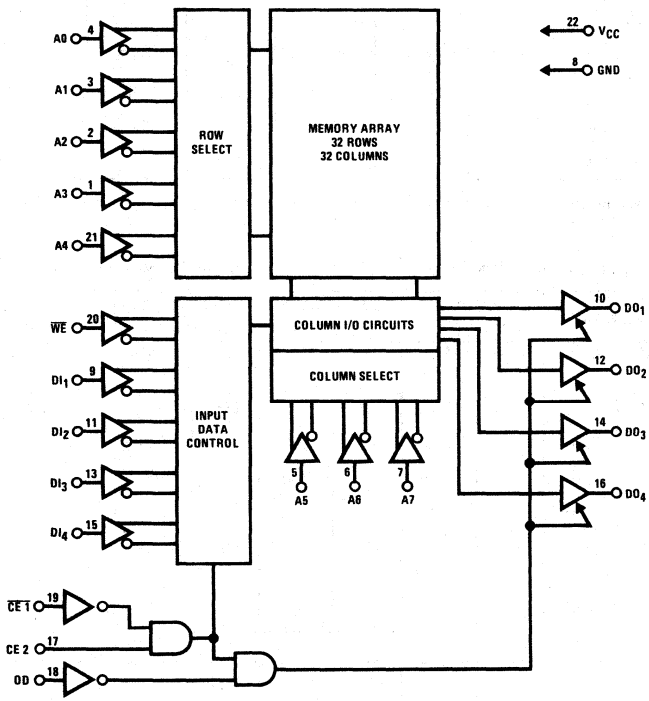
The MM2101A family of high speed 256 x 4-bit static random access read/write memories is manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. Two chip enable inputs and an output disable input controlling the TRI-STATE® output allow easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

Features

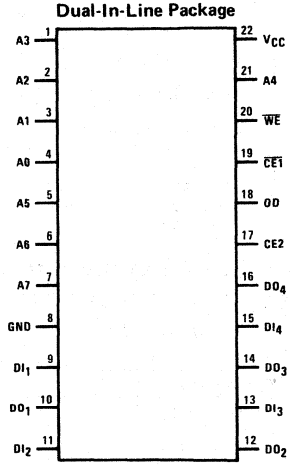
- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

Block Diagram



Connection Diagram

Dual-In-Line Package

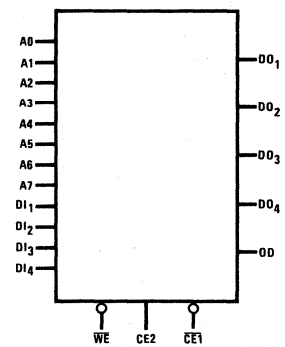


TOP VIEW

Order Number MM2101AJ, AJ-2, AJ-4, AJ-6, AJ-L, AJ-4L or AJ-6L
See NS Package J22A

Order Number MM2101AN, AN-2, AN-4, AN-6, AN-L, AN-4L or AN-6L
See NS Package N22A

Logic Symbol



Truth Table

$\overline{CE1}$	CE2	$\overline{WE}$	OD	D_{IN}	D_{OUT}	MODE
H	X	X	X	X	Hi-Z	Not Selected
X	L	X	X	X	Hi-Z	Not Selected
L	H	L	H*	L	Hi-Z*	Write "0"
L	H	L	H*	H	Hi-Z*	Write "1"
L	H	H	L	X	D_{OUT}	Read

*For common I/O operation, OD should be tied low and for separate I/O operation, D_{OUT} follows D_{IN}.

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = \pm5\%$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2101A MM2101A-2 MM2101A-4 MM2101A-6		MM2101A-L MM2101A-4L MM2101A-6L		UNITS
			MIN	MAX	MIN	MAX	
I_{LI}	Input Load Current	V_{IN} = 0 to 5.25V		10		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		5		5	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10		−10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open, $T_A = 25°C$		50		39	mA
I_{CC2}	Power Supply Current	All Inputs = 5.25V, Data Output Open, $T_A = 0°C$		55		44	mA
V_{IL}	Input Low Voltage		−0.5	0.65	−0.5	0.65	V
V_{IH}	Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.2		2.2		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

AC Electrical Characteristics (With standard load) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm5\%$ unless otherwise specified.

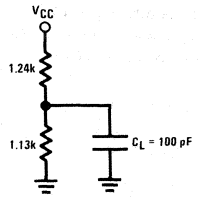
SYMBOL	PARAMETER	MM2101A-2		MM2101A MM2101A-L		MM2101A-4 MM2101A-4L		MM2101A-6 MM2101A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE *(Figure 1)*										
t_{RC}	Read Cycle	250		350		450		650		ns
t_A	Access Time		250		350		450		650	ns
t_{CO}	Chip Enable to Output Time		125		175		200		400	ns
t_{OD}	Output Disable to Output		100		125		175		350	ns
t_{OH}	Previous Read Data Valid After Change of Address	30		40		40		40		ns
t_{DF}	Data Output to Hi-Z State	0	100	0	125	0	150	0	150	ns
WRITE CYCLE *(Figure 2)*										
t_{WC}	Write Cycle	250		350		450		650		ns
t_{AW}*	Address to Write Set-Up	0		0		0		0		ns
t_{WP}	Write Pulse Width	100		150		175		400		ns
t_{WR}*	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Set-Up Time	100		150		175		400		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable to Write Set-Up	100		150		175		400		ns
t_{DS}	Output Disable Set-Up	20		20		20		50		ns

*The $\overline{WE}$ line must be high for at least 30 ns between consecutive write cycles

AC Electrical Characteristics $T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	TYP	MAX	UNITS
CAPACITANCE (Note 2)				
C_{IN}	Input Capacitance (All Inputs $V_{IN} = 0V$)	4	8	pF
C_{OUT}	Output Capacitance, $V_O = 0V$	8	12	pF

AC Test Circuit and Switching Time Waveforms



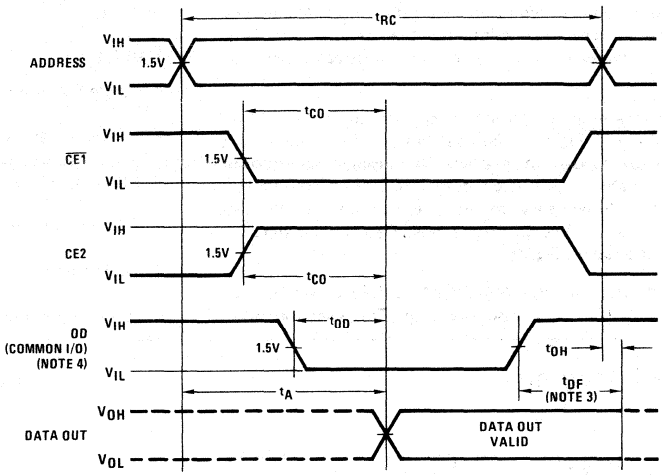


FIGURE 1. Read Cycle

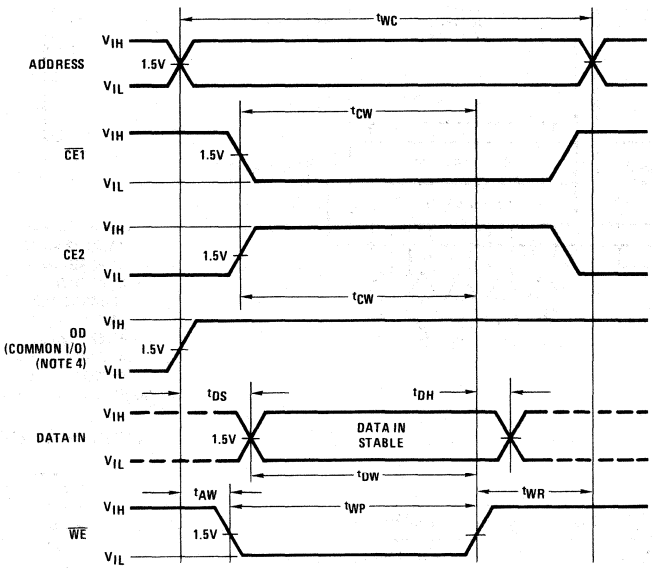


FIGURE 2. Write Cycle

Note 1: Typical values are for $T_A = 25°C$ and typical supply voltage.

Note 2: This parameter is periodically sampled and is not 100% tested.

Note 3: t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2 or OD, whichever occurs first.

Note 4: OD should be tied low for separate I/O operation.

National Semiconductor

MM2102A, MM2102AL Family 1024-Bit (1024 × 1) Static RAMs

general description

The MM2102A family of high speed 1024 x 1-bit static random access read/write memories is manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

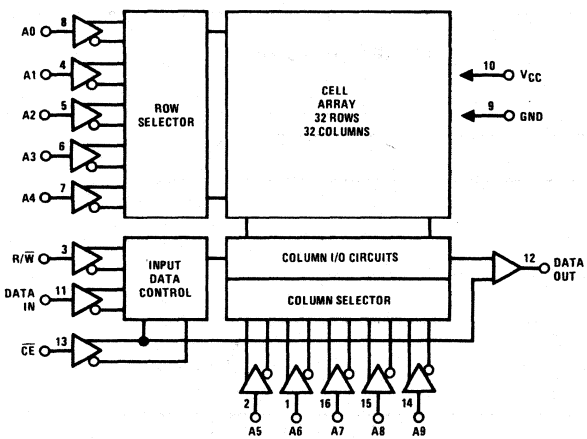
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

In addition to the MM2102A, a low power version, the MM2102AL, is also available. This selection offers a maximum operating current of 33 mA and a guaranteed standby mode down to a power supply voltage of 1.5V.

features

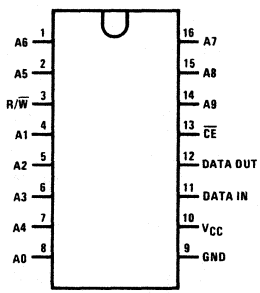
- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

block diagram



connection diagram

Dual-In-Line Package



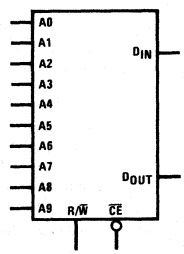
TOP VIEW

Order Number:	Order Number:
MM2102AJ-2L	MM2102AN-2L
MM2102AJ-2	MM2102AN-2
MM2102AJ-L	MM2102AN-L
MM2102AJ	MM2102AN
MM2102AJ-4L	MM2102AN-4L
MM2102AJ-4	MM2102AN-4
MM2102AJ-6L	MM2102AN-6L
MM2102AJ-6	MM2102AN-6
See NS Package J16A	See NS Package N16A

truth table

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	Hi-Z	Not selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

logic symbol



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Input Low Voltage	−0.5	0.8	V
Input High Voltage	2.0	V_{CC}	V

dc electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = \pm5\%$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2102A, MM2102A-2, MM2102A-4, MM2102A-6		MM2102A-L, MM2102A-2L, MM2102A-4L, MM2102A-6L		UNITS
			MIN	MAX	MIN	MAX	
I_{LI}	Input Load Current	V_{IN} = 0 to 5.25V		10		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		5		5	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10		−10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 25°C		45		31	mA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 0°C		50		33	mA
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.4		2.4		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

ac electrical characteristics (With standard load) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm5\%$ unless otherwise specified.

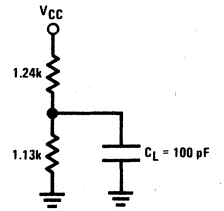
SYMBOL	PARAMETER	MM2102A-2, MM2102A-2L		MM2102A, MM2102A-L		MM2102A-4, MM2102A-4L		MM2102A-6, MM2102A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE *(Figure 1)*										
t_{RC}	Read Cycle	250		350		450		650		ns
t_A	Access Time		250		350		450		650	ns
t_{CO}	Chip Enable to Output Time		100		150		200		200	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50		ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0		ns
WRITE CYCLE *(Figure 2)*										
t_{WC}	Write Cycle	250		350		450		650		ns
t_{AW}	Address to Write Set-Up	20		20		20		20		ns
t_{WP}	Write Pulse Width	100		150		200		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Date Set-Up Time	85		125		175		175		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable To Write Set-Up	100		150		200		200		ns

ac electrical characteristics $T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	LIMIT (pF)	
		TYP	MAX
CAPACITANCE [2]			
C_{IN}	Input Capacitance (All Inputs V_{IN} = 0V)	3	5
C_{OUT}	Output Capacitance, V_O = 0V	4	6

Note 2: This parameter is guaranteed by periodic testing

ac test circuit



switching time waveforms

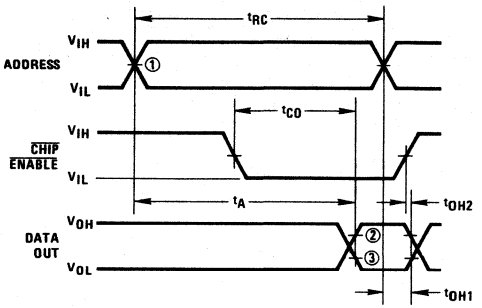


FIGURE 1. Read Cycle

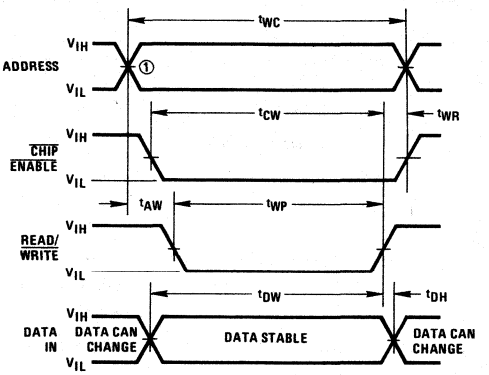


FIGURE 2. Write Cycle

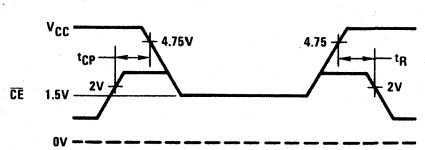
Note ①: Input reference level for timing is 1.5V.
Note ②: V_{OH} = 2V is reference level for output high.
Note ③: V_{OL} = 0.8V is reference level for output low.
Note ④: Input rise and fall times are 10 ns.

standby characteristics $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	CONDITIONS	MM2102A, MM2102A-2, MM2102A-4, MM2102-6			MM2102A-L, MM2102A-2L, MM2102A-4L, MM2102A-6L			UNITS
			MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	
V_{PD}	V_{CC} in Standby		1.5			1.5			V
V_{CES}	$\overline{CE}$ Bias in Standby	$2 \leq V_{PD} \leq V_{CCMAX}$	2.0			2.0			V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}			V_{PD}			V
I_{PD1}	Standby Current	All Inputs = V_{PD} = 1.5V			28			23	mA
I_{PD2}	Standby Current	All Inputs = V_{PD} = 2V			38			28	mA
t_{CP}	Chip Deselect to Standby Time		0			0			ns
t_R	Recovery Time (Note 4)		t_{RC}			t_{RC}			ns

Note 3: Typical values at $T_A = 25°C$.
Note 4: $t_R = t_{RC}$ = read cycle time.

standby waveforms



National Semiconductor

MM2111A, MM2111AL Family 1024-Bit (256 × 4) Static RAMs

General Description

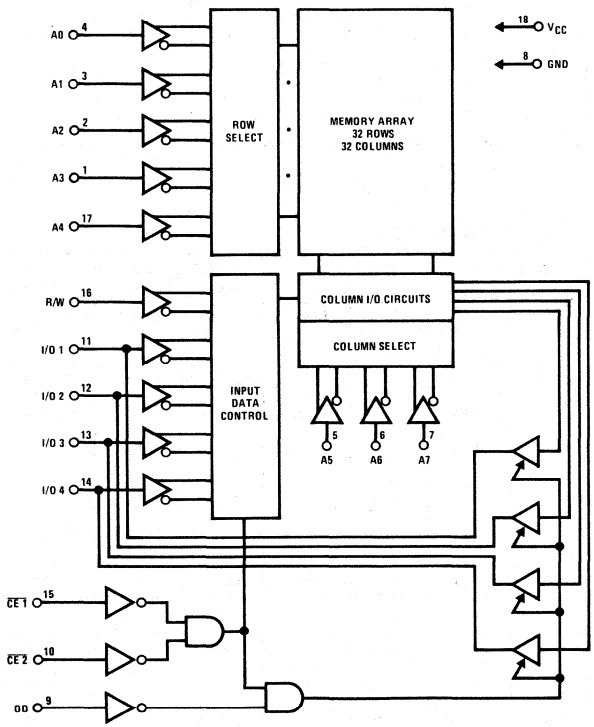
The MM2111A family of high speed 256 x 4-bit static random access read/write memories is manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. Two chip enable inputs and an output disable input control the TRI-STATE® output allowing easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity. Common input/output pins are provided.

Features

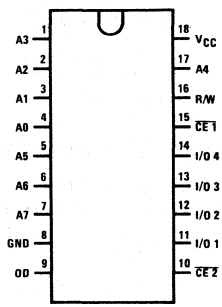
- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

Block Diagram



Connection Diagram

Dual-In-Line Package

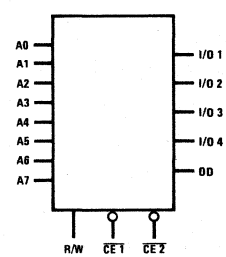


TOP VIEW

Order Number MM2111AJ, AJ-2, AJ-4, AJ-6, AJ-L, AJ-4L or AJ-6L
See NS Package J18A

Order Number MM2111AN, AN-2, AN-4, AN-6, AN-L, AN-4L or AN-6L
See NS Package N18A

Logic Symbol



Truth Table

OD	$\overline{CE1}$	$\overline{CE2}$	R/W	D_{IN}	D_{OUT}	MODE
X	X	H	X	X	Hi-Z	Not selected
H	L	L	L	L	Hi-Z	Write "0"
H	L	L	L	H	Hi-Z	Write "1"
L	L	L	H	X	D_{OUT}	Read
X	H	X	X	X	Hi-Z	Not selected

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = \pm5\%$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2111A MM2111A-2 MM2111A-4 MM2111A-6		MM2111A-L MM2111A-4L MM2111A-6L		UNITS
			MIN	MAX	MIN	MAX	
I_{LI}	Input Load Current	V_{IN} = 0 to 5.25V		10		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		5		5	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10		−10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open, $T_A = 25°C$		50		39	mA
I_{CC2}	Power Supply Current	All Inputs = 5.25V, Data Output Open, $T_A = 0°C$		55		44	mA
V_{IL}	Input Low Voltage		−0.5	0.65	−0.5	0.65	V
V_{IH}	Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.2		2.2		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

AC Electrical Characteristics

(With standard load) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm5\%$ unless otherwise specified.

SYMBOL	PARAMETER	MM2111A-2		MM2111A MM2111A-L		MM2111A-4 MM2111A-4L		MM2111A-6 MM2111A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE *(Figure 1)*										
t_{RC}	Read Cycle	250		350		450		650		ns
t_A	Access Time		250		350		450		650	ns
t_{CO}	Chip Enable to Output Time		125		175		200		400	ns
t_{OH}	Previous Read Data Valid with Respect to Address	30		40		40		40		ns
t_{OD}	Output Disable to Output		100		125		175		350	ns
t_{DF}	Data Output to Hi-Z State	0	100	0	125	0	150	0	150	ns
WRITE CYCLE *(Figure 2)*										
t_{WC}	Write Cycle	250		350		450		650		ns
t_{AW}*	Address to Write Set-Up	0		0		0		0		ns
t_{WP}	Write Pulse Width	100		150		175		400		ns
t_{WR}*	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Set-Up Time	100		150		175		400		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable to Write Set-Up	100		150		175		400		ns
t_{DS}	Output Disable Set-Up	20		20		20		50		ns

*The R/W line must be high for at least 30 ns between consecutive write cycles

AC Electrical Characteristics $T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	TYP	MAX	UNITS
CAPACITANCE (Note 2)				
C_{IN}	Input Capacitance (All Inputs $V_{IN} = 0V$)	4	8	pF
C_{OUT}	Output Capacitance, $V_O = 0V$	10	15	pF

Note 2: This parameter is guaranteed by periodic testing.

AC Test Circuit and Switching Time Waveforms

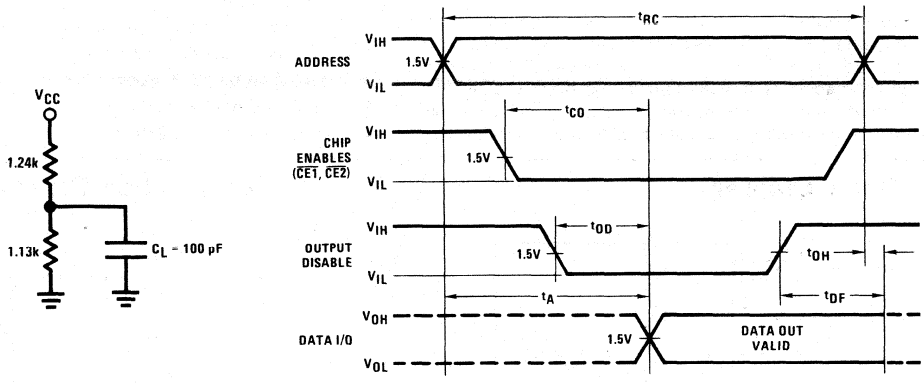


FIGURE 1. Read Cycle

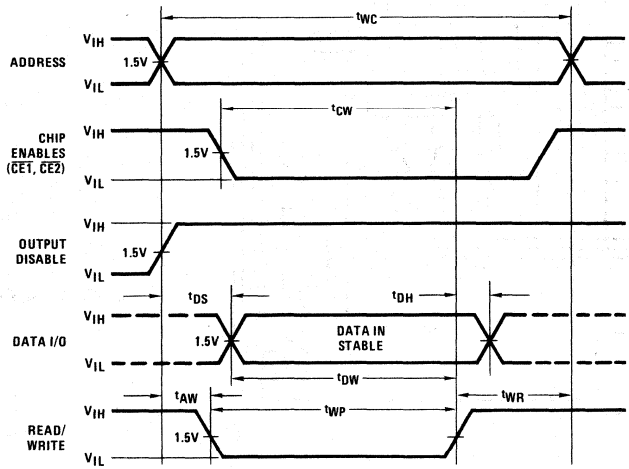


FIGURE 2. Write Cycle

Note 1: Typical values are for $T_A = 25°C$ and typical supply voltage.
Note 2: This parameter is periodically sampled and is not 100% tested.
Note 3: t_{DF} is with respect to the trailing edge of $\overline{CE\,1}$, $\overline{CE\,2}$ or OD, whichever occurs first.

National Semiconductor

MM2112A, MM2112AL Family 1024-Bit (256 × 4) Static RAMs

General Description

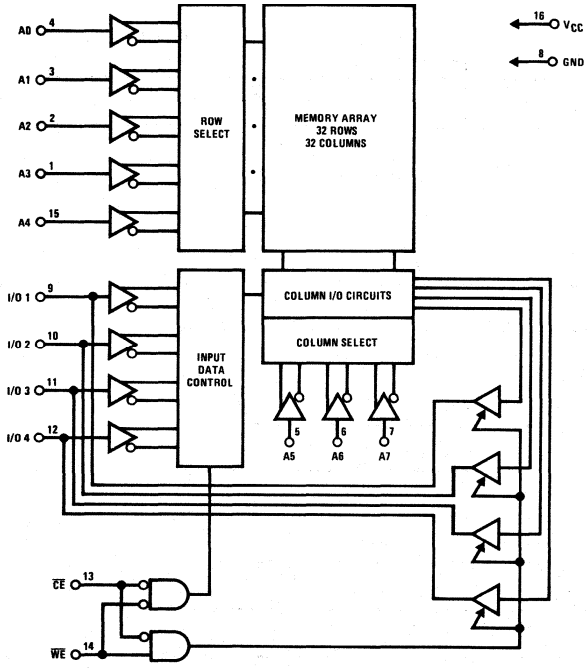
The MM2112A family of high speed 256 x 4-bit static random access read/write memories is manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity. Common input/output pins are provided.

Features

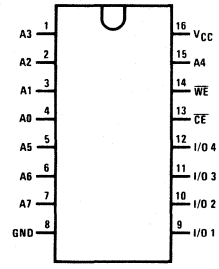
- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

Block Diagram



Connection Diagram

Dual-In-Line Package

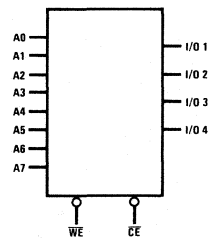


TOP VIEW

Order Number MM2112AJ, AJ-2, AJ-4, AJ-6, AJ-L, AJ-4L or AJ-6L
See NS Package J16A

Order Number MM2112AN, AN-2, AN-4, AN-6, AN-L, AN-4L or AN-6L
See NS Package N16A

Logic Symbol



Truth Table

$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	X	X	Hi-Z	Not Selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = \pm5\%$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2112A MM2112A-2 MM2112A-4 MM2112A-6		MM2112A-L MM2112A-4L MM2112A-6L		UNITS
			MIN	MAX	MIN	MAX	
I_{LI}	Input Load Current	V_{IN} = 0 to 5.25V		10		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		5		5	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10		−10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 25°C		50		39	mA
I_{CC2}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 0°C		55		44	mA
V_{IL}	Input Low Voltage		−0.5	0.65	−0.5	0.65	V
V_{IH}	Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.2		2.2		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

AC Electrical Characteristics (With standard load) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm5\%$ unless otherwise specified.

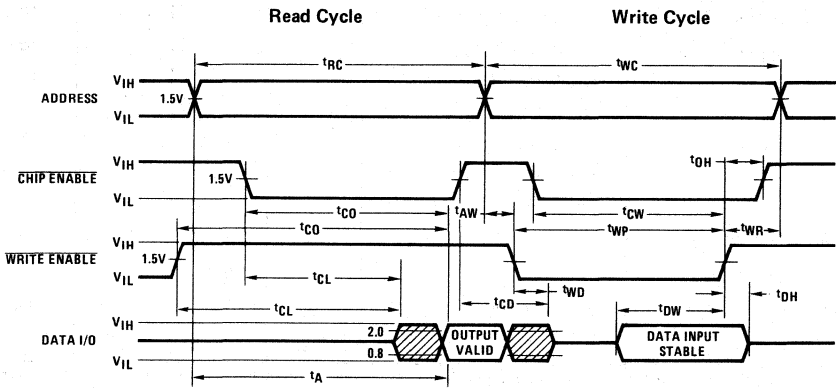
SYMBOL	PARAMETER	MM2112A-2		MM2112A MM2112A-L		MM2112A-4 MM2112A-4L		MM2112A-6 MM2112A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE										
t_{RC}	Read Cycle	250		350		450		650		ns
t_A	Access Time		250		350		450		650	ns
t_{CO}	Chip Enable to Valid Output Time		125		175		200			ns
t_{OH}	Previous Read Data Valid with Respect to Address	30		40		40		40		ns
t_{CL}	Output Enabled to Output ON Delay (Note 1)	5		5		5		5		ns
t_{CD}	Chip Enable to Output Disable Time		100		125		150		150	ns
WRITE CYCLE										
t_{WC}	Write Cycle	250		350		450		650		ns
t_{AW}	Address to Write Set-Up (Note 3)	0		0		0		0		ns
t_{WP}	Write Pulse Width (Note 2)	100		150		175		200		ns
t_{WR}	Write Recovery Time (Note 3)	0		0		0		0		ns
t_{DW}	Data Set-Up Time	100		150		175		200		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable to Write Set-Up	100		150		175		200		ns
t_{CH}	Chip Enable Hold Time	0		0		0		0		ns
t_{WD}	Write to Output Disable Time	100		125		150		150		ns

AC Electrical Characteristics $T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	TYP	MAX	UNITS
CAPACITANCE (Note 2)				
C_{IN}	Input Capacitance (All Inputs V_{IN} = 0V)	4	8	pF
C_{OUT}	Output Capacitance, V_O = 0V	10	15	pF

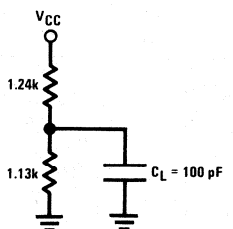
Note 2: This parameter is guaranteed by periodic testing.

Switching Time Waveform



Note 1: Output is enabled and t_{CO}/t_{CL} commence only with both $\overline{CE}$ low and $\overline{WE}$ high.
Note 2: Minimum t_{WP} is valid when $\overline{CE}$ has been high at least t_{CD} before $\overline{WE}$ goes low. Otherwise, $t_{WP(MIN)} = t_{DW(MIN)} + t_{CD(MAX)}$.
Note 3: The $\overline{WE}$ line must be high for at least 30 ns between consecutive write cycles.

AC Test Circuit



National Semiconductor

MM2114, MM2114L Family 4096-Bit (1024 × 4) Static RAMs

General Description

The MM2114 family of 1024-word by 4-bit static random access memories is fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

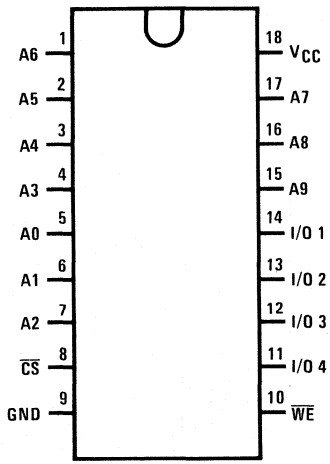
The separate chip select input ($\overline{CS}$) allows easy memory expansion by OR-tying individual devices to a data bus.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—down to 200 ns access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Standard 18-pin dual-in-line package

Connection Diagram

Dual-In-Line Package

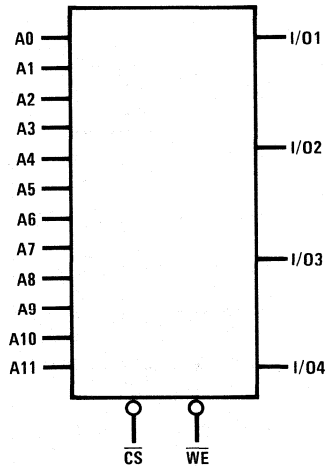


TOP VIEW

Order Number MM2114J, J-2, J-3, J-L, J-2L or J-3L
See NS Package J18A

Order Number MM2114N, N-2, N-3, N-L, N-2L or N-3L
See NS Package N18A

Logic Symbol



Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	MODE
H	X	Hi-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	D_{OUT}	Read

Functional Description

Two pins control the operation of the MM2114. Chip Select ($\overline{CS}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CS}$ and $\overline{WE}$ controls.

READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CS}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CS}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

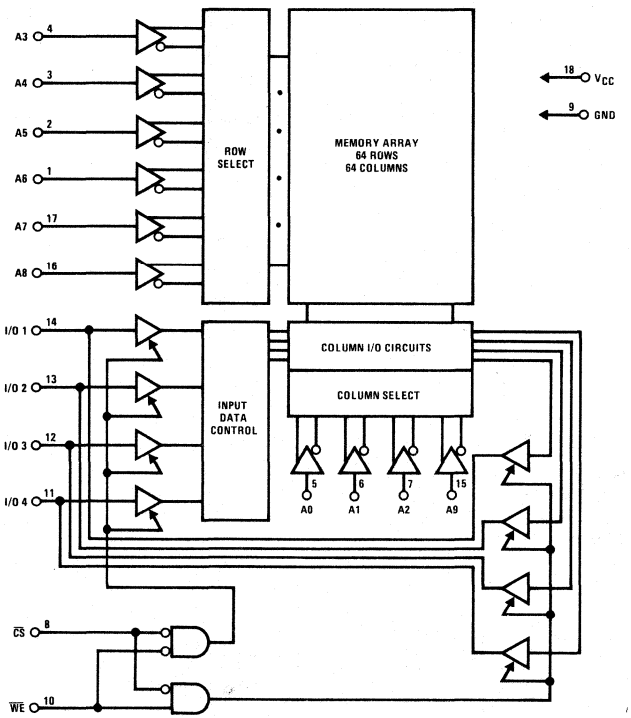
Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CS}$ has enabled the output buffer prior to data arrival. Chip Select-to-output delay, t_{CO}, is the time required for $\overline{CS}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CS}$ continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CS}$ and $\overline{WE}$ are low. Minimum write pulse width, t_{WP}, refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CS}$ continuously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CS}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Stand-by operation allows data to be maintained with approximately 50% less operating current. The 2 requirements to guarantee data retention are: a) the power supply voltage must meet the condition $V_{CC} \geq 1.5V$, and b) $\overline{CS}$ must be controlled; to disable the chip prior to reducing V_{CC}, to keep it disabled during the time V_{CC} is reduced, and to maintain the disabled state long enough after V_{CC} is increased to normal for the chip to recover. These requirements are shown by the stand-by waveforms and characteristics.

Block Diagram



Absolute Maximum Ratings

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MM2114 MM2114-2 MM2114-3		MM2114-L MM2114-2L MM2114-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		−0.5	0.8	−0.5	0.8	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -1.0$ mA	2.4		2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.1$ mA		0.4		0.4	V
I_{LI}	Input Load Current	$V_{IN} = 0$ to 5.25V	−10	10	−10	10	μA
I_{LO}	Output Leakage Current	$V_O = 4V$ to 0.4V, $\overline{CS} = V_{IH}$	−10	10	−10	10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, $T_A = 25°C$		95		65	mA
I_{CC2}	Power Supply Current	All Inputs = 5.25V, $T_A = 0°C$		100		70	mA

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, (Note 2)

SYMBOL	PARAMETER	MM2114-2 MM2114-2L		MM2114-3 MM2114-3L		MM2114 MM2114-L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Time ($\overline{WE} = V_{IH}$)		200		300		450	ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Select to Output Valid		70		100		120	ns
t_{CX}	Chip Select to Output Active	20		20		20		ns
t_{COT}	Chip Select to Output TRI-STATE	0	40	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	10		10		10		ns
WRITE CYCLE								
t_{WC}	Write Cycle Time		200		300		450	ns
t_{AW}	Address to Write Set-Up Time	20		20		20		ns
t_{WP}	Write Pulse Width	100		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DS}	Data Set-Up Time	100		150		200		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WOT}	Write Enable to Output TRI-STATE	0	40	0	80	0	100	ns
t_{WO}	Write Enable to Output Valid		80		100		120	ns

Note 1: Typical values at $T_A = 25°C$.

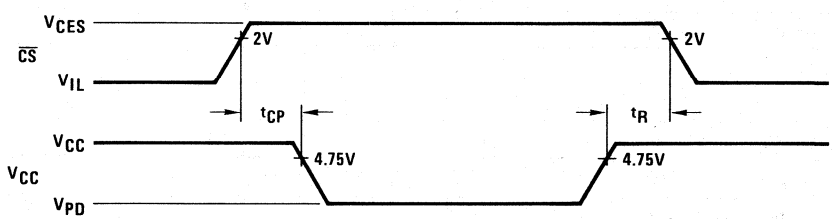
Note 2: All input transitions ≤ 10 ns. Timing referenced to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ for inputs, 0.8V and 2V for output. For test purposes, input levels should swing between 0V and 3V. Output load = 1 TTL gate and $C_L = 100$ pF.

Standby Characteristics $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	CONDITIONS	MM2114 MM2114-2 MM2114-3		MM2114-L MM2114-2L MM2114-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{PD}	V_{CC} in Stand-by		1.5		1.5		V
V_{CES}	$\overline{CS}$ Bias in Stand-by	$2 \leq V_{PD} \leq V_{CC(MAX)}$	2.0		2.0		V
V_{CES}	$\overline{CS}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}		V_{PD}		V
I_{PD1}	Stand-by Current	All Inputs = V_{PD} = 1.5V		70		45	mA
I_{PD2}	Stand-by Current	All Inputs = V_{PD} = 2V		75		50	mA
t_{CP}	Chip Deselect to Stand-by Time		0		0		ns
t_R	Recovery Time		t_{RC}		t_{RC}		ns
CAPACITANCE T_A = 25°C, f = 1 MHz, (Note 3)							
C_{IN}	Input Capacitance	All Inputs V_{IN} = 0V		5		5	pF
C_{OUT}	Output Capacitance	V_O = 0V		10		10	pF

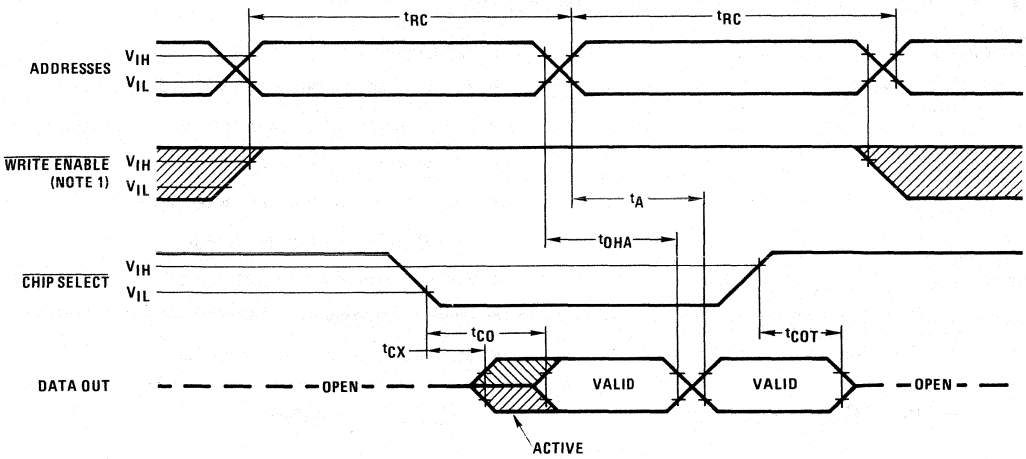
Note 3: This parameter is guaranteed by periodic testing.

Standby Waveforms

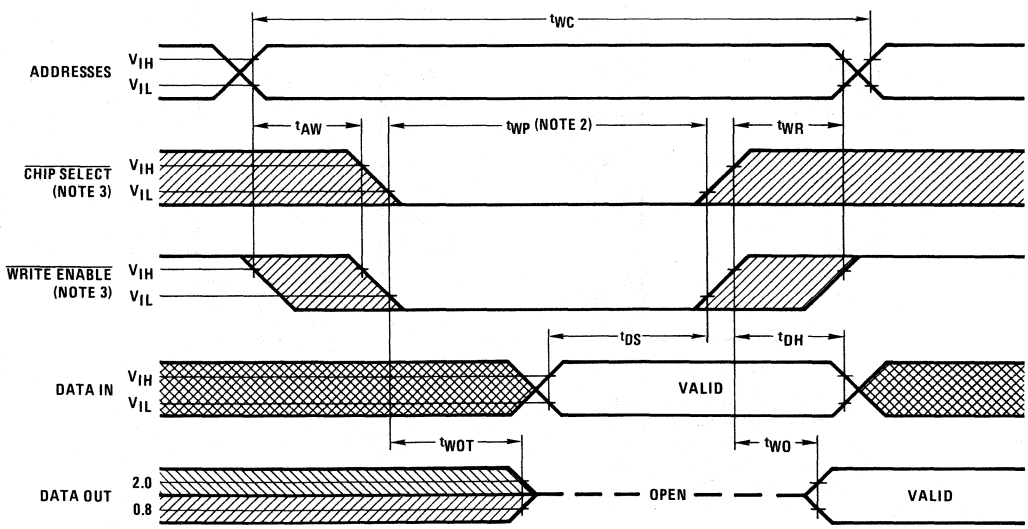


Switching Time Waveforms

Read Cycle



Write Cycle



Note 1: $\overline{WE}$ is high during a read cycle ($\overline{WE} \geq V_{IH(MIN)}$).

Note 2: t_{WP} defines the period when both $\overline{CS}$ and $\overline{WE}$ are low. t_{AW} is referenced to the later of $\overline{CS}$ or $\overline{WE}$ going low while t_{DS}, t_{DH} and t_{WR} are referenced to the earlier of $\overline{CS}$ or $\overline{WE}$ going high. t_{WOT} and t_{WO} are referenced to $\overline{WE}$ with $\overline{CS}$ low.

Note 3: Either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous write.

National Semiconductor

MM5257, MM5257L Family 4096-Bit (4096 × 1) Static RAMs

General Description

The MM5257 family of 4096-word by 1-bit static random access memories is fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

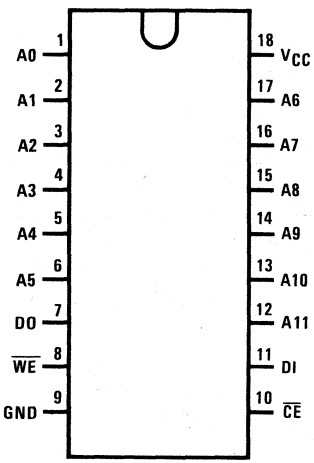
The output is held in a high impedance state during write to simplify common I/O applications.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—down to 200 ns access time
- TRI-STATE output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package

Connection Diagram

Dual-In-Line Package

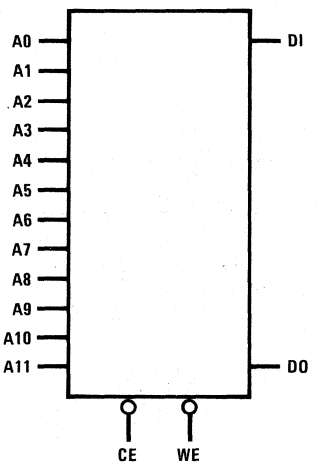


TOP VIEW

Order Number MM5257J, J-2, J-25, J-3, J-L, J-2L, J-25L or J-3L
See NS Package J18A

Order Number MM5257N, N-2, N-25, N-3, N-L, N-2L, N-25L, or N-3L
See NS Package N18A

Logic Symbol



Truth Table

$\overline{CE}$	$\overline{WE}$	DI	D_{OUT}	MODE
H	X	X	Hi-Z	Not Selected
L	L	H	Hi-Z	Write 1
L	L	L	Hi-Z	Write 0
L	H	X	D_{OUT}	Read

Functional Description

Two pins control the operation of the MM5257. Chip Enable ($\overline{CE}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CE}$ and $\overline{WE}$ controls.

READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CE}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CE}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

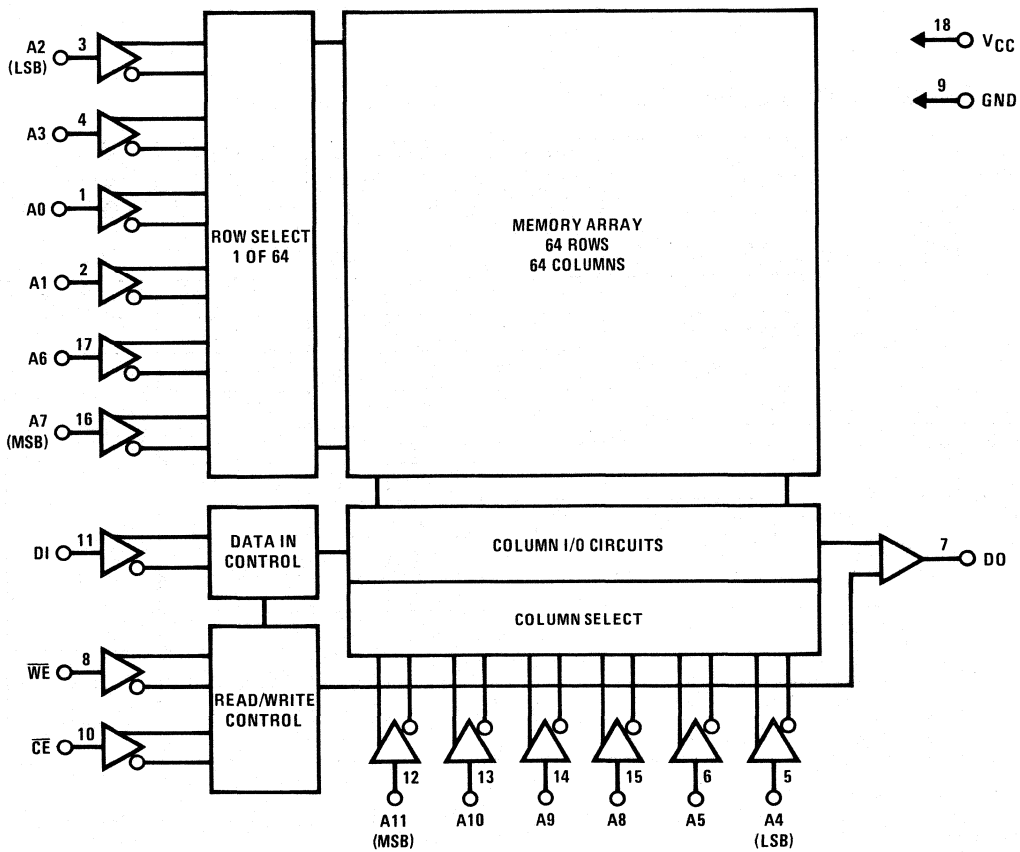
Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CE}$ has enabled the output buffer prior to data arrival. Chip Enable-to-output delay, t_{CO}, is the time required for $\overline{CE}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CE}$ continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CE}$ and $\overline{WE}$ are low. Minimum write-pulse width, t_{WP}, refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CE}$ continuously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CE}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CE}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Stand-by operation allows data to be maintained with approximately 50% less operating current. The 2 requirements to guarantee data retention are: a) the power supply voltage must meet the condition $V_{CC} \geq 1.5V$, and b) $\overline{CE}$ must be controlled; to disable the chip prior to reducing V_{CC}, to keep it disabled during the time V_{CC} is reduced, and to maintain the disabled state long enough after V_{CC} is increased to normal for the chip to recover. These requirements are shown by the stand-by waveforms and characteristics.

Block Diagram



Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS}	−0.3V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Short-Circuit Output Current	50 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MM5257 MM5257-2 MM5257-25 MM5257-3		MM5257-L MM5257-2L MM5257-25L MM5257-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		−0.5	0.8	−0.5	0.8	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -200\ \mu A$	2.4		2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.1$ mA		0.4		0.4	V
I_{LI}	Input Load Current	$V_{IN} = 0$ to 5.25V	−10	10	−10	10	μA
I_{LO}	Output Leakage Current	$V_O = 4V$ to 0.4V, $\overline{CE} = V_{IH}$	−10	10	−10	10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V, $T_A = 25°C$		80		55	mA
I_{CC}	Power Supply Current	All Inputs = 5.25V, $T_A = 0°C$		90		65	mA

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, (Note 2)

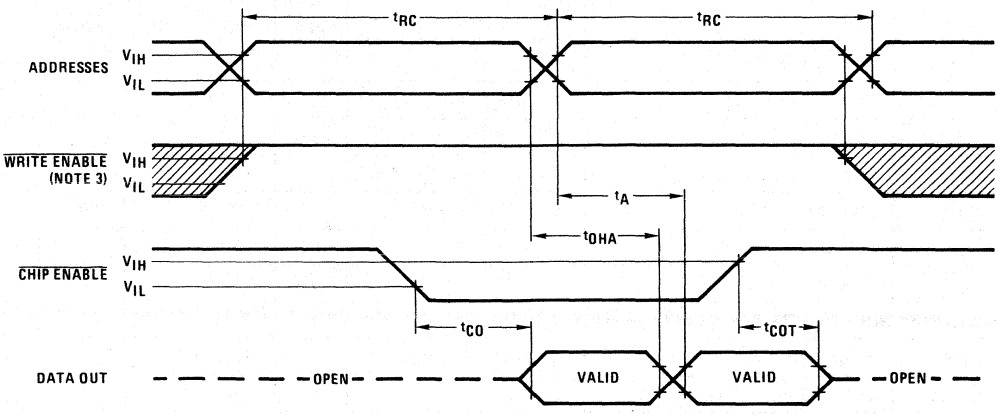
SYMBOL	PARAMETER	MM5257-2 MM5257-2L		MM5257-25 MM5257-25L		MM5257-3 MM5257-3L		MM5257 MM5257-L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE										
t_{RC}	Read Cycle Time ($\overline{WE} = V_{IH}$)		200		250		300		450	ns
t_A	Access Time		200		250		300		450	ns
t_{CO}	Chip Enable to Output Valid		80		100		150		200	ns
t_{COT}	Chip Enable to Output TRI-STATE	0	60	0	70	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	30		30		30		30		ns
WRITE CYCLE										
t_{WC}	Write Cycle Time		200		250		300		450	ns
t_{AW}	Address to Write Set-Up Time	20		20		20		20		ns
t_{WP}	Write Pulse Width	100		100		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DS}	Data Set-Up Time	85		85		120		175		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WOT}	Write Enable to Output TRI-STATE	0	80	0	80	0	100	0	120	ns
t_{WO}	Write Enable to Output Valid		80		80		100		120	ns

Note 1: Typical values at $T_A = 25°C$.

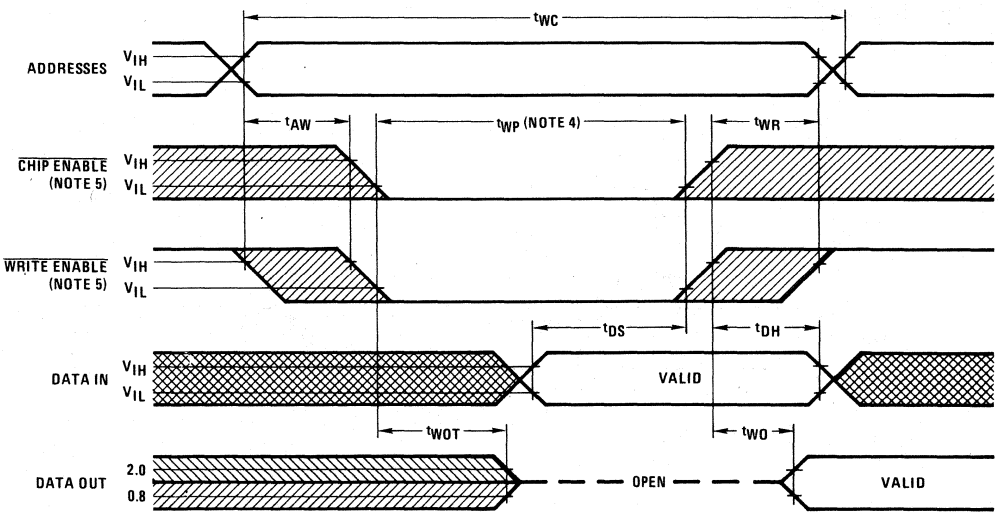
Note 2: All input transitions ≤ 10 ns. Timing referenced to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ for inputs, 0.8V and 2V for output. For test purposes, input levels should swing between 0V and 3V. Output load = 1 TTL gate and $C_L = 50$ pF.

Switching Time Waveforms

Read Cycle



Write Cycle



Note 3: $\overline{WE}$ is high during a read cycle ($\overline{WE} \geq V_{IH(MIN)}$).

Note 4: t_{WP} defines the period when both $\overline{CE}$ and $\overline{WE}$ are low. t_{AW} is referenced to the later of $\overline{CE}$ or $\overline{WE}$ going low while t_{DS}, t_{DH} and t_{WR} are referenced to the earlier of $\overline{CE}$ or $\overline{WE}$ going high. t_{WOT} and t_{WO} are referenced to $\overline{WE}$ with $\overline{CE}$ low.

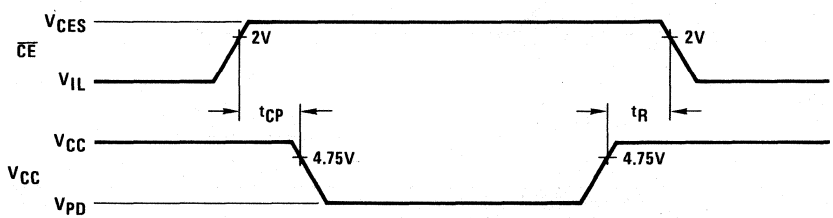
Note 5: Either $\overline{WE}$ or $\overline{CE}$ (or both) must be high during address transitions to prevent erroneous write.

Standby Characteristics $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	CONDITIONS	MM5257 MM5257-2 MM5257-25 MM5257-3		MM5257-L MM5257-2L MM5257-25L MM5257-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{PD}	V_{CC} in Stand-by		1.5		1.5		V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$2 \leq V_{PD} \leq V_{CC(MAX)}$	2.0		2.0		V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}		V_{PD}		V
I_{PD1}	Stand-by Current	All Inputs = V_{PD} = 1.5V		70		45	mA
I_{PD2}	Stand-by Current	All Inputs = V_{PD} = 2V		75		50	mA
t_{CP}	Chip Deselect to Stand-by Time		0		0		ns
t_R	Recovery Time		t_{RC}		t_{RC}		ns
CAPACITANCE $T_A = 25°C$, f = 1 MHz, (Note 6)							
C_{IN}	Input Capacitance	All Inputs V_{IN} = 0V		5		5	pF
C_{OUT}	Output Capacitance	V_O = 0V		10		10	pF

Note 6: This parameter is guaranteed by periodic testing.

Standby Waveforms



National Semiconductor

MOS RAMs

MM4270 4096-Bit (4096 × 1) TRI-SHARE™ Extended Temperature Range Dynamic RAM

general description

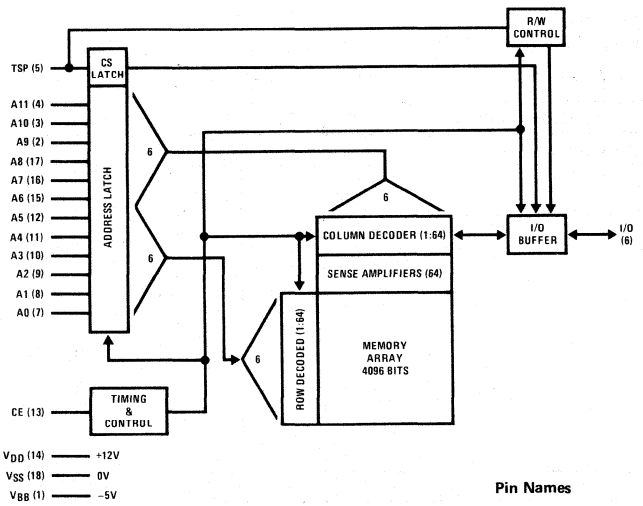
The MM4270 is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also performs a V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM4270 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed if the chip enable clock is pulsed.

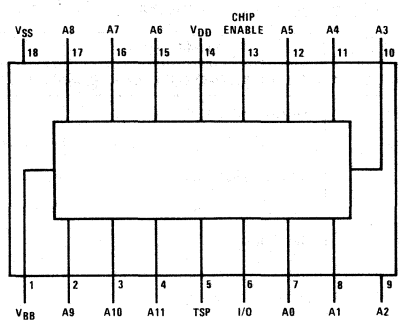
features

- 4096 x 1 bit organization
- Access time 270 ns maximum
- Cycle time 470 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs (except chip enable)
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4270D
See NS Package D18A

Order Number MM4270J
See NS Package J18A

Pin Names

A0—A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	$D_{IN}/\overline{D_{OUT}}$		

*Refresh Addess A0—A5

absolute maximum ratings

Operating Temperature Range	−55°C to +85°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

ac electrical characteristics

T_A = −55°C to +85°C, V_{DD} = 12V ±5%, V_{BB} (Note 2) = −5V ±10%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP(3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20	50	mA
$I_{DD\,AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 470 ns, t_{CE} = 300 ns		35	70	mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns, *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.2		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

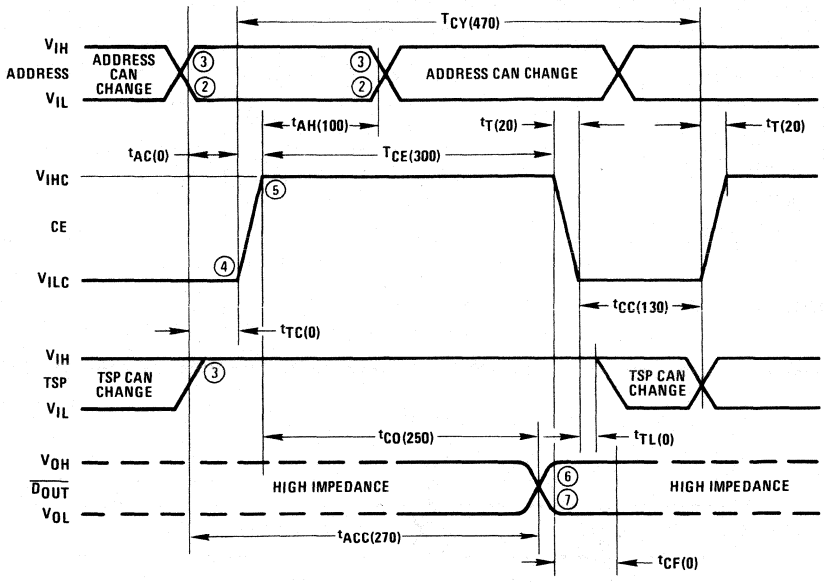
Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = −55°C to +85°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±10%

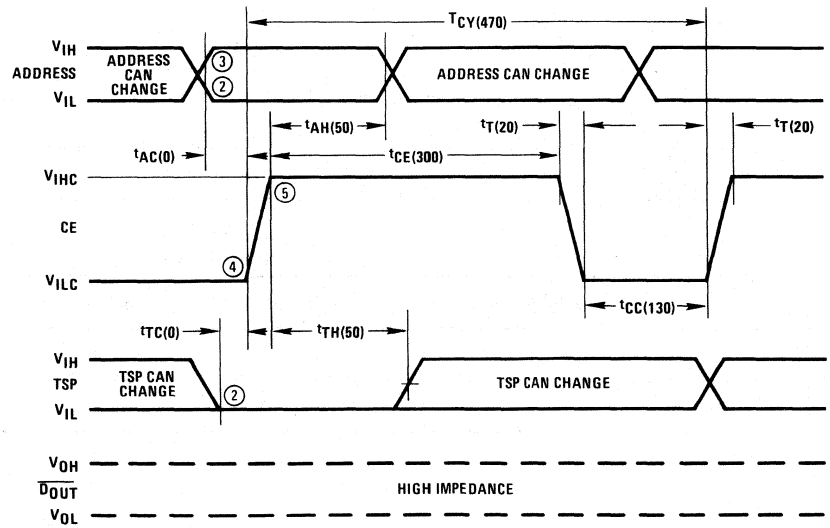
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				1	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		50			ns
READ CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time	t_T = 20 ns	300		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = One TTL Gate			250	ns
t_{ACC}	Address to Output Access	Ref 1 = 2.0V, Ref 0 = 0.8V			270	ns
t_{TL}	CE to TSP	$t_{ACC} = t_{AC} + t_{CO} + t_T$	0			ns

switching time waveforms

Read Cycle



Refresh Cycle ①



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\,MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 3: $V_{IH\,MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 4: V_{SS} + 2.0V is the reference level for measuring timing of CE.

Note 5: V_{DD} − 2V is the reference level for measuring timing of CE.

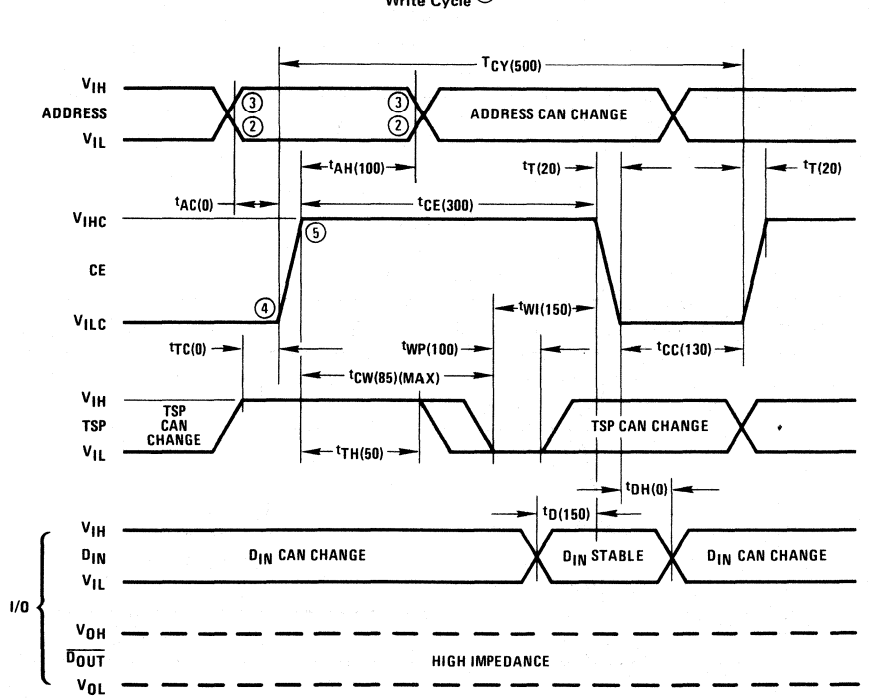
Note 6: V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT} for a high output.

Note 7: V_{SS} + 0.8V is the reference level for measuring timing of D_{OUT} for a low output.

ac electrical characteristics (Continued) $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{WI}	TSP to CE "OFF"		150			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			85	ns
t_D	D_{IN} to CE "OFF"		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns

switching time waveforms (Continued)



Note 1: If $t_{CW(MAX)}$ is greater than 85 ns, then memory operation is like Read/Modify/Write cycle.
Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.
Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.

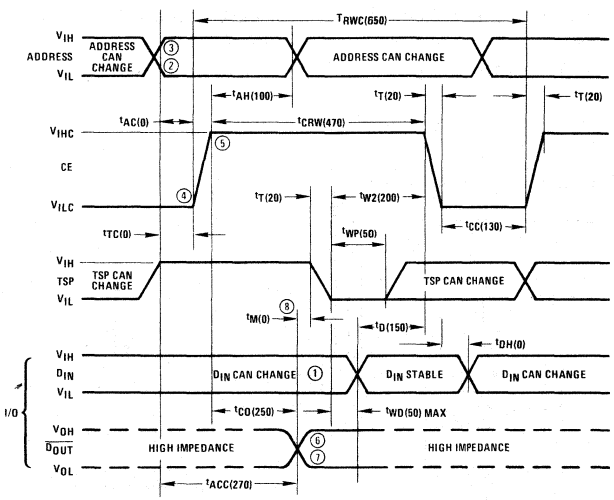
ac electrical characteristics (Continued) $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		650			ns
t_{CRW}	CE Width During RMW		480		3000	ns
t_{WC}	TSP to CE "ON"	t_T = 20 ns	0			ns
t_{W2}	TSP to CE "OFF"	C_{LOAD} = 50 pF, Load = One TTL Gate	200			ns
t_{WP}	TSP Pulse Width	Ref 1 = 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{ACC}	Access Time				270	ns
t_{WD}	TSP to Output High Impedance				50	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2	6	pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15	25	pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8	10	pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5	6	pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (Continued)

Read Modify Write Cycle



Note 1: If D_{IN} is forced prior to $\overline{D_{OUT}}$ becoming high impedance ($t_{WD(MAX)}$), then maximum ambient temperature should be derated by T_{OV}/T_{CYCLE} (35°C). Where T_{OV} is time between forcing D_{IN} and $\overline{D_{OUT}}$ becoming TRI-STATE.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 4: V_{SS} + 2.0V is the reference level for measuring timing of CE.

Note 5: V_{DD} − 2V is the reference level for measuring timing of CE.

Note 6: V_{SS} + 2.0V is the reference level for measuring timing of D_{OUT} for a high output.

Note 7: V_{SS} + 0.8V is the reference level for measuring timing of D_{OUT} for a low output.

Note 8: For minimum cycle, $t_M = 0$, for test purposes $t_M = 10$ ns.

National Semiconductor

MM5270 4096-Bit (4096 × 1) TRI-SHARE™ Dynamic RAM

general description

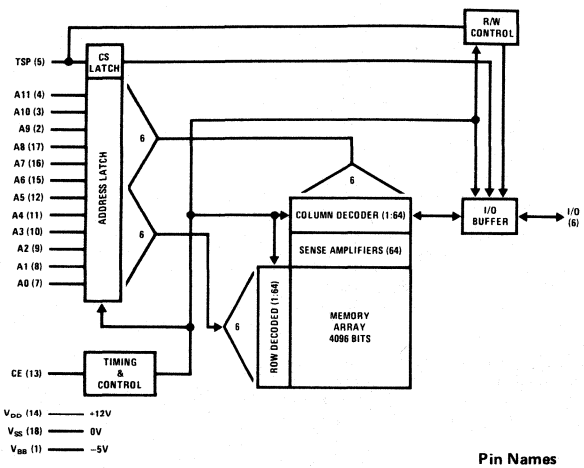
The MM5270 is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also performs a V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM5270 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed if the chip enable clock is pulsed.

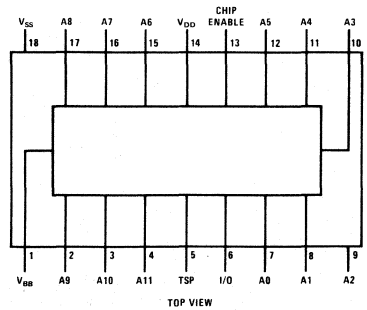
features

- 4096 x 1 bit organization
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs (except chip enable)
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



Order Number MM5270J
See NS Package J18A

Order Number MM5270N
See NS Package N18A

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	D_{IN}/D_{OUT}		

*Refresh Addess A0–A5

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
I_{LO}	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}		20	40	mA
$I_{DD\ AV1}$	Average V_{DD} Current	Cycle Time = 400 ns, t_{CE} = 230 ns		35	60	mA
$I_{DD\ AV2}$	Average V_{DD} Current	Cycle Time = 1000 ns, t_{CE} = 230 ns		15	30	mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns, (*Figure 4*)	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

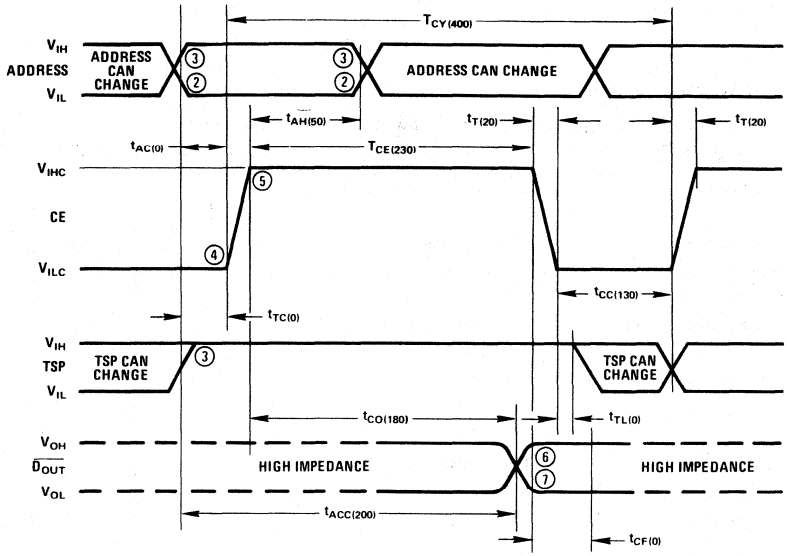
Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%

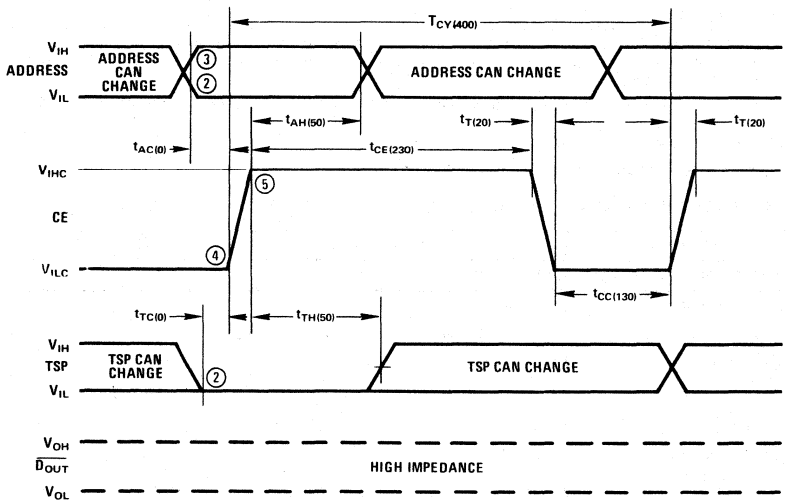
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		50			ns
READ CYCLE						
t_{CY}	Cycle Time	t_T = 20 ns C_{LOAD} = 50 pF, Load = One TTL Gate Ref 1 = 2.0V, Ref 0 = 0.8V $t_{ACC} = t_{AC} + t_{CO} + t_T$	400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{CO}	CE Output Delay				180	ns
t_{ACC}	Address to Output Access				200	ns
t_{TL}	CE to TSP		0			ns

switching time waveforms

Read Cycle



Refresh Cycle ①



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 4: V_{SS} + 2.0V is the reference level for measuring timing of CE.

Note 5: V_{DD} − 2V is the reference level for measuring timing of CE.

Note 6: V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT} for a high output.

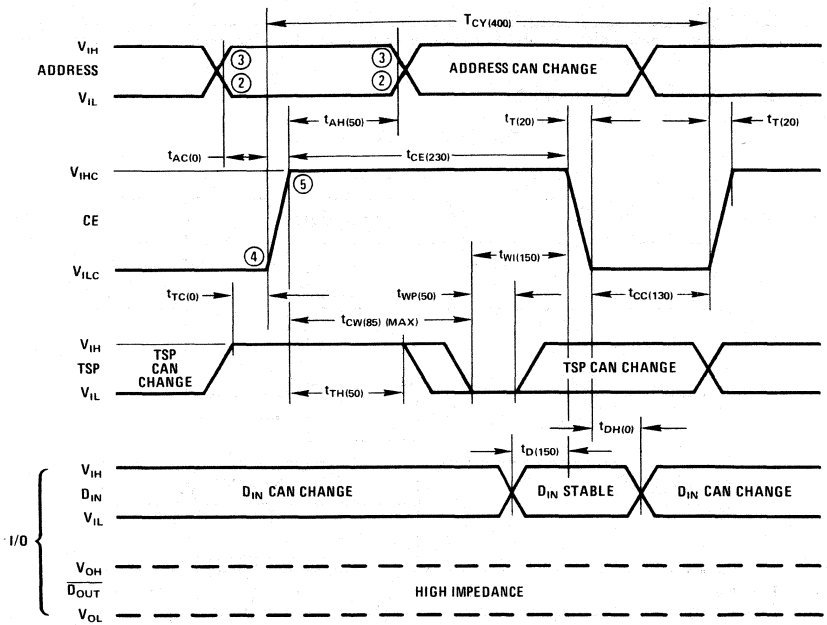
Note 7: V_{SS} + 0.8V is the reference level for measuring timing of D_{OUT} for a low output.

ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{WI}	TSP to CE "OFF"		150			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			85	ns
t_D	D_{IN} to CE "OFF"		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns

switching time waveforms (con't)

Write Cycle



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.

Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.

Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

Note 7: $V_{SS} + 0.8V$ is the reference level for measuring timing of D_{OUT} for a low output.

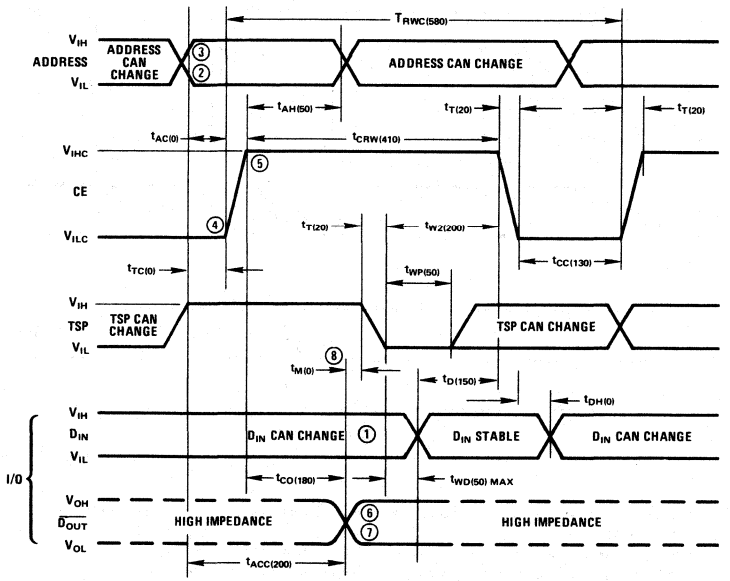
ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		580			ns
t_{CRW}	CE Width During RMW		410		3000	ns
t_{WC}	TSP to CE "ON"	$t_T = 20$ ns	0			ns
t_{W2}	TSP to CE "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	200			ns
t_{WP}	TSP Pulse Width	Ref 1 - 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{ACC}	Access Time				200	ns
t_{WD}	TSP to Output High Impedance				50	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (con't)

Read Modify Write Cycle



Note 1: If D_{IN} is forced prior to $\overline{D_{OUT}}$ becoming high impedance ($t_{WD(MAX)}$), then maximum ambient temperature should be derated by T_{OV}/T_{CYCLE} (35°C). Where T_{OV} is time between forcing D_{IN} and $\overline{D_{OUT}}$ becoming TRI-STATE.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.

Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.

Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

Note 7: $V_{SS} + 0.8V$ is the reference level for measuring timing of D_{OUT} for a low output.

Note 8: For minimum cycle, $t_M = 0$, for test purposes $t_M = 10$ ns.

National Semiconductor

MM5270-5 4096-Bit (4096 x 1) TRI-SHARE™ Dynamic RAM

general description

The MM5270-5 is a slower speed version of National's MM5270 dynamic RAM. Please refer to the MM5270 specification for pin configuration, block diagram and switching time waveforms.

features

- Access time—270 ns
- Cycle time—470 ns

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

Order Number MM5270J-5
See NS Package J18A

Order Number MM5270N-5
See NS Package N18A

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}		20	40	mA
$I_{DD\ AV1}$	Average V_{DD} Current	Cycle Time = 470 ns, t_{CE} = 300 ns		35	60	mA
$I_{DD\ AV2}$	Average V_{DD} Current	Cycle Time = 1000 ns t_{CE} = 300 ns		15	30	mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		80			ns
READ CYCLE						
t_{CY}	Cycle Time	$t_T = 20$ ns	470			ns
t_{CE}	CE "ON" Time	$C_{LOAD} = 50$ pF, Load = One TTL Gate	300		3000	ns
t_{CO}	CE Output Delay	Ref 1 = 2.0V, Ref 0 = 0.8V			250	ns
t_{ACC}	Address to Output Access	$t_{ACC} = t_{AC} + t_{CO} + t_T$			270	ns
t_{TL}	CE to TSP		0			ns
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{WI}	TSP to CE "OFF"		150			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			115	ns
t_D	D_{IN} to CE "OFF"		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		650			ns
t_{CRW}	CE Width During RMW		480		3000	ns
t_{WC}	TSP to CE "ON"	$t_T = 20$ ns	0			ns
t_{W2}	TSP to CE "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	200			ns
t_{WP}	TSP Pulse Width	Ref 1 = 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{ACC}	Access Time				270	ns
t_{WD}	TSP to Output High Impedance				250	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

MM5271 4096-Bit (4096 × 1) TRI-SHARE™ Fully TTL Compatible Dynamic RAM

general description

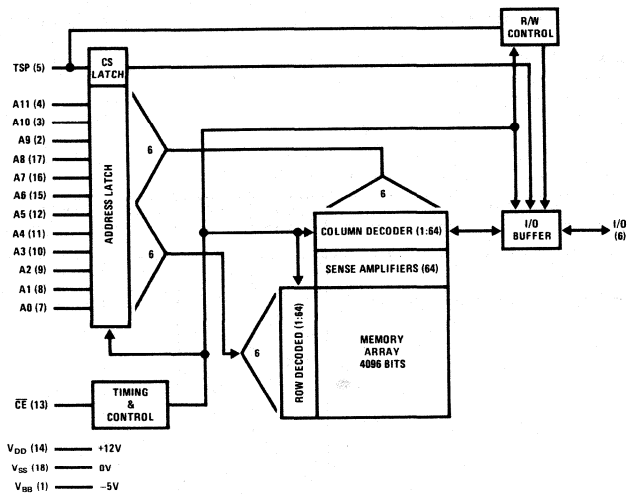
The MM5271 is a fully TTL compatible 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to house a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also controls the V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM5271 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed when the chip enable clock is pulsed.

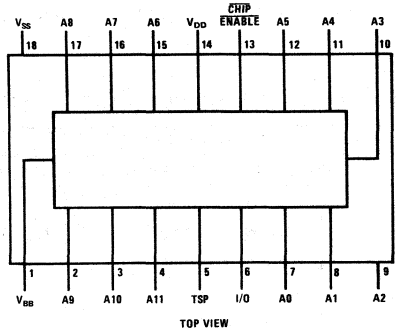
features

- 4096 x 1 bit organization
- Access time 250 ns maximum
- Cycle time 400 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



Order Number MM5271J
See NS Package J18A

Order Number MM5271N
See NS Package N18A

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
$\overline{CE}$	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	$D_{IN}/\overline{D_{OUT}}$		

*Refresh Addess A0–A5

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	$\overline{CE}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During $\overline{CE}$ "OFF"	$\overline{CE}$ = V_{IH}, (Note 4)		1	2	mA
I_{DD2}	V_{DD} Supply Current During $\overline{CE}$ "ON"	CE = V_{IL}		20	40	mA
$I_{DD\ AV1}$	Average V_{DD} Current	Cycle Time = 400 ns, t_{CE} = 240 ns		35	60	mA
$I_{DD\ AV2}$	Average V_{DD} Current	Cycle Time = 1000 ns, t_{CE} = 240 ns		15	30	mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 10 ns, *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

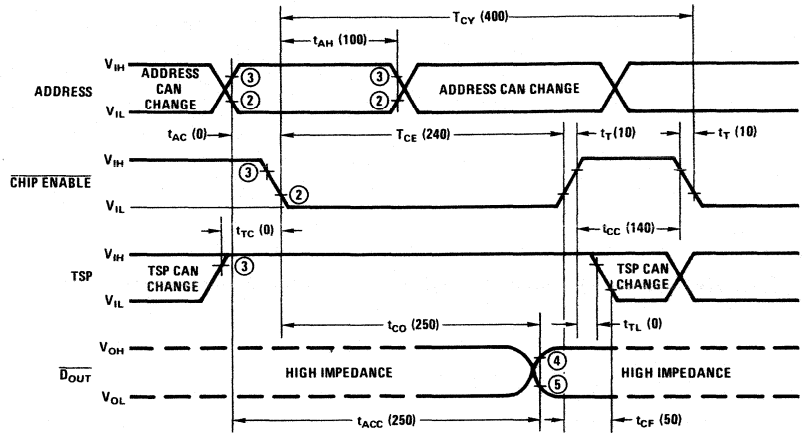
Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%

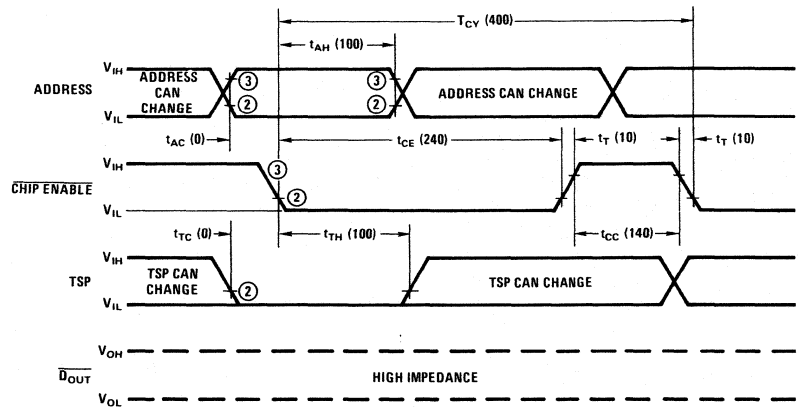
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to $\overline{CE}$ Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	$\overline{CE}$ "OFF" Time		140			ns
t_T	$\overline{CE}$ Transition Time				40	ns
t_{CF}	$\overline{CE}$ "OFF" to Output High Impedance State		50			ns
t_{TC}	TRI-SHARE Port to $\overline{CE}$ Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		100			ns
READ CYCLE						
t_{CY}	Cycle Time	t_T = 10 ns	400			ns
t_{CE}	$\overline{CE}$ "ON" Time	C_{LOAD} = 50 pF, Load = One TTL Gate	240		3000	ns
t_{CO}	$\overline{CE}$ Output Delay	Ref 1 = 2.0V, Ref 0 = 0.8V			250	ns
t_{ACC}	Address to Output Access	t_{ACC} = t_{AC} + t_{CO}			250	ns
t_{TL}	$\overline{CE}$ to TSP		0			ns

switching time waveforms

Read Cycle



Refresh Cycle (See Note 1)



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 4: V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT} for a high output.

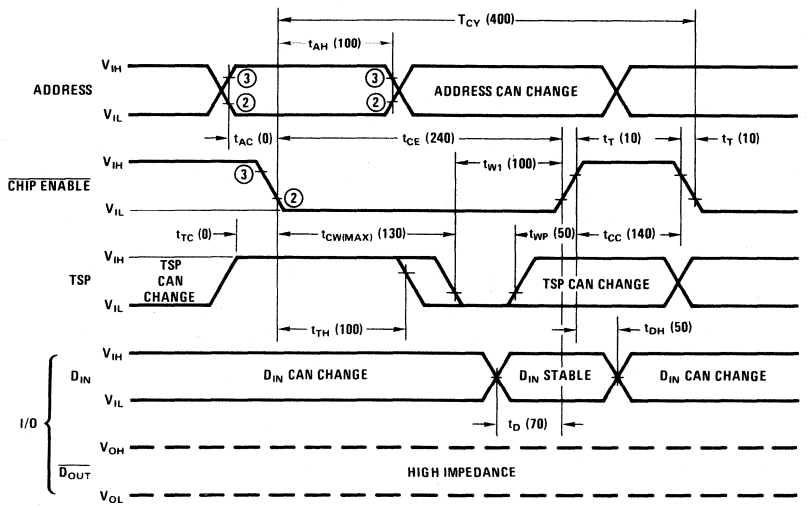
Note 5: V_{SS} + 0.8V is the reference level for measuring timing of D_{OUT} for a low output.

ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	$\overline{CE}$ "ON" Time		240		3000	ns
t_{WI}	TSP to CE "OFF"		100			ns
t_{CW}	$\overline{CE}$ to TSP	t_T = 10 ns, (Note 4)			130	ns
t_D	D_{IN} to $\overline{CE}$ "OFF"		70			ns
t_{DH}	D_{IN} Hold Time		50			ns
t_{WP}	TSP Pulse Width		50			ns

switching time waveforms (con't)

Write Cycle (See Note 4)



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 4: If $t_{CW(MAX)}$ is greater than 130 ns then memory operation is like Read/Modify/Write cycle.

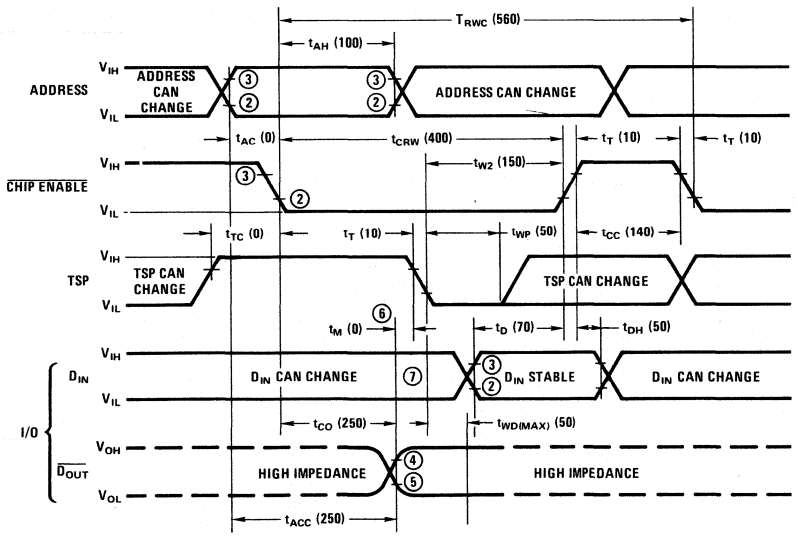
ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		560			ns
t_{CRW}	$\overline{CE}$ Width During RMW	$t_T = 10$ ns	400		3000	ns
t_{W2}	TSP to $\overline{CE}$ "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	150			ns
t_{WP}	TSP Pulse Width	Ref 1 - 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to $\overline{CE}$ "OFF"	$t_{ACC} = t_{AC} + t_{CO}$	70			ns
t_{DH}	D_{IN} Hold Time		50			ns
t_{CO}	$\overline{CE}$ to Output Delay				250	ns
t_{ACC}	Access Time				250	ns
t_{WD}	TSP to Output High Impedance				50	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	$\overline{CE}$ Capacitance	$V_{IN} = V_{SS}$		5		pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (con't)

Read Modify Write Cycle



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 4: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

Note 5: $V_{SS} + 0.8V$ is the reference level for measuring timing of D_{OUT} for a low output.

Note 6: For minimum cycle, $t_M = 0$, for test purposes $t_M = 10$ ns.

Note 7: If D_{IN} is forced prior to $\overline{D_{OUT}}$ becoming high impedance ($t_{WD(MAX)}$), then maximum ambient temperature should be derated by T_{OV}/T_{CYCLE} (35°C). Where T_{OV} is time between forcing D_{IN} and $\overline{D_{OUT}}$ becoming TRI-STATE.

National Semiconductor

MM4280 4096-Bit (4096 × 1) Extended Temperature Range Dynamic RAM

general description

National's MM4280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The MM4280 must be refreshed every 1 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh. Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

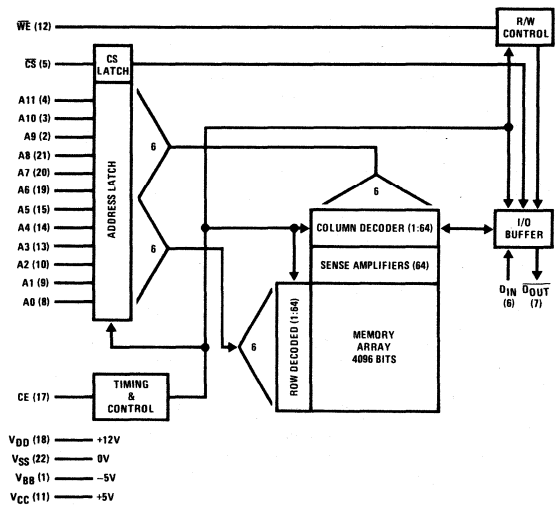
The MM4280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM4280 uses a single transistor cell to minimize the device area.

The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

features

- Extended temperature range: −55°C to +85°C
- Organization: 4096 x 1
- Access time 270 ns maximum
- Cycle time 470 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and outputs
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

block diagram

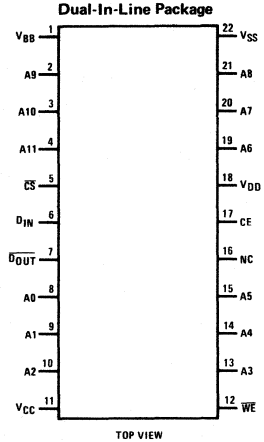


VDD (18) —— +12V
VSS (22) —— 0V
VBB (1) —— −5V
VCC (11) —— +5V

Memory Inverts From Data In to Data Out

connection diagram

Dual-In-Line Package

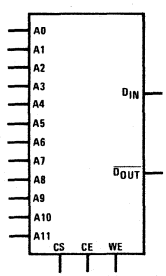


TOP VIEW

Order Number MM4280D
See NS Package D22B

Order Number MM4280J
See NS Package J22A

logic symbol



Pin Numbers

A0–A11	Address Inputs *	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

* Refresh Address A0–A5

absolute maximum ratings (Note 1)

Operating Temperature Range	−55°C to +85°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5V$)	−0.3V to +20V
Power Dissipation	1.25W

dc electrical characteristics

$T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, V_{BB} (Note 2) $= -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to 0.6V, (Note 4)		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20	50	mA
I_{DDAV1}	Average V_{DD} Current	Cycle Time = 470 ns, t_{CE} = 300 ns		35	70	mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH} (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.2		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA	0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS} and V_{BB} must be applied before and removed after other supply voltages.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

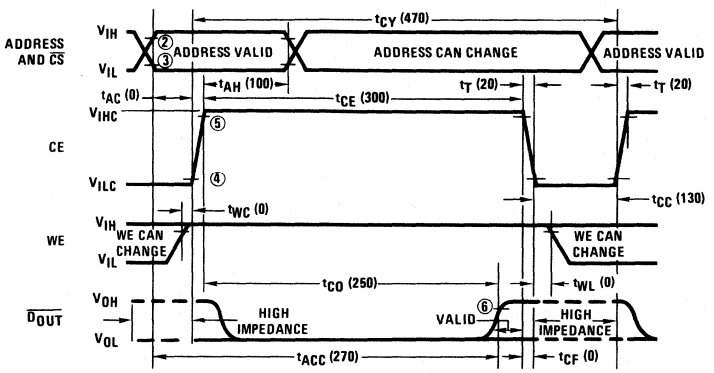
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				1	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2V,			250	ns
t_{ACC}	Address to Output Access	$t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$			270	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

ac electrical characteristics (Continued)

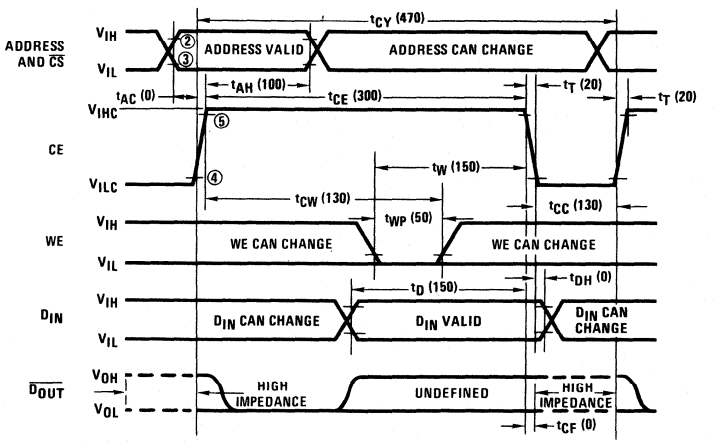
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	t_T = 20 ns	130			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

switching time waveforms

Read and Refresh Cycle ①



Write Cycle



Note 1: For refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$ and D_{IN}.
Note 3: V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$ and D_{IN}.
Note 4: V_{SS} + 2V is the reference level for measuring timing of CE.
Note 5: V_{DD} − 2V is the reference level for measuring timing of CE.
Note 6: V_{SS} + 2V is the reference level for measuring the timing of D_{OUT} for a high output.

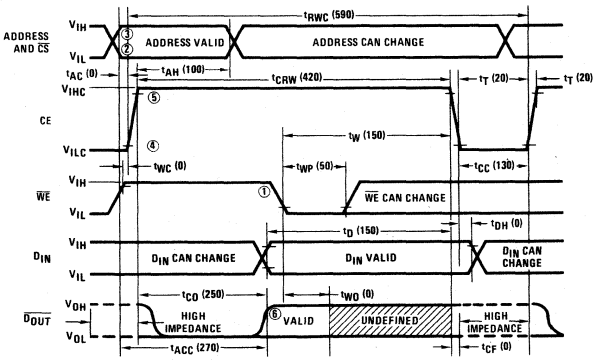
ac electrical characteristics (Continued) $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read/Modify/Write (RMW) Cycle Time		590			ns
t_{CRW}	CE Width During RMW		420		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			ns
t_{ACC}	Access Time				270	ns
CAPACITANCE (Note 1) $T_A = 25°C$						
C_{AD}	Address Capacitance, CS	$V_{IN} = V_{SS}$		2	6	pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15	25	pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5	10	pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4	6	pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (Continued)

Read Modify Write Cycle



Note 1: $\overline{WE}$ must be high until end of t_{CO}.

Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.

Note 3: V_{IH} min is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.

Note 4: $V_{SS} + 2V$ is the reference level for measuring timing of CE.

Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.

Note 6: $V_{SS} + 2V$ is the reference level for measuring the timing of $\overline{D_{OUT}}$ for a high output.

National Semiconductor

MM5280 4096-Bit (4096 × 1) Dynamic RAM

general description

National's MM5280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

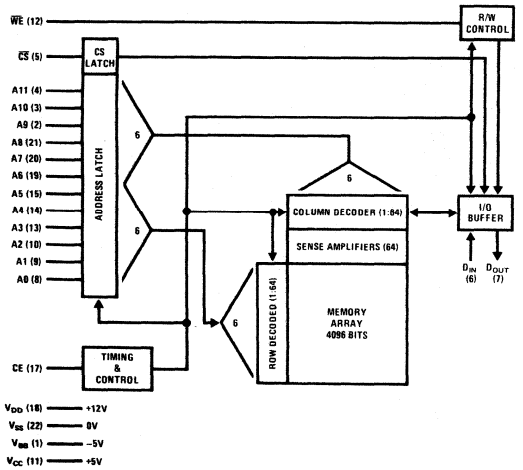
The MM5280 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

The MM5280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5280 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

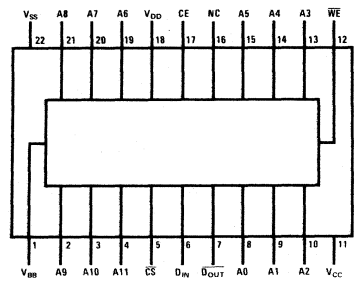
features

- Organization: 4096 x 1
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and output
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5280J
See NS Package J22A

Order Number MM5280N
See NS Package N22A

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh Address A0–A5

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.25W
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V		

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} (Note 2) = −5V ±10%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20	40	mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 230 ns		35	60	mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 1000 ns, t_{CE} = 230 ns		15	30	mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH},(Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$			180	ns
t_{ACC}	Address to Output Access				200	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

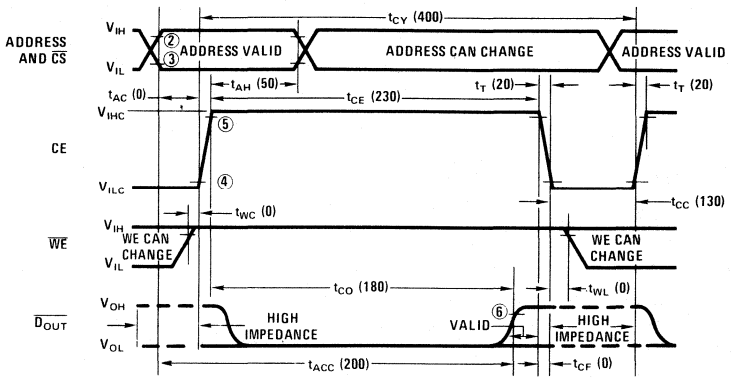
ac electrical characteristics (con't)

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

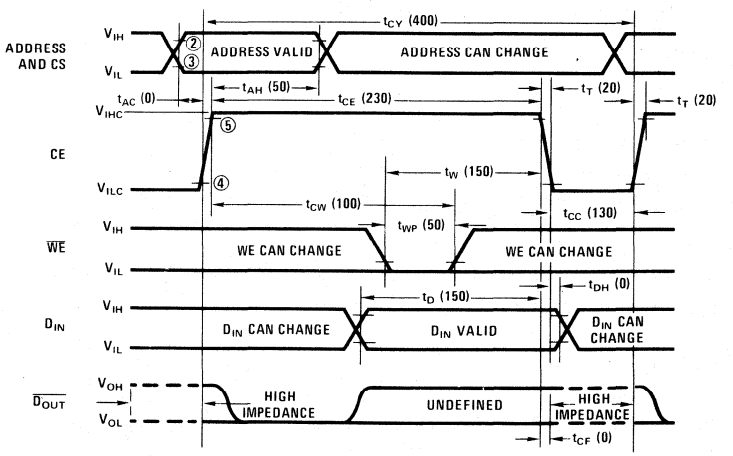
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	$t_T = 20$ ns	100			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

switching time waveforms

Read and Refresh Cycle ①



Write Cycle



Note 1: For refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$ and D_{IN}.
Note 3: V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$ and D_{IN}.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.
Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

ac electrical characteristics (con't)

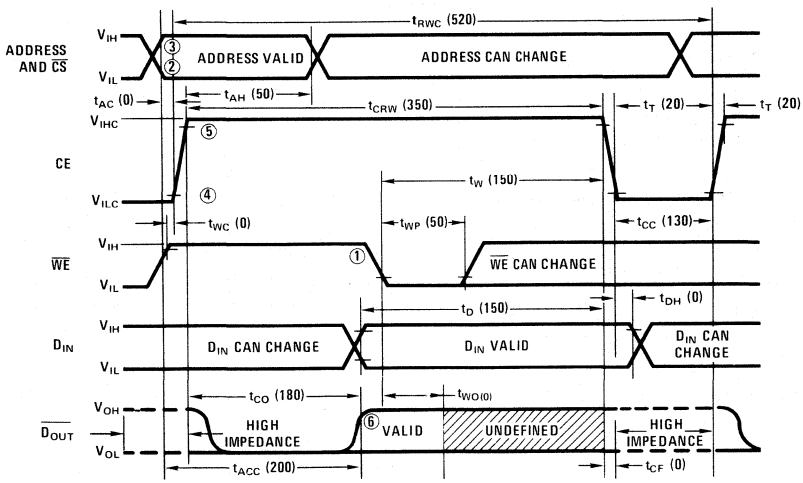
$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$	520			ns
t_{CRW}	CE Width During RMW		350		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				200	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (con't)

Read Modify Write Cycle



Note 1: $\overline{WE}$ must be high until end of t_{CO}.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 3: V_{IH} min is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.
Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of $\overline{D_{OUT}}$ for a high output.

National Semiconductor

MM5280-5 4096-Bit (4096 × 1) Dynamic RAM

general description

The MM5280-5 is a slower speed version of National's MM5280. Please refer to the MM5280 specification for pin configuration, block diagram and switching time waveforms.

features

- Access time—270 ns
- Cycle time—470 ns

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.25W

Order Number MM5280J-5
See NS Package J22A

Order Number MM5280N-5
See NS Package N22A

dc electrical characteristics

T_A = 0°C to +70°C V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20	40	mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 230 ns		35	60	mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 1000 ns, t_{CE} = 230 ns		15	30	mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time	$C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{CO}	CE Output Delay				250	ns
t_{ACC}	Address to Output Access				270	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
WRITE CYCLE						
t_{CY}	Cycle Time	$t_T = 20$ ns	470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$		130			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	590			ns
t_{CRW}	CE Width During RMW		420		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				270	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

National Semiconductor

MM5280-055 4096-Bit (4096 × 1) Dynamic RAM

General Description

National's MM5280-055 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications where low cost and large bit capacity are the prime criteria.

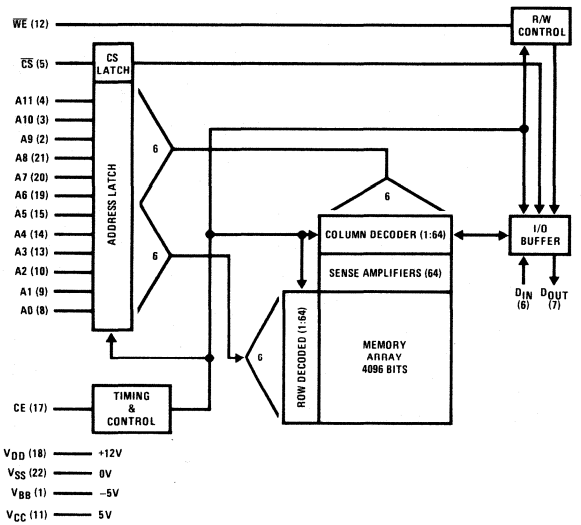
The MM5280-055 must be refreshed every 1 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

The MM5280-055 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits.

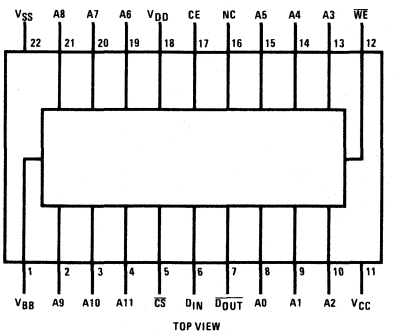
Features

- Organization: 4096 x 1
- Access time: 270 ns maximum
- Cycle time: 470 ns minimum
- Very low cost
- Industry standard pin configuration

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5280J-055
See NS Package J22A

Order Number MM5280N-055
See NS Package N22A

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh address A0–A5

Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +55°C	Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.25W
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V		

DC Electrical Characteristics

T_A = 0°C to +55°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} Max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} Max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE OFF	CE = −1V to 6V, (Note 4)		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE ON	CE = V_{IHC}, T_A = 25°C		20	40	mA
I_{DDAV1}	Average V_{DD} Current	T_A = 25°C, Cycle Time = 400 ns, t_{CE} = 230 ns		35	60	mA
I_{DDAV2}	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 230 ns		15	30	mA
I_{CC1}	V_{CC} Supply Current During CE OFF	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns, *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC} and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE ON, V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

AC Electrical Characteristics T_A = 0°C to +55°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±5%, V_{BB} = −5V ±5%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ-MODIFY-WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				1	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured from End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE OFF Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE OFF to Output High Impedance State		0			ns

AC Electrical Characteristics (Continued)

$T_A = 0°C$ to $+55°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

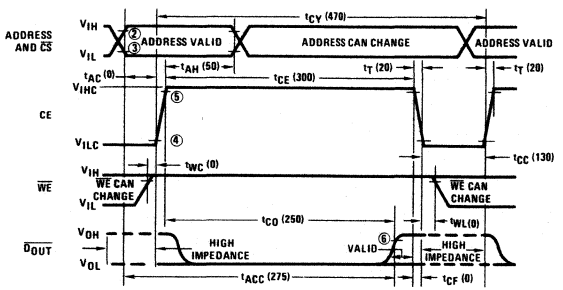
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ CYCLE						
t_{CY}	Cycle Time	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V	470			ns
t_{CE}	CE ON Time		300		3000	ns
t_{CO}	CE Output Delay				250	ns
t_{ACC}	Address to Output Access (Note 6)				270	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE ON		0			ns
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE ON Time		300		3000	ns
t_W	$\overline{WE}$ to CE OFF		150			ns
t_{CW}	CE to $\overline{WE}$	t_T = 20 ns	130			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
CAPACITANCE (Note 7), $T_A = 25°C$						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 6: $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$

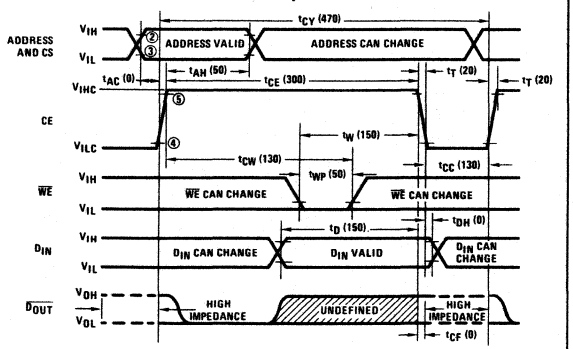
Note 7: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = |\Delta t/\Delta V$ with the current equal to a constant 20 mA.

Switching Time Waveforms

Read and Refresh Cycle ①



Write Cycle



Note 1: For refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$ and D_{IN}.

Note 3: V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$ and D_{IN}.

Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.

Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.

Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

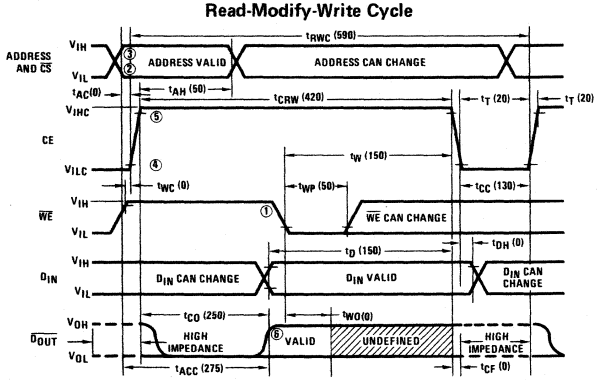
AC Electrical Characteristics (Continued)

$T_A = 0°C$ to $+55°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ-MODIFY-WRITE CYCLE						
t_{RWC}	Read-Modify-Write (RMW) Cycle Time	t_T = 20 ns, C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V	590			ns
t_{CRW}	CE Width During RMW		420		3000	ns
t_{WC}	$\overline{WE}$ to CE ON		0			ns
t_W	$\overline{WE}$ to CE OFF		150			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			ns
t_{ACC}	Access Time				270	ns

Switching Time Waveforms (Continued)

Read-Modify-Write Cycle



Note 1. $\overline{WE}$ must be high until end of t_{CO}.

Note 2: V_{IL} max is the reference level for measuring timing of the address $\overline{CS}$, D_{IN} and $\overline{WE}$.

Note 3: V_{IH} min is the reference level for measuring timing of the address, $\overline{CS}$ D_{IN} and $\overline{WE}$.

Note 4: V_{SS} + 2.0V is the reference level for measuring timing of CE.

Note 5: V_{DD} − 2V is the reference level for measuring timing of CE.

Note 6: V_{SS} + 2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$ for a high output.

National Semiconductor

MM5290 16,384-Bit (16,384 × 1) Dynamic RAM

General Description

The MM5290 is a 16,384 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5290 to be used in page mode operation.

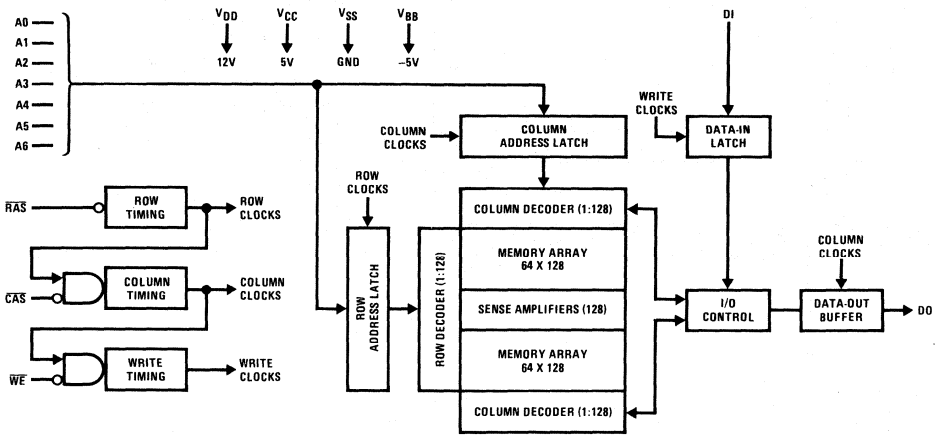
The MM5290 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including a $\overline{RAS}$-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology, developed by National, is used in the manufacture of the MM5290. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the MM5290.

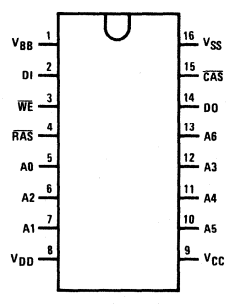
Features

- Access times: 150 ns, 200 ns, 250 ns
- Low power: 528 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$—noncritical timing
- Read, Write, Read-Modify-Write and $\overline{RAS}$-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5290J
See NS Package J16A

Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0—A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Voltage on Any Pin Relative to V_{BB}	−0.3V to +20V
Storage Temperature	−65°C to +150°C	($V_{SS} - V_{BB} \geq 4.5V$)	
Power Dissipation	1W	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Ambient Temperature	0	70	°C	
V_{DD}	Supply Voltages	10.8	13.2	V	2, 3
V_{CC}		4.5	5.5	V	2, 3
V_{SS}		0	0	V	2, 3
V_{BB}		−4.5	−5.5	V	2, 3
V_{IHC}	Input High Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.7	7.0	V	2
V_{IH}	Input High Voltage, A0–A6, DI	2.4	7.0	V	2
V_{IL}	Input Low Voltage, All Inputs	−1.0	0.8	V	2

DC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	**Operating Current**		40	mA	4
I_{CC1}	Average Power Supply Operating Current				5
I_{BB1}	($\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC} = t_{RC}$ MIN)		200	μA	
I_{DD2}	**Standby Current**		1.5	mA	
I_{CC2}	Power Supply Standby Current ($\overline{RAS} = V_{IHC}$,	−10	10	μA	
I_{BB2}	DO = High Impedance)		100	μA	
I_{DD3}	**Refresh Current**		30	mA	4
I_{CC3}	Average Power Supply Current, Refresh Mode	−10	10	μA	
I_{BB3}	($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IHC}$; $t_{RC} = t_{RC}$ MIN)		200	μA	
I_{DD4}	**Page Mode Current**		32	mA	4
I_{CC4}	Average Power Supply Current, Page Mode				5
I_{BB4}	($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling; t_{PC} = 225 ns)		200	μA	
$I_{I(L)}$	**Input Leakage**	−10	10	μA	
	Input Leakage Current, Any Input				
	($V_{BB} = -5V$, $0V \leq V_{IN} \leq 7V$, All Other				
	Pins not Under Test = 0V)				
$I_{O(L)}$	**Output Leakage**	−10	10	μA	
	Output Leakage Current (DO is Disabled,				
	$0V \leq V_{OUT} \leq 5.5V$)				
	Output Levels				
V_{OH}	Output High Voltage ($I_{OUT} = -5$ mA)	2.4		V	
V_{OL}	Output Low Voltage ($I_{OUT} = 4.2$ mA)		0.4	V	
CAPACITANCE					
C_I	Input Capacitance A0–A6, DI		5	pF	6
C_C	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		10	pF	6
C_O	Output Capacitance, DO		7	pF	6

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. When applying voltages to the device, V_{DD}, V_{CC} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 RAS cycles are adequate for this purpose.

Note 4: I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.

Note 5: I_{CC} depends on output load.

Note 6: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$. Capacitance is guaranteed by periodic testing.

AC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MM5290-2		MM5290-3		MM5290-4		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	375		375		410		ns	7, 8
t_{RWC}	Read-Write Cycle Time	375		375		515		ns	7, 8
t_{PC}	Page Mode Cycle Time	170		225		275		ns	
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250	ns	9, 11
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165	ns	10, 11
t_{OFF}	Output Buffer Turn-Off Delay	0	40	0	50	0	60	ns	12
t_T	Transition Time (Rise and Fall)	3	35	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	9
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	13, 14
t_{DH}	Data-In Hold Time	45		55		75		ns	13, 14
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	60		80		100		ns	
t_{REF}	Refresh Period		2		2		2	ms	
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	−20		−20		−20		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		125		ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		200		ns	15

Note 7: The specifications for $t_{RC(MIN)}$ and $t_{RWC(MIN)}$ are used only to indicate cycle time at which proper operation over the full temperature range is guaranteed.

Note 8: Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Timing measurements are made between $V_{IHC(MIN)}$ or $V_{IH(MIN)}$ and $V_{IL(MAX)}$, and assume $t_T = 5$ ns.

Note 9: Assumes row-limited access, i.e., $t_{RCD} \leq t_{RCD(MAX)}$. If this condition is not satisfied, then note 10 applies.

Note 10: Assumes column-limited access, i.e., $t_{RCD} > t_{RCD(MAX)}$.

Note 11: Equivalent load is 2 standard TTL inputs plus 100 pF.

Note 12: $\overline{CAS}$ going high disables the Data Output. t_{OFF} is the delay to the high impedance state.

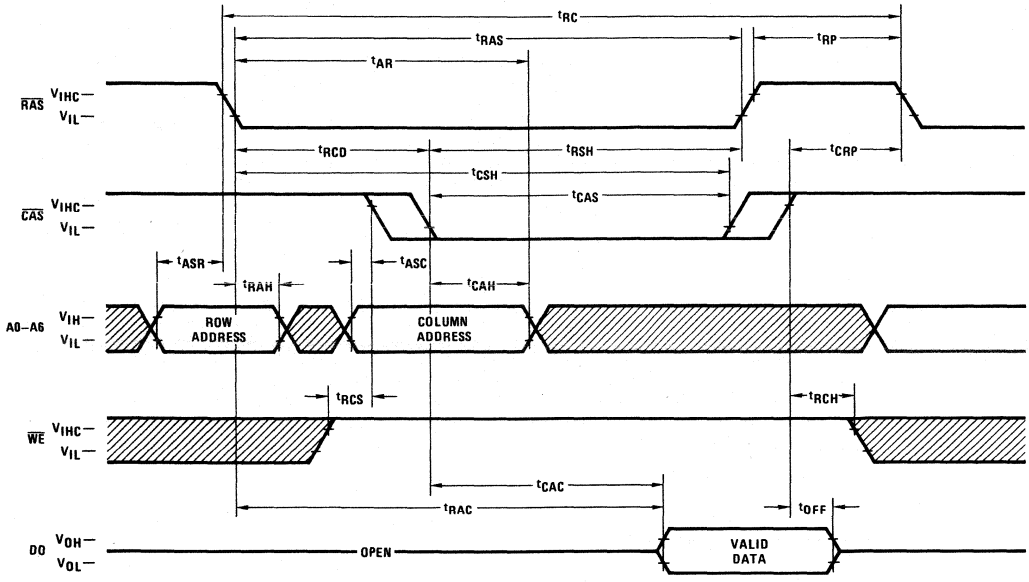
Note 13: These parameters are referenced to the negative edge of $\overline{CAS}$ in an early-write cycle and to the negative edge of $\overline{WE}$ in a Read-Modify-Write cycle. (See Note 12, below).

Note 14: If $t_{WCS} \geq t_{WCS(MIN)}$, the Data Output is guaranteed to remain in the high impedance state for the duration of the cycle. This is the "early-write" cycle.

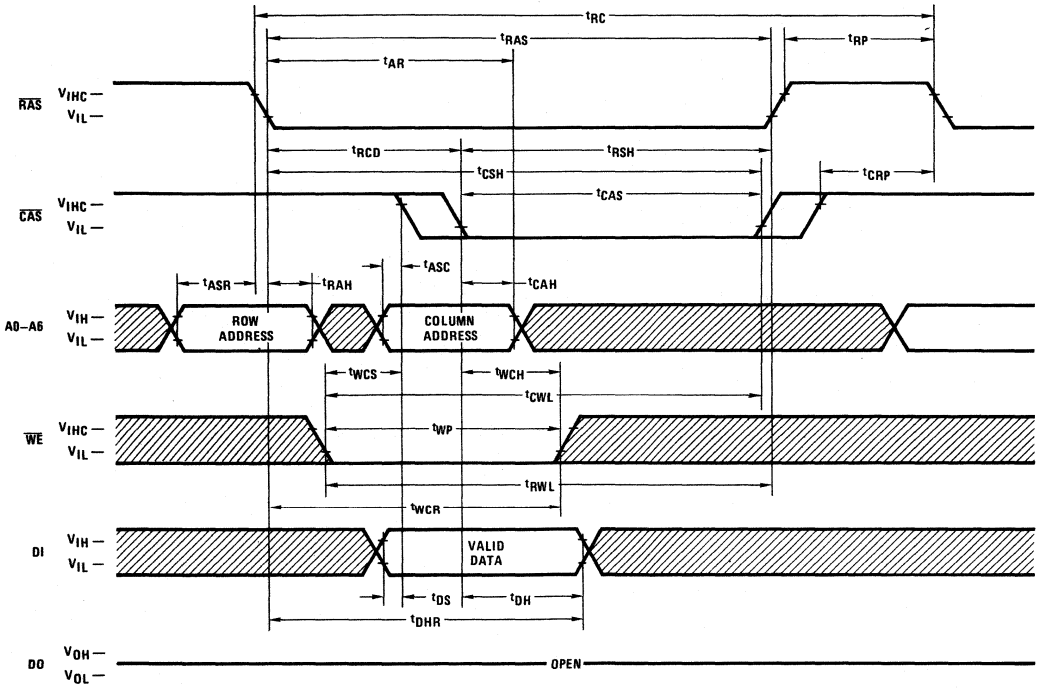
Note 15: If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$, the Data Output will contain the original data in the selected cell. This is the Read-Modify-Write cycle. If either of these conditions is not satisfied, the output will be indeterminate unless the early-write condition of Note 12 is met.

Switching Time Waveforms

Read Cycle

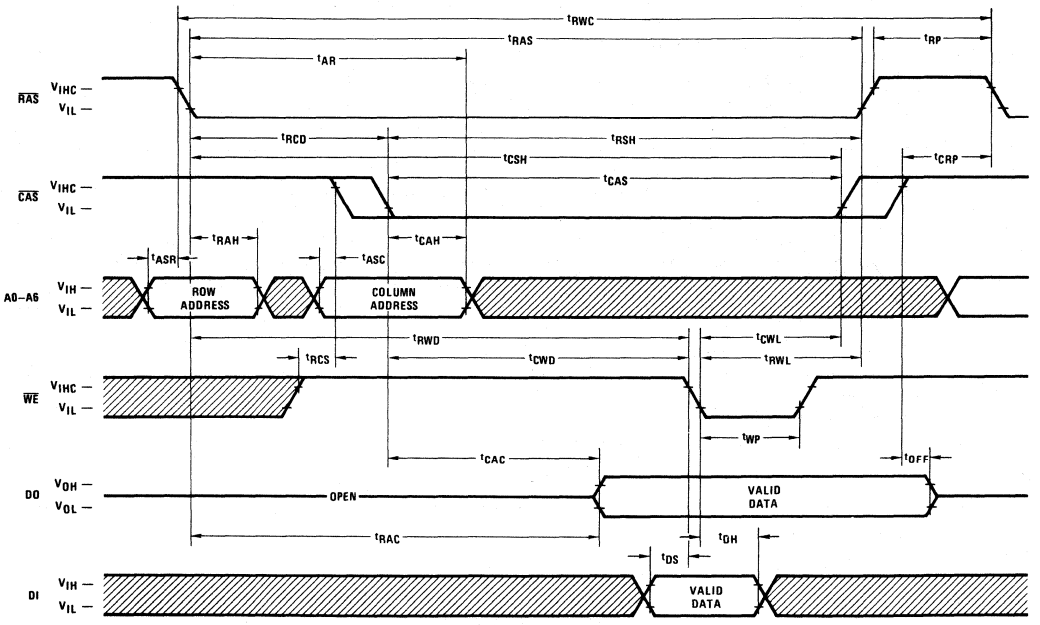


Write Cycle (Early Write)

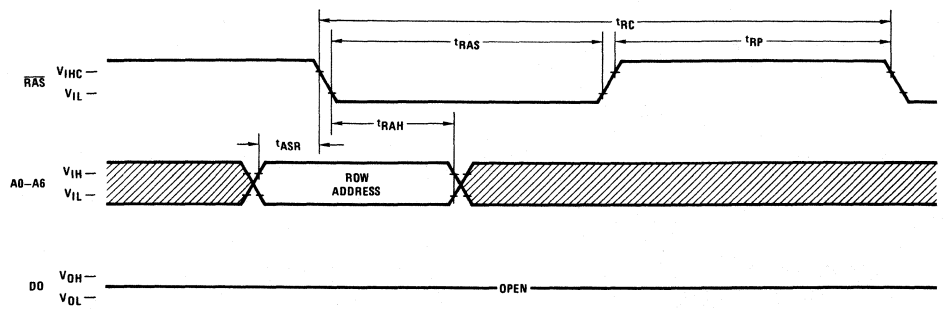


Switching Time Waveforms (Continued)

Read-Write Cycle, Read-Modify-Write Cycle



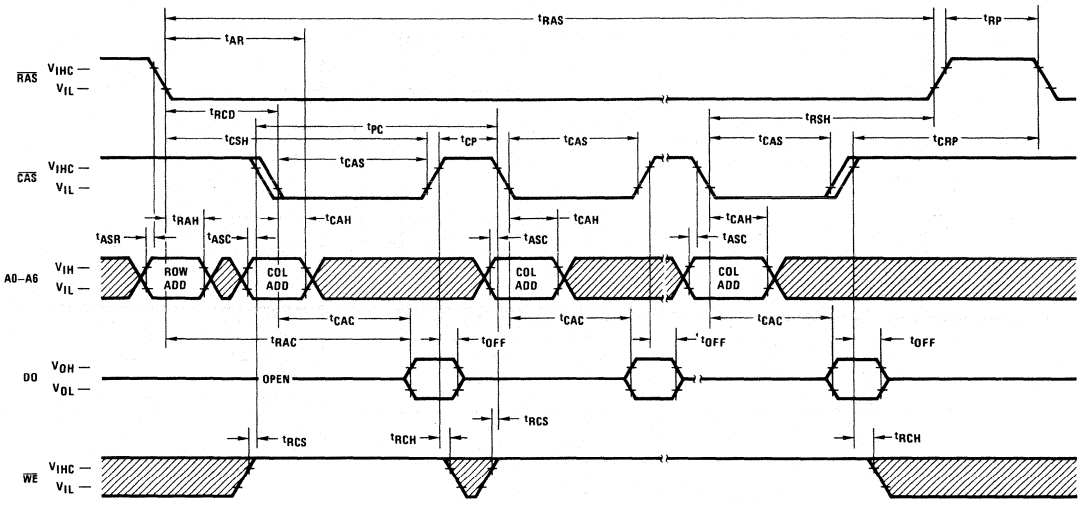
RAS-Only Refresh Cycle



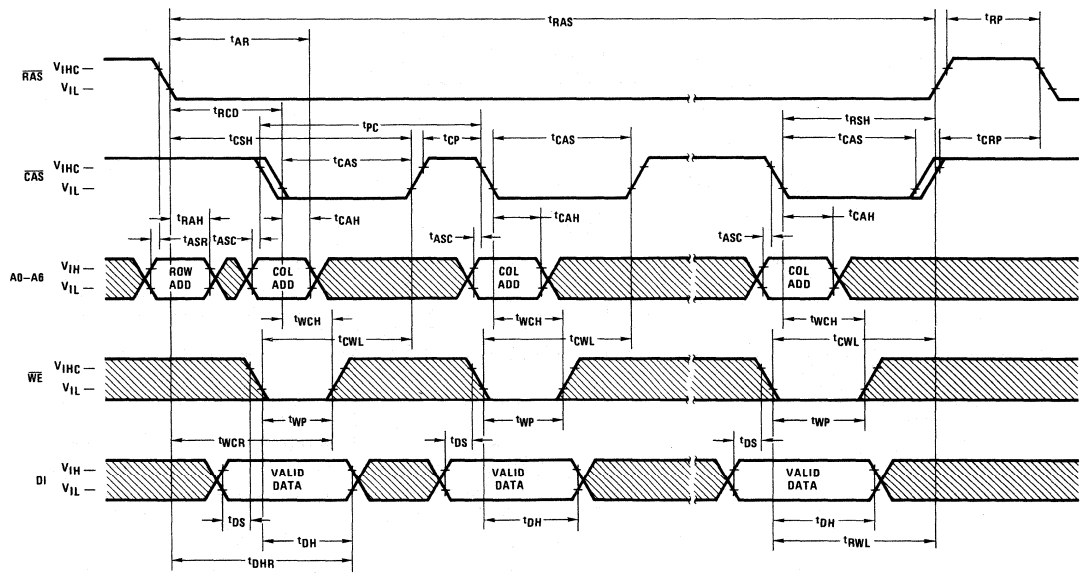
Note. $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = don't care

Switching Time Waveforms (Continued)

Page Mode Read Cycle



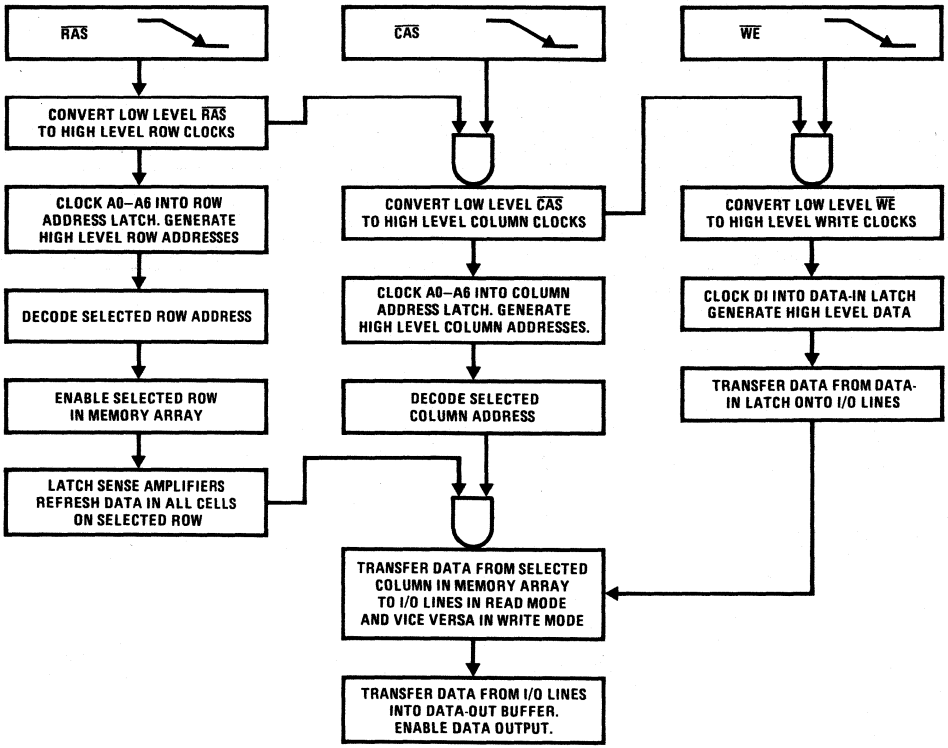
Page Mode Write Cycle



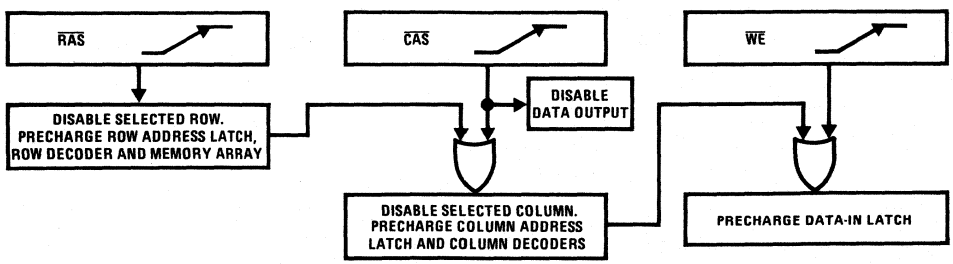
Note. Standard part not tested for page mode

Timing Flow Chart

ACTIVE



PRECHARGE



Section 2

Bipolar RAMs

2

Bipolar RAMs offer the best solution to problems requiring high speed read-write memory. National's product line includes the devices in this section to complement our bipolar microprocessor and logic lines.

DM54LS189/DM74LS189 64-Bit (16 × 4) TRI-STATE® RAM

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip enable input to simplify decoding required to achieve the desired system organization. This device is implemented with low power Schottky technology resulting in one-fifth power while retaining the speed of standard TTL.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM54LS289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip enable input and the read/write input are low. While the read/write input is low, the outputs are in the high impedance state. When a number of the DM54LS189 outputs are bus-connected, this high impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

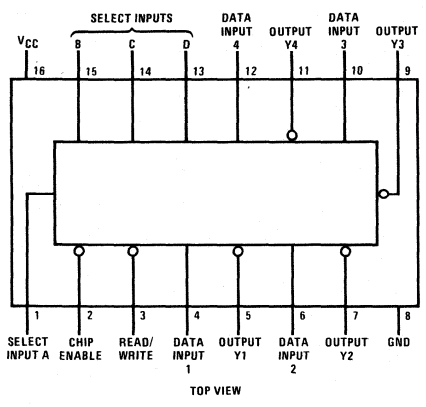
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip enable is low. When the chip enable input is high, the outputs will be in the high impedance state.

features

- Schottky-clamped for high speed applications
  - Access from chip enable input—40 ns typ
  - Access from address inputs—60 ns typ
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- Low power—75 mW typ
- DM54LS189 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip enable input simplifies system decoding

connection diagram

Dual-In-Line Package



TOP VIEW

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	Hz
Read	L	H	Stored Data
Inhibit	H	X	Hz

H = high level
L = low level
X = don't care

Order Number DM54LS189J or DM74LS189J
See NS Package J16A
Order Number DM74LS189N
See NS Package N16A

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

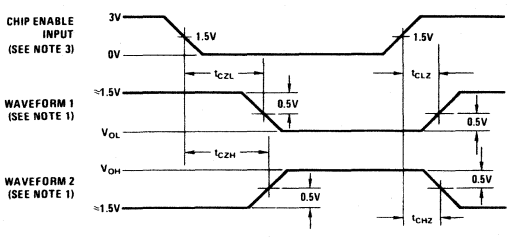
	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54LS189	4.5	5.5	V
DM74LS189	4.75	5.25	V
Temperature (T_A)			
DM54LS189	−55	+125	°C
DM74LS189	0	+70	°C

electrical characteristics

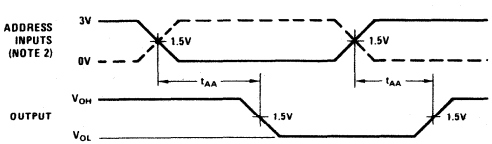
Over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA		2.4	3.4		V
					2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 4 mA	DM54LS189			0.45	V
			I_{OL} = 8 mA	DM74LS189			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7					10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V					1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V					−100	μA
I_{OS}	Short-Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V			−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max				15	29	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V					40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V					40	μA

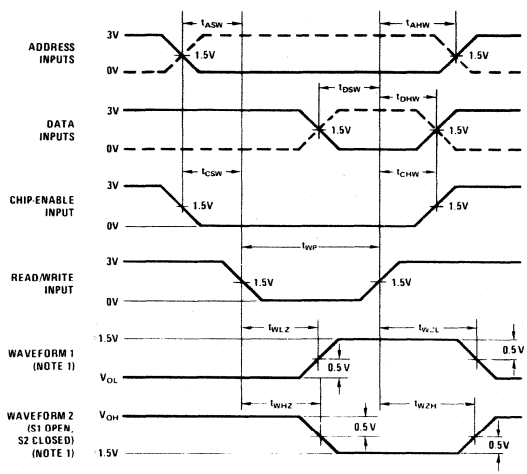
switching time waveforms



Enable and Disable Time From Chip Enable



Access Time From Address Inputs



Write Cycle

FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note 2. When measuring delay times from address inputs, the chip enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{OUT} \approx 50\Omega$.

switching characteristics

Over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			CONDITIONS	DM54LS189			DM74LS189			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{AA}	Access Times From Address		C_L = 30 pF, R_L = 1 kΩ,		60	100		60	80	ns
t_{CZH}	Output Enable Time to High Level	Access Times From Chip Enable			40	80		40	60	ns
t_{CZL}	Output Enable Time to Low Level				40	80		40	60	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times From Read/Write			60	100		60	80	ns
t_{WZL}	Output Enable Time to Low Level				60	100		60	80	ns
t_{CHZ}	Output Disable Time From High Level	Disable Times From Chip Enable	C_L = 5 pF, R_L = 1 kΩ,		40	80		40	60	ns
t_{CLZ}	Output Disable Time From Low Level				40	80		40	60	ns
t_{WHZ}	Output Disable Time From High Level	Disable Times From Read/Write			40			40		ns
t_{WLZ}	Output Disable Time From Low Level				40			40		
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			100			80			ns
t_{ASW}	Set-Up Time	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		100			80			
t_{CSW}		Chip Enable to Read/Write		0			0			
t_{AHW}	Hold Time	Address From Read/Write		50			50			ns
t_{DHW}		Data From Read/Write		0			0			
t_{CHW}		Chip Enable From Read/Write		0			0			

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54LS189 and across the 0°C to +70°C range for the DM74LS189. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded, and the outputs open.

National Semiconductor

DM54S189/DM74S189 64-Bit (16 × 4) TRI-STATE® RAM

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output. Systems utilizing data-bus lines with a defined pull-up impedance can employ the open-collector DM54S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM54S189 outputs are bus-connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs will be in the high-impedance state.

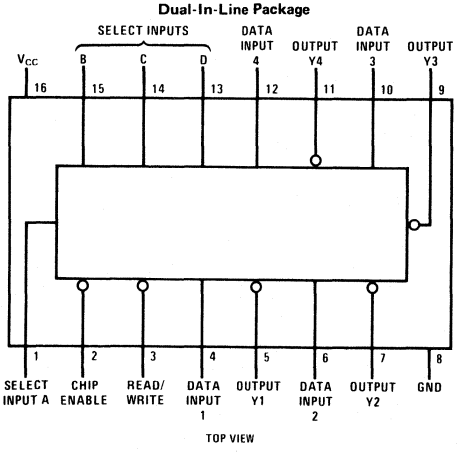
The fast access time of the DM54S189 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 ns. The high capacitive-drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM54S189 outputs being at a high impedance during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

features

- Schottky-clamped for high-speed applications:
  - access from chip-enable input 12 ns typ
  - access from address inputs 25 ns typ
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- DM54S289, DM74S289 are functionally equivalent, have open-collector outputs, and are compatible with Intel 3101A in most applications
- DM54S189 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip-enable input simplifies system decoding

connection diagram

Dual-In-Line Package



TOP VIEW

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = High Level
L = Low Level
X = Don't Care

Order Number DM54S189J or DM74S189J
See NS Package J16A
Order Number DM74S189N
See NS Package N16A

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S189	4.5	5.5	V
DM74S189	4.75	5.25	V
Temperature (T_A)			
DM54S189	−55	+125	°C
DM74S189	0	+70	°C

electrical characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM54S189			0.5	V
			DM74S189			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				50	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V				−50	μA

switching characteristics

over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			CONDITIONS	LIMITS DM54S189 MIN	LIMITS DM54S189 TYP(1)	LIMITS DM54S189 MAX	LIMITS DM74S189 MIN	LIMITS DM74S189 TYP(1)	LIMITS DM74S189 MAX	UNITS
t_{AA}	Access Times From Address		C_L = 30 pF, R_L = 280Ω, *(Figure 1)*		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times From Chip Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times From Read/Write			22	40		22	35	ns
t_{WZL}	Output Enable Time to Low Level				22	40		22	35	ns

switching characteristics (con't)

PARAMETER			CONDITIONS	LIMITS						UNITS
				DM54S189			DM74S189			
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{CHZ}	Output Disable Time From High Level	Disable Times From Chip Enable	C_L = 5 pF, R_L = 280Ω *(Figure 1)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time From Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time From High Level	Disable Times From Read/Write			12			12		ns
t_{WLZ}	Output Disable Time From Low Level				12			12		ns
t_{WP}	Width of Write-Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			
t_{CSW}		Chip-Enable to Read/Write		0			0			
t_{AHW}	Hold Time *(Figure 1)*	Address From Read/Write		0			0			ns
t_{DHW}		Data From Read/Write		0			0			
t_{CHW}		Chip-Enable From Read/Write		0			0			

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

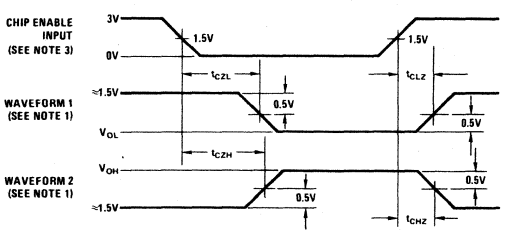
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189 and across the 0°C to +70°C range for the DM74S189. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

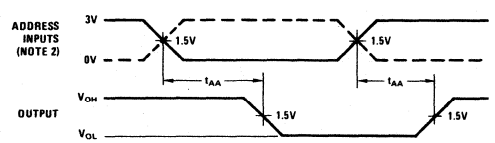
Note 4. Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded, and the outputs open.

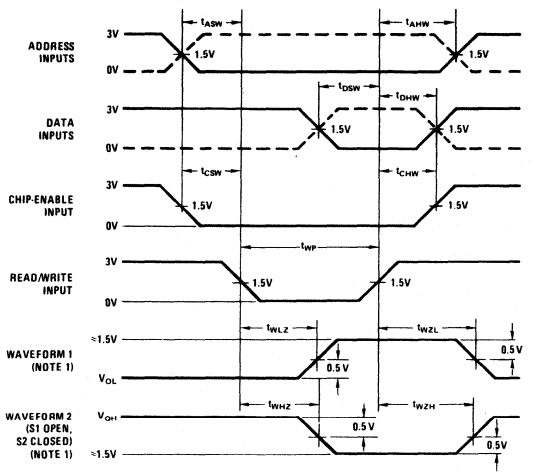
switching time waveforms



Enable and Disable Time From Chip Enable



Access Time From Address Inputs



Write Cycle

FIGURE 1

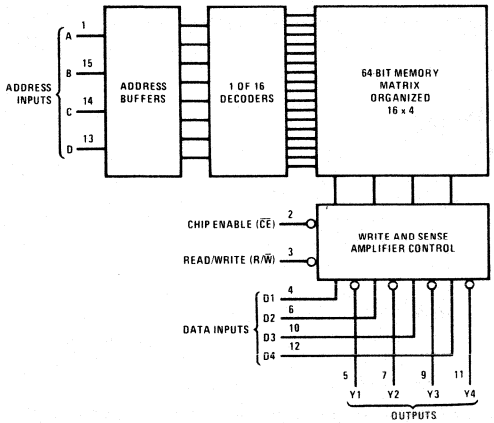
Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note 2. When measuring delay times from address inputs, the chip enable input is low and the read/write input is high.

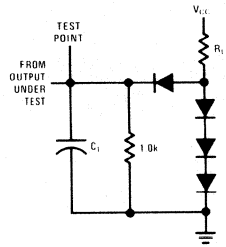
Note 3: When measuring delay times from chip enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{OUT} \approx 50\Omega$.

block diagram



ac test circuit



C_1 includes probe and jig capacitance.
All diodes are 1N3064.

National Semiconductor

DM54S200/DM74S200 256-Bit (256 × 1) TRI-STATE® RAM

general description

The DM54S200/DM74S200 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output.

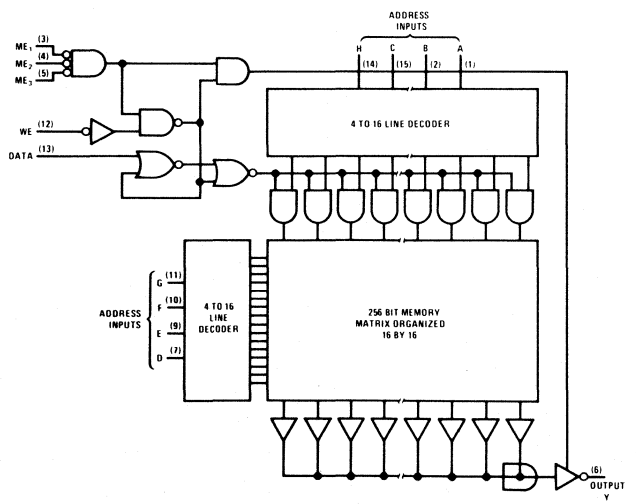
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

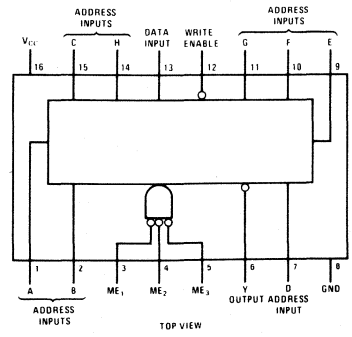
features

- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 20 ns typ
  - Access from address inputs 31 ns typ
  - Power dissipation 1.7 mW/bit typ
- TRI-STATE output for driving bus-organized systems and/or highly capacitive loads
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

block and connection diagrams



Dual-In-Line Package



Order Number DM54S200J
or DM74S200J
See NS Package J16A

Order Number DM74S200N
See NS Package N16A

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S200	4.5	5.5	V
DM74S200	4.75	5.25	V
Temperature (T_A)			
DM54S200	−55	+125	°C
DM74S200	0	+70	°C

recommended operating conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Output Current (I_{OH})					
DM54S200				−2.0	mA
DM74S200				−5.2	mA
Low Level Output Current (I_{OL})				16	mA
Width of Write Enable Pulse (t_W)					
DM54S200		50			ns
DM74S200		40			ns
Setup Time (t_{SETUP})					
Address to Write Enable		0			ns
Data to Write Enable		0			ns
Memory Enable to Write Enable		0			ns
Hold Time (t_{HOLD})					
Address from Write Enable		10			ns
Data from Write Enable		10			ns
Memory Enable from Write Enable		0			ns

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})			2.0			V
Low Level Input Voltage (V_{IL})					0.8	V
Input Clamp Voltage (V_I)	V_{CC} = Min, I_I = −18 mA				−1.2	V
High Level Output Voltage (V_{OH})	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = Max		2.4			V
Low Level Output Voltage (V_{OL})	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = Max	DM54S200 / DM74S200			0.5 / 0.45	V
Off State (High Impedance State) Output Current ($I_{O(OFF)}$)	V_{CC} = Max, V_{IH} = 2.0V					
	V_O = 2.4V				50	μA
	V_O = 0.5V				−50	μA
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V				1.0	mA
High Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.7V				25	μA
Low Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.5V				−250	μA
Short Circuit Output Current (I_{OS}) (Note 3)	V_{CC} = Max		−30		−100	mA
Supply Current (I_{CC})	V_{CC} = Max (Note 5)			87	130	mA

switching characteristics All Typical Values are at V_{CC} = 5.0V, T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	PARAMETER CONDITIONS	TEST CONDITIONS	DM54S200			DM74S200			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address			33	70		33	50	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address			29	70		29	50	ns
t_{ZH}	Output Enable Time to High Level	Access Times from Memory Enable	C_L = 30 pF, R_L = 300Ω		21	45		21	35	ns
t_{ZL}	Output Enable Time to Low Level	Access Times from Memory Enable			10	30		10	20	ns
t_{ZH}	Output Enable Time to High Level	Sense Recovery Times from Write Enable			24	50		24	40	ns
t_{ZL}	Output Enable Time to Low Level	Sense Recovery Times from Write Enable			12	50		12	40	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Memory Enable			7.0	30		7.0	20	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Memory Enable	C_L = 5.0 pF R_L = 300Ω		20	45		20	35	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Write Enable			13	40		13	30	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Write Enable			16	40		16	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM54S200 and across the 0°C to +70°C range for the DM74S200. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Duration of the short-circuit should not exceed one second.

Note 4: All voltage values are with respect to network ground terminal.

Note 5: I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.

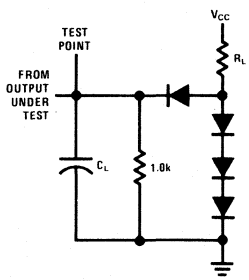
truth table

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = high level, L = low level, X = irrelevant

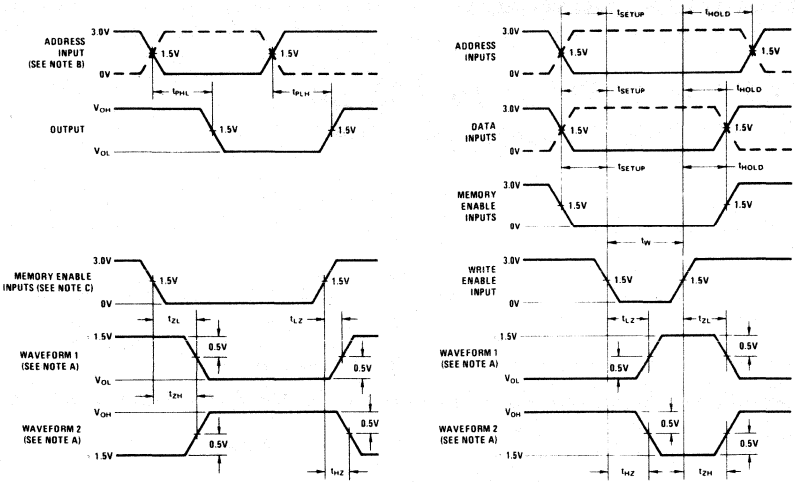
†For memory enable: L = all ME inputs low; H = one or more ME inputs high.

ac test circuit



C_L INCLUDES PROBE AND JIG CAPACITANCE.
ALL DIODES ARE 1N3064.

switching time waveforms



NOTE A: WAVEFORM 1 IS FOR THE OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED. WAVEFORM 2 IS FOR THE OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED.

NOTE B: WHEN MEASURING DELAY TIMES FROM ADDRESS INPUTS, THE MEMORY ENABLE INPUTS ARE LOW AND THE WRITE ENABLE INPUT IS HIGH.

NOTE C: WHEN MEASURING DELAY TIMES FROM MEMORY ENABLE INPUTS, THE ADDRESS INPUTS ARE STEADY-STATE AND THE WRITE ENABLE INPUT IS HIGH.

NOTE D: INPUT WAVEFORMS ARE SUPPLIED BY PULSE GENERATORS HAVING THE FOLLOWING CHARACTERISTICS: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, AND $Z_{OUT} \approx 50\Omega$.

National Semiconductor

DM54S206/DM74S206 256-Bit (256 × 1) Open-Collector RAM

general description

The DM54S206/DM74S206 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

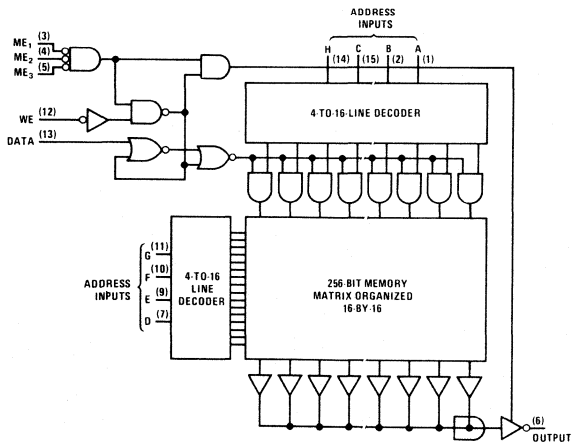
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is off.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be off.

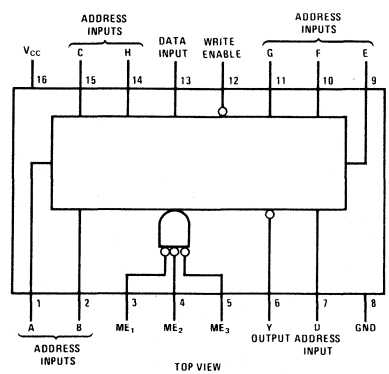
features

- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 17 ns typ
  - Access from address inputs 35 ns typ
  - Power dissipation 1.4 mW/bit typ
- Open-collector output for word expansion
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

block and connection diagrams



Dual-In-Line Package



Order Number DM54S206J or DM74S206J
See NS Package J16A

Order Number DM74S206N
See NS Package N16A

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S206	4.5	5.5	V
DM74S206	4.75	5.25	V
Temperature (T_A)			
DM54S206	−55	+125	°C
DM74S206	0	+70	°C

operating conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Level Output Current (I_{OL})				16	mA
Width of Write Enable Pulse (t_W)					
DM54S206		50			ns
DM74S206		40			ns
Setup Time (t_{SETUP})					
Address to Write Enable		0			ns
Data to Write Enable		0			ns
Memory Enable to Write Enable		0			ns
Hold Time (t_{HOLD})					
Address from Write Enable		10			ns
Data from Write Enable		10			ns
Memory Enable from Write Enable		0			ns

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Input Voltage (V_{IH})		2			V
Low-Level Input Voltage (V_{IL})				0.8	V
Input clamp voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
High-Level Output Current (I_{OH})	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V				
	V_{OH} = 2.4V			40	μA
	V_{OH} = 5.5V			100	μA
Low-Level Output Voltage (V_{OL}) DM54S206 / DM74S206	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5 / 0.45	V
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V			1	mA
High-Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.7V			25	μA
Low-Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.5V			−250	μA
Supply Current (I_{CC})	V_{CC} = Max, Note 2		70	130	mA

switching characteristics

All typical values are at V_{CC} = 5.0V, T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		DM54S206			DM74S206			
		MIN	TYP	MAX	MIN	TYP	MAX	
Access Times from Address (t_{PLH})	C_L = 30 pF, R_L = 300Ω		38	80		38	60	ns
Access Times from Address (t_{PHL})			32	80		32	60	ns
Disable Time from Memory Enable (t_{PLH})			21	45		21	35	ns
Enable Time from Memory Enable (t_{PHL})			13	35		13	25	ns
Disable Time from Write Enable (t_{PLH})			20	50		20	40	ns
Sense-Recovery Time (t_{SR})			14	50		14	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM54S206 and across the 0°C to +70°C range for the DM74S206. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: All voltage values are with respect to network ground terminal.

Note 4: I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.

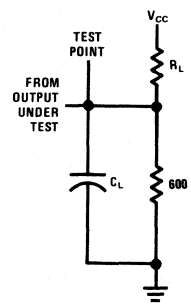
truth table

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant

†For memory enable: L = all ME inputs low; H = one or more ME inputs high.

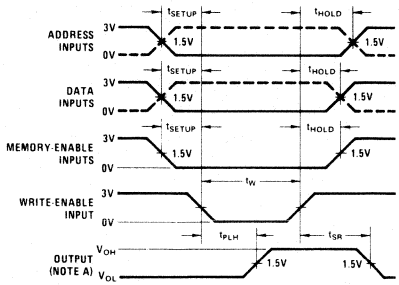
ac test circuit



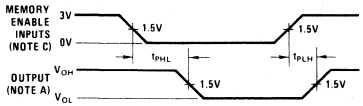
C_L includes probe and jig capacitance.

switching time waveforms

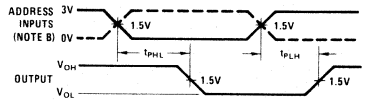
Write-Cycle



Access (Enable) Time and Disable Time from Memory Enable



Access Time from Address Inputs



Note A: Waveform shown is for the output with internal conditions such that the output is low except when disabled.
Note B: When measuring delay times from address inputs, the memory-enable inputs are low and the write-enable input is high.
Note C: When measuring delay times from memory-enable inputs, the address inputs are steady-state and the write-enable input is high.
Note D: Input waveforms are supplied by pulse generators having the following characteristics: t_r 2.5 ns, t_f 2.5 ns, PRR 1 MHz, and Z_{OUT} 50Ω.

National Semiconductor

DM54LS289/DM74LS289 64-Bit (16 × 4) Open-Collector RAM

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip enable input to simplify decoding required to achieve the desired system organization. This device is implemented with low power Schottky technology resulting in one-fifth power while retaining the speed of standard TTL.

The open-collector outputs are ideal for controlled-impedance bus lines.

The unique functional capability of the DM54LS289 outputs being at a high during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-logic level (OFF).

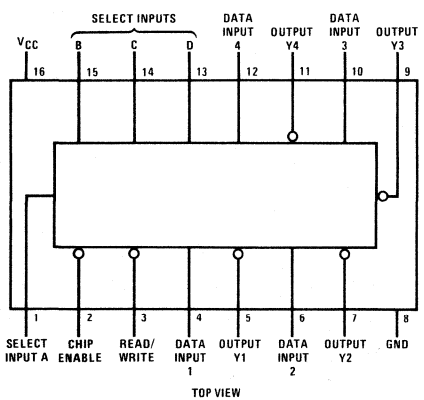
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs are high (OFF).

features

- Schottky-clamped for high speed applications
  - Access from chip enable input—40 ns typ
  - Access from address inputs—60 ns typ
- Open-collector outputs for controlled-impedance bus lines
- DM54LS189/DM74LS189 are functionally equivalent, but have TRI-STATE® outputs
- DM54LS289 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip enable input simplifies system decoding

connection diagram

Dual-In-Line Package



Order Number DM54LS289J or DM74LS289J
See NS Package J16A

Order Number DM74LS289N
See NS Package N16A

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level
L = low level
X = don't care

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54LS289	4.5	5.5	V
DM74LS289	4.75	5.25	V
Temperature (T_A)			
DM54LS289	−55	+125	°C
DM74LS289	0	+70	°C

electrical characteristics

Over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	2.4	3.4		V
				2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 4 mA DM54LS289			0.45	V
			I_{OL} = 8 mA DM74LS289			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−100	μA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			15	29	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V

switching characteristics

Over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			CONDITIONS	DM54LS289			DM74LS289			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{AA}	Access Times From Address		C_L = 30 pF, R_L = 1 kΩ,		60	110		60	90	ns
t_{CZH}	Output Enable Time to High Level	Access Times From Chip Enable			40	90		40	70	ns
t_{CZL}	Output Enable Time to Low Level				40	90		40	70	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times From Read/Write			60	110		60	90	ns
t_{WZL}	Output Enable Time to Low Level				60	110		60	90	ns
t_{CHZ}	Output Disable Time From High Level	Disable Times From Chip Enable	C_L = 5 pF, R_L = 1 kΩ,		40	90		40	70	ns
t_{CLZ}	Output Disable Time From Low Level				40	90		40	70	ns
t_{WHZ}	Output Disable Time From High Level	Disable Times From Read/Write			40			40		ns
t_{WLZ}	Output Disable Time From Low Level				40			40		
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			100			80			ns
t_{ASW}	Set-Up Time	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		100			80			
t_{CSW}		Chip Enable to Read/Write		0			0			
t_{AHW}	Hold Time	Address From Read/Write		50			50			ns
t_{DHW}		Data From Read/Write		0			0			
t_{CHW}		Chip Enable From Read/Write		0			0			

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54LS289 and across the 0°C to +70°C range for the DM74LS289. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded, and the outputs open.

DM54S289/DM74S289 64-Bit (16 × 4) Open-Collector RAM

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-logic level ("OFF").

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs are high ("OFF").

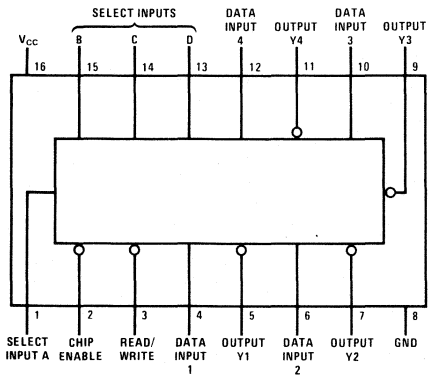
The fast access time of the DM54S289 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 ns. The unique functional capability of the DM54S289 outputs being at a high during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

features

- Schottky-clamped for high-speed applications:
  Access from chip-enable 12 ns typ
  Access from address inputs 25 ns typ
- Open collector outputs for controlled-impedance bus lines
- DM54S189/DM74S189 are functionally equivalent, but have TRI-STATE® outputs
- DM54S289 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip-enable input simplifies system decoding
- Compatible with Intel 3101A in most applications

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S289J or DM74S289J
See NS Package J16A
Order Number DM74S289N
See NS Package N16A

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = High Level
L = Low Level
X = Don't Care

absolute maximum ratings

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S289	4.5	5.5	V
DM74S289	4.75	5.25	V
Temperature (T_A)			
DM54S289	−55	+125	°C
DM74S289	0	+70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
I_{OH}	High Level Output Current	V_{CC} = Min	V_{OH} = 2.4V				40	μA
			V_{OH} = 5.5V				100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		DM54S289			0.5	V
				DM74S289			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7					25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V					1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V					−250	μA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)				75	105	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.2	V

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			CONDITIONS	DM54S289			DM74S289			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{AA}		Access Times From Address	C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω, *(Figure 1)*		25	50		25	35	ns
t_{CHL}	Enable Time From Chip Enable				12	25		12	17	ns
t_{WHL}	Enable Time From Read/Write	Sense Recovery Time From Read/Write			22	40		22	35	ns
t_{CLH}	Disable Time From Chip Enable				12	25		12	17	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			
t_{CSW}		Chip-Enable to Read/Write		0			0			
t_{AHW}	Hold Time *(Figure 1)*	Address From Read/Write		0			0			ns
t_{DHW}		Data From Read/Write		0			0			
t_{CHW}		Chip-Enable From Read/Write		0			0			

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S289 and across the 0°C to +70°C range for the DM74S289. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: I_{CC} is measured with all inputs grounded, and the outputs open.

switching time waveforms

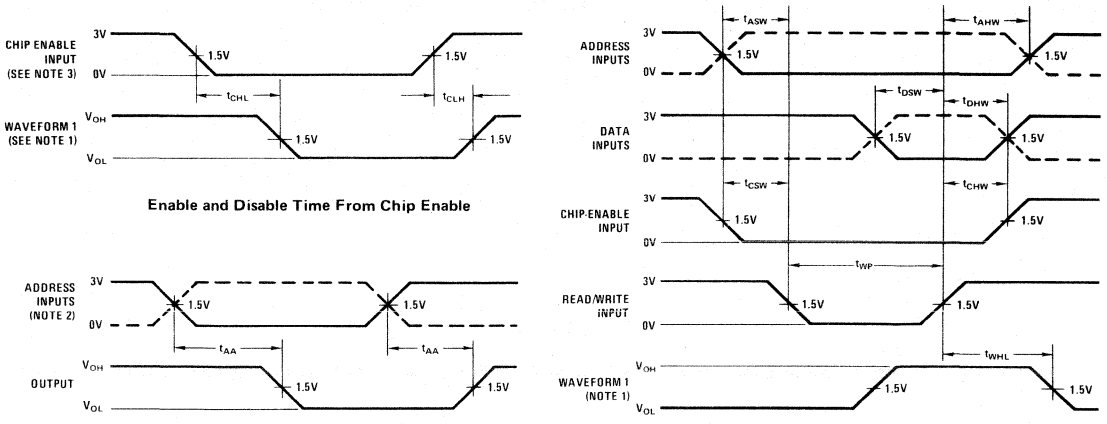


FIGURE 1

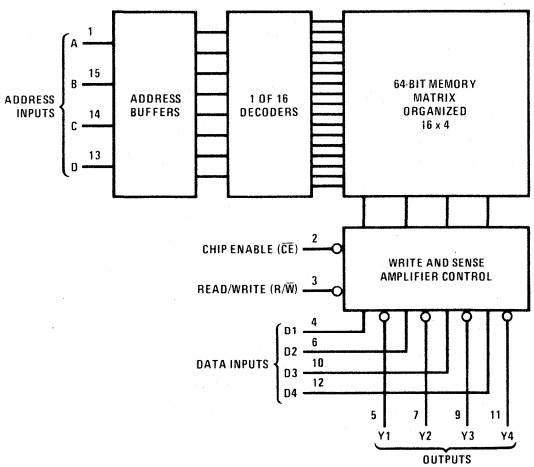
Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip enable input is low and the read/write input is high.

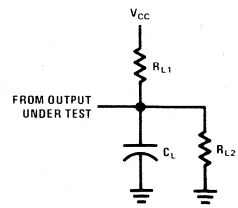
Note 3: When measuring delay times from chip enable input, the address inputs are steady state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

block diagram



ac test circuit



National Semiconductor

DM85S68 64-Bit (16 × 4) Edge Triggered Register

general description

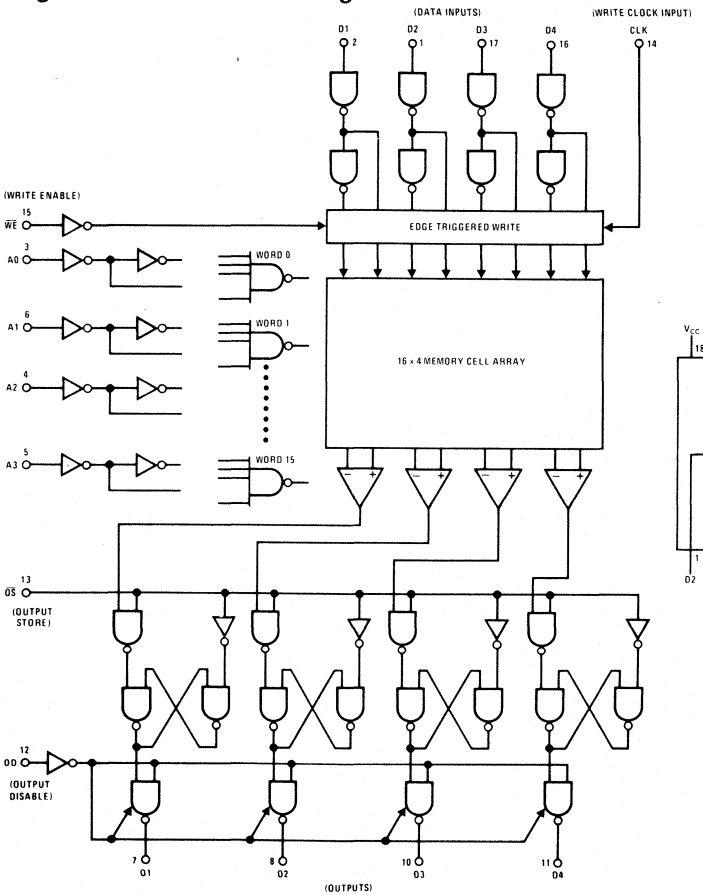
The DM85S68 is an addressable "D" register file. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

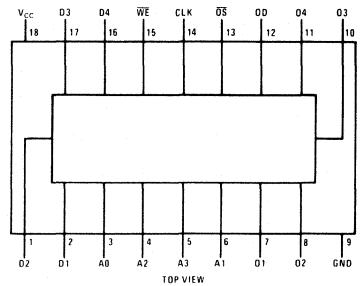
features

- On chip output register
- Edge triggered write
- High speed — 30 ns typ
- TRI-STATE output
- Optimized for register stack applications
- Typical power dissipation — 350 mW
- 18-pin package

logic and connection diagrams



Dual-In-Line Package



Order Number DM85S68J
See NS Package J18A

Order Number DM85S68N
See NS Package N18A

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	70	°C

electrical characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −5.2 mA		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA				0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.4V	Clock Input			50	μA
			All Others			25	
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_{IH} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.5V	Clock Input			−500	μA
			All Others			−250	μA
I_{OS}	Short Circuit Output Current(4)	V_{CC} = Max, V_{OL} = 0V		−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max			70	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{OZ}	TRI-STATE Output Current	V_{CC} = Max	V_O = 2.4V			+40	μA
			V_O = 0.5V			−40	

switching characteristics over recommended operating range of T_A and V_{CC} (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNITS
t_{ZH}	Output Enable to High Level			20	35	ns
t_{ZL}	Output Enable to Low Level			14	24	ns
t_{HZ}	Output Disable Time From High Level			10	15	ns
t_{LZ}	Output Disable Time From Low Level			12	18	ns
t_{AA}	Access Time	Address to Output		30	40	
t_{OSA}		Output Store to Output		20	30	ns
t_{CA}		Clock to Output		25	40	
t_{ASC}	Set-Up Time	Address to Clock	15	5		
t_{DSC}		Data to Clock	5	5		ns
t_{ASOS}		Address to Output Store	30	0		
t_{WESC}		Write Enable Set-Up Time	5	15		
t_{OSSC}		Store Before Write (t_{10})	10	0		
t_{AHC}	Hold Time	Address From Clock	10	5		
t_{DHC}		Data From Clock	15	5		ns
t_{AHOS}		Address From Output Store	5	0		
t_{WEHC}		Write Enable Hold Time	15	5		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DM85S68. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

typical applications

The DM85S68 can enhance the dynamic performance of a TTL processor, since it may safely operate using single phase clocking instead of the multiphase clocking systems being used currently. This simple feature not only enhances the system's dynamic performance, since multiple levels of registers need not be activated, but also reduces component count by elimination of one set of buffer registers. For example, note the simplicity of register file/ALU loop shown in *Figure 1*.

In a four-bit slice with zero delay within the arithmetic-logic unit, a level-triggered memory with buffering to prevent logic oscillation requires about 80 ns to make the loop with a 30 ns delay in the ALU, the system speed is 110 ns.

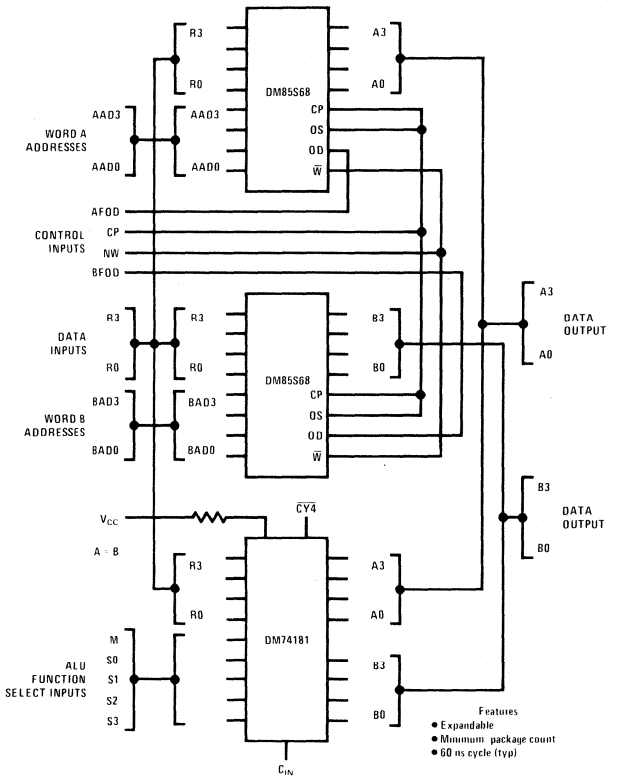
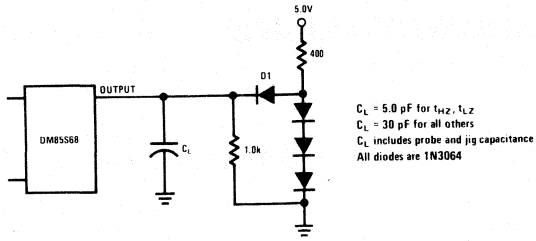


FIGURE 1. 4-Bit Register ALU

truth table

O_D	$\overline{W_E}$	CLK	$\overline{O_S}$	MODE	OUTPUTS
0	X	X	0	Output Store	Data From Last Addressed Location
X	0	⌐	X	Write Data	Dependent on State of OD and $\overline{OS}$
0	X	X	1	Read Data	Data Stored in Addressed Location
1	X	X	0	Output Store	High Impedance State
1	X	X	1	Output Disable	High Impedance State

ac test circuit and switching time waveforms



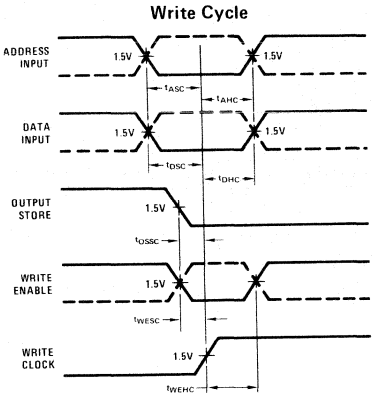


FIGURE 2. Clock Set-Up and Hold Time

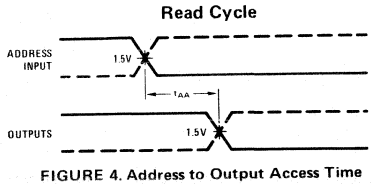


FIGURE 4. Address to Output Access Time

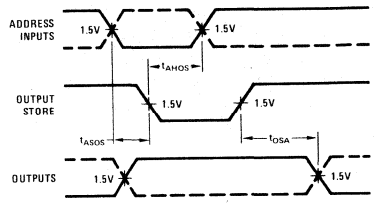


FIGURE 5. Output Store Access, Set-Up and Hold Time

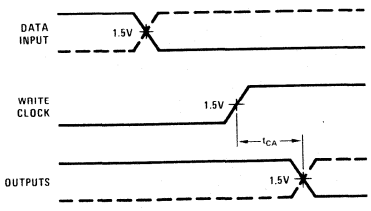


FIGURE 3. Clock to Output Access

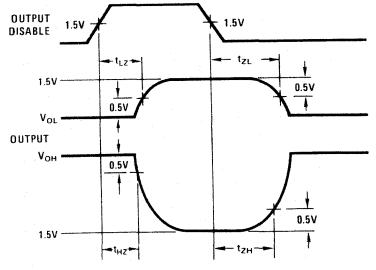


FIGURE 6. Output Disable and Enable Time

Note: Input waveforms supplied by pulse generator having the following characteristics: V = 3.0V, $t_R \leq 2.5$ ns, PRR $\leq$ 1.0 MHz and Z_{OUT} = 50M

National Semiconductor

DM7589/DM8589 64-Bit (16 × 4) RAM

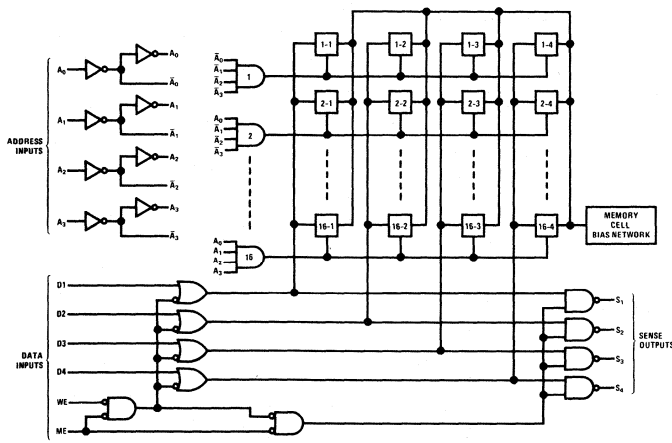
general description

The DM7589/DM8589 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

features

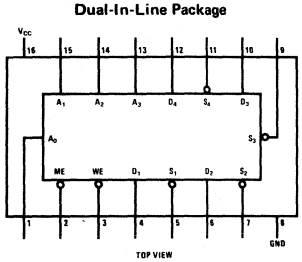
- Series 54/74 compatible
- Organized as 16 4-bit words
- Typical access from chip enable 23 ns
- Typical access 35 ns
- Typical power dissipation 400 mW
- Open collector outputs to permit "wire OR" capability

block diagram



connection diagram

Dual-In-Line Package



Order Number DM7589J or DM8589J
See NS Package J16A

Order Number DM8589N
See NS Package N16A

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM7589	−55°C to +125°C
DM8589	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7589	V_{CC} = 4.5V		2.0			V
	DM8589	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7589	V_{CC} = 4.5V				0.8	V
	DM8589	V_{CC} = 4.75V					
Logical "1" Output Current	DM7589	V_{CC} = 5.5V	V_O = 5.25V			100	μA
	DM8589	V_{CC} = 5.25V				20	μA
Logical "0" Output Voltage	DM7589	V_{CC} = 4.5V	I_O = 12 mA			0.4	V
	DM8589	V_{CC} = 4.75V					
Logical "1" Input Current	DM7589	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8589	V_{CC} = 5.25V					
	DM7589	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8589	V_{CC} = 5.25V					
Logical "0" Input Current	DM7589	V_{CC} = 5.5V				−1.6	mA
	DM8589	V_{CC} = 5.25V					
Supply Current	DM7589	V_{CC} = 5.5V	All Inputs at GND		80	120	mA
	DM8589	V_{CC} = 5.25V					
Input Clamp Voltage	DM7589	V_{CC} = 4.5V	I_{IN} = −12 mA			−1.5	V
	DM8589	V_{CC} = 4.75V					

switching characteristics (Over recommended operating ranges of V_{CC} and T_A)

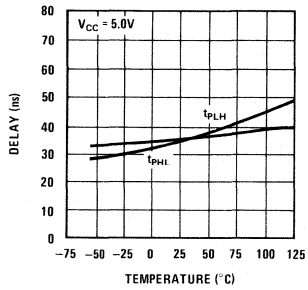
PARAMETER			CONDITIONS	DM7589			DM8589			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Access Time From Address		R_{L1} = 300Ω, R_{L2} = 600Ω, C_L = 30 pF		34	80		34	60	ns
t_{PHL}					35	80		35	60	ns
t_{PLH}	Disable Time From Memory Enable				23	55		23	40	ns
t_{PHL}	Enable Time From Memory Enable				23	55		23	40	ns
t_{SETUP}	Setup Time	Address to Write Enable		0	−14		0	−14		ns
		Data to Write Enable		0	−15		0	−15		ns
		Memory Enable To Write Enable		0	−10		0	−10		ns
t_{HOLD}	Hold Time	Address From Write Enable		5	−7		5	−7		ns
		Data From Write Enable		0	−14		0	−14		ns
		Memory Enable From Write Enable		0	−10		0	−10		ns
t_{WP}	Write Pulse Width			50	20		40	20		ns
t_{SR}	Sense Recovery Time				31	65		31	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

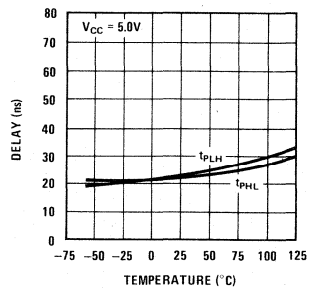
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7589 and across the 0°C to 70°C range for the DM8589. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

typical performance characteristics

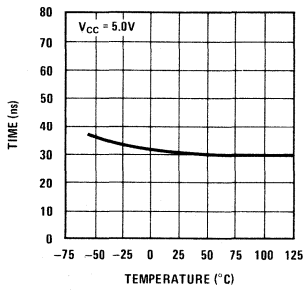
Delay from Address to Output



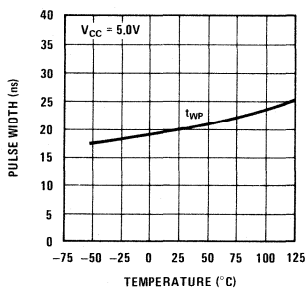
Delay from Memory Enable to Output



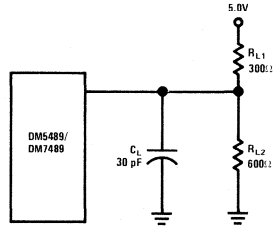
Sense Recovery Time



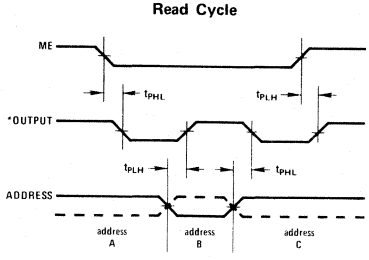
Minimum Write Pulse Width



ac test circuit and switching time waveforms

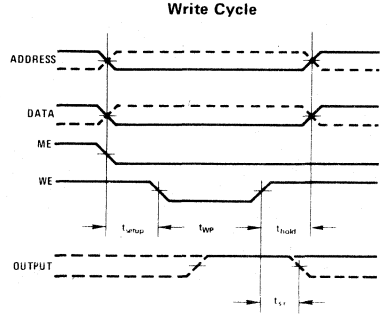


Read Cycle



*Output shown for stored data in address A = 1, in address B = 0.

Write Cycle



National Semiconductor

DM7599/DM8599 64-Bit (16 × 4) TRI-STATE® RAM

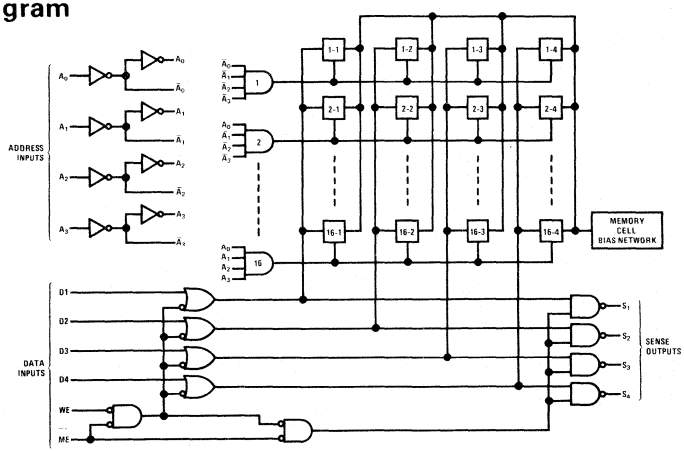
general description

The DM7599/DM8599 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

features

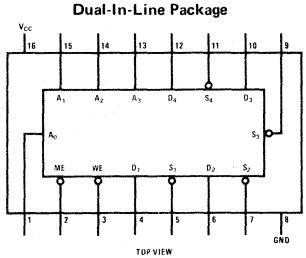
- Series 54/74 compatible
- Same pin-out as SN5489/SN7489
- Organized as 16 4-bit words
- Expandable to 2048 4-bit words without additional resistors (DM8599 only)
- Typical access from chip enable 20 ns
- Typical access time 28 ns
- Typical power dissipation 400 mW

block diagram



connection diagram

Dual-In-Line Package



Order Number DM7599J or DM8599J
See NS Package J16A
Order Number DM8599N
See NS Package N16A

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Hi-Z State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

absolute maximum ratings (Note 1)

Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V	Operating Temperature Range	
Output Voltage	5.5V	DM7599	−55°C to +125°C
Time that two bus-connected devices may be in opposite low impedance states simultaneously	Indefinite	DM8599	0°C to +70°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7599	V_{CC} = 4.5V		2.0			V
	DM8599	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7599	V_{CC} = 4.5V				0.8	V
	DM8599	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7599	V_{CC} = 4.5V	I_O = −2 mA	2.4			V
	DM8599	V_{CC} = 4.75V	I_O = −5.2 mA	2.4			V
Logical "0" Output Voltage	DM7599	V_{CC} = 4.5V	I_O = 12 mA			0.4	V
	DM8599	V_{CC} = 4.75V					
Third State Output Current	DM7599	V_{CC} = 5.5V	V_O = 0.4V			±40	μA
	DM8599	V_{CC} = 5.25V	V_O = 2.4V			±40	
Logical "1" Input Current	DM7599	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8599	V_{CC} = 5.25V					
	DM7599	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8599	V_{CC} = 5.25V					
Logical "0" Input Current	DM7599	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.6	mA
	DM8599	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7599	V_{CC} = 5.5V		−30		−70	mA
	DM8599	V_{CC} = 5.25V					
Supply Current	DM7599	V_{CC} = 5.5V	All Inputs at GND		80	120	mA
	DM8599	V_{CC} = 5.25V					
Input Clamp Voltage	DM7599	V_{CC} = 4.5V	I_{IN} = −12 mA			−1.5	V
	DM8599	V_{CC} = 4.75V					

switching characteristics (Over recommended operating ranges of V_{CC} and T_A)

PARAMETER			CONDITIONS	DM7599			DM8599			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Access Time From Address		R_{L1} = 400Ω, R_{L2} = 1.0 kΩ, C_L = 50 pF		27	70		27	50	ns
t_{PHL}					28	70		28	50	ns
t_{ZH}	Enable Time From Memory Enable				16	45		16	30	ns
t_{ZL}					20	40		20	35	ns
t_{ZH}	Sense Recovery Time From Write Enable				20	40		20	35	ns
t_{ZL}					35	65		35	55	ns
t_{HZ}	Disable Time From Memory Enable		R_{L1} = 400Ω, R_{L2} = 1.0k, C_L = 5.0 pF		10	30		10	25	ns
t_{LZ}					14	35		14	30	ns
t_{SETUP}	Setup Time	Address to Write Enable		0	−14		0	−14		ns
		Data to Write Enable		0	−15		0	−15		ns
		Memory Enable to Write Enable		0	−10		0	−10		ns
t_{HOLD}	Hold Time	Address From Write Enable		5	−7		5	−7		ns
		Data From Write Enable		0	−14		0	−14		ns
		Memory Enable From Write Enable		0	−10		0	−10		ns
t_{WP}	Write Pulse Width			50	20		40	20		ns

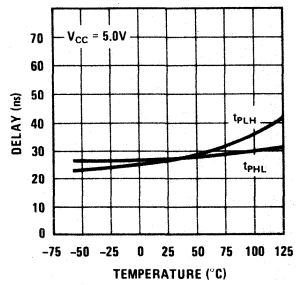
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7599 and across the 0°C to 70°C range for the DM8599. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

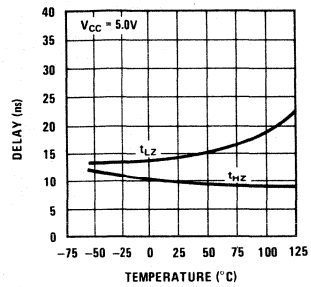
Note 3: Only one output at a time should be shorted.

typical performance curves

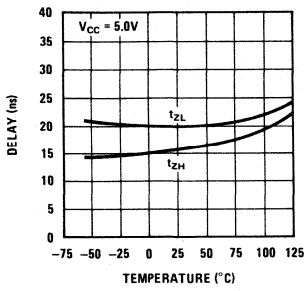
Delay from Address to Output



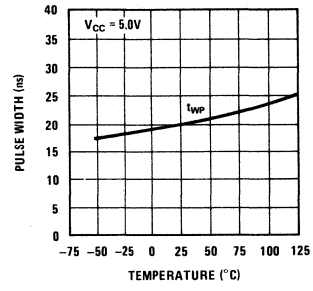
Delay From Memory Enable To High Impedance State



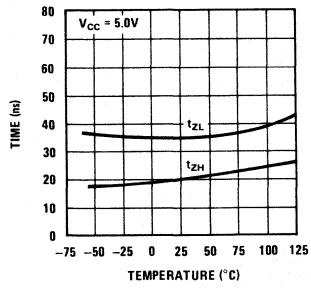
Delay from Memory Enable to Low Impedance State



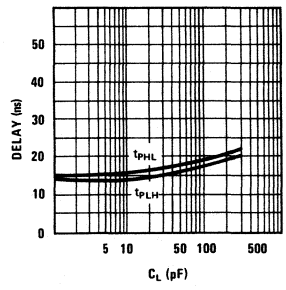
Minimum Write Pulse Width



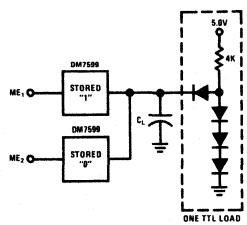
Sense Recovery Time



Delay from Enable to Output vs Load Capacitance



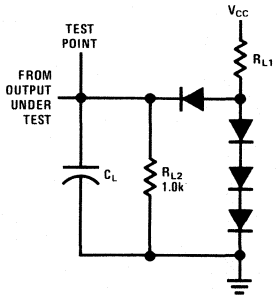
test circuit



Test Circuit for Delay vs Load Capacitance

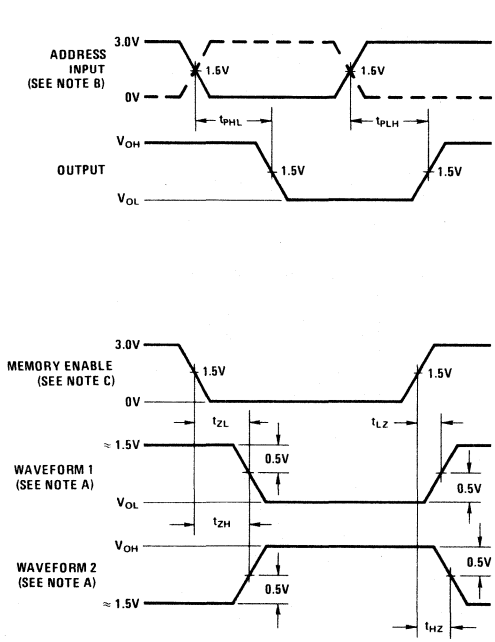
Note: In a typical application the output of the TRI-STATE memories might be wired together and one would be switching to the low impedance state at the same time the circuit previously selected would be switching back into the high impedance state. The measurements of delay versus load capacitance were made under conditions which simulate actual operating conditions in an application. (See test circuit.)

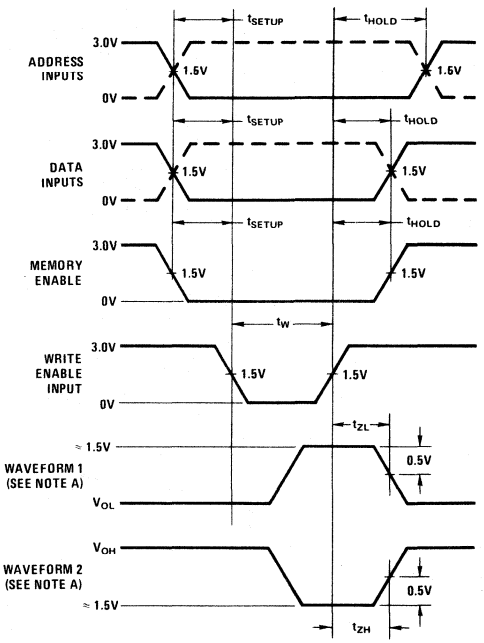
ac test circuit



C_L includes probe and jig capacitance.
All diodes are 1N3064.

switching time waveforms





Note A: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note B: When measuring delay times from address inputs, the memory enable input is low and the write enable input is high.

Note C: When measuring delay times from memory enable input, the address inputs are steady-state and the write enable input is high.

Note D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1.0 MHz, and $Z_{OUT} \approx 50\Omega$.

Section 3

CMOS RAMs

3

CMOS RAMs provide the lowest power of any of the semiconductor read/write memory technologies. National's CMOS memory line may be mixed with our CMOS logic, TTL logic, bipolar microprocessor, MOS microprocessor, custom LSI, and our other semiconductor products to optimize system power/speed/cost tradeoffs. Refer to National's related databooks and catalogs for further details; an order form is included in this book.

National Semiconductor

MM54C89/MM74C89
64-Bit (16 × 4) TRI-STATE® RAM

general description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

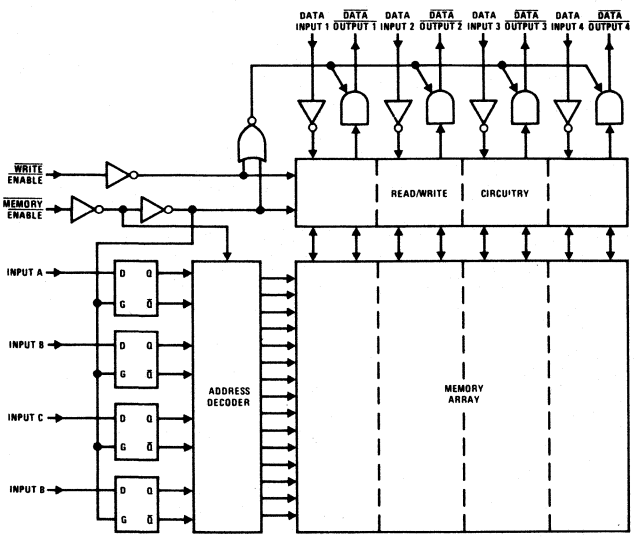
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

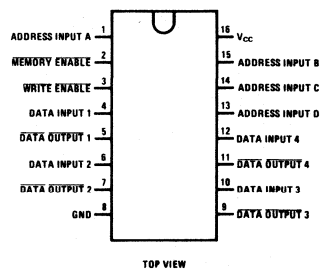
features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 100 nW/package typ @ V_{CC} = 5V
- Fast access time — 130 ns typ at V_{CC} = 10V
- TRI-STATE output

logic and connection diagrams



Dual-In-Line Package



Order Number MM54C89D
or MM74C89D
See NS Package D16C

Order Number MM74C89N
See NS Package N16A

absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics (T_A = 25°C, C_L = 50 pF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from $\overline{\text{Memory Enable}}$ (t_{pd})	V_{CC} = 5.0V		270	500	ns
	V_{CC} = 10V		100	220	ns
Access Time from Address Input (t_{acc})	V_{CC} = 5.0V		350	650	ns
	V_{CC} = 10V		130	280	ns
Address Input Setup Time (t_{SA})	V_{CC} = 5.0V	150			ns
	V_{CC} = 10V	60			ns
Address Input Hold Time (t_{HA})	V_{CC} = 5.0V	60			ns
	V_{CC} = 10V	40			ns
$\overline{\text{Memory Enable}}$ Pulse Width (t_{ME})	V_{CC} = 5.0V	400	250		ns
	V_{CC} = 10V	150	90		ns
$\overline{\text{Memory Enable}}$ Pulse Width ($t_{\overline{ME}}$)	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	150	70		ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Read (t_{SR})	V_{CC} = 5.0V V_{CC} = 10V	0 0			ns ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Write (t_{WS})	V_{CC} = 5.0V V_{CC} = 10V			t_{ME} t_{ME}	ns ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V, t_{WS} = 0 V_{CC} = 10V, t_{WS} = 0	300 100	160 60		ns ns
Data Input Hold Time (t_{HD})	V_{CC} = 5.0V V_{CC} = 10V	50 25			ns ns
Data Input Setup (t_{SD})	V_{CC} = 5.0V V_{CC} = 10V	50 25			ns ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		180 85	300 120	ns ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Write}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		180 85	300 120	ns ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity (C_{OUT})	Any Output (Note 2)		6.5		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

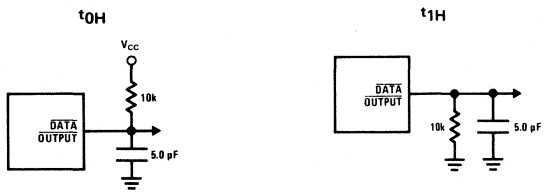
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

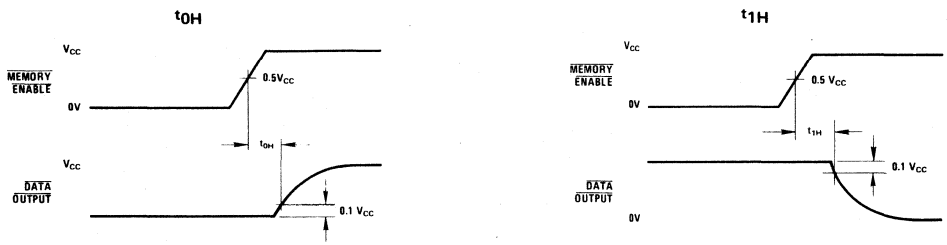
truth table

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

ac test circuits

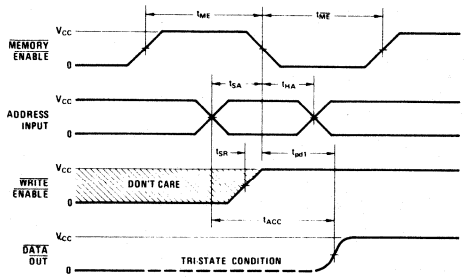


switching time waveforms

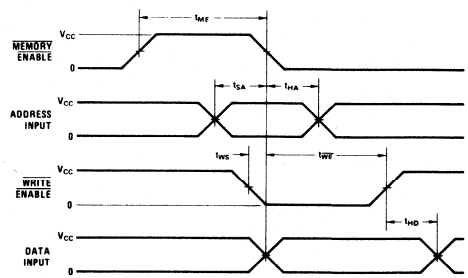


switching time waveforms (con't)

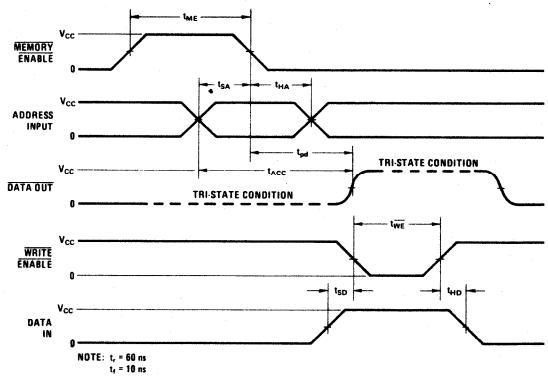
Read Cycle



Write Cycle



Read Modify Write Cycle



National Semiconductor

MM54C989/MM74C989
64-Bit (16 × 4) TRI-STATE® RAM

General Description

The MM54C989/MM74C989 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of 4 address lines, 4 data input lines, a write enable line and a memory enable line. The 4 binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The 4 TRI-STATE data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note. The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

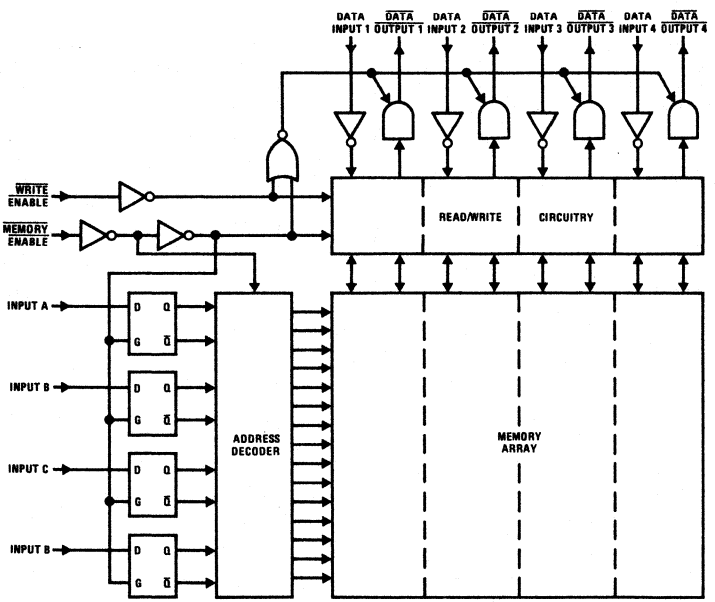
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the 4 outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-Z) condition.

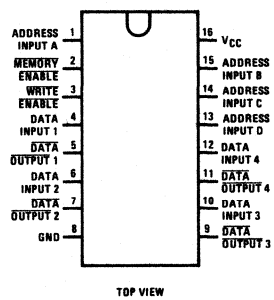
Features

■ Wide supply voltage range	3.0V to 5.5V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Input address register	
■ Low power consumption	250 nW/package typ @ V_{CC} = 5V
■ Fast access time	140 ns typ at V_{CC} = 5V
■ TRI-STATE output	

Logic and Connection Diagrams



Dual-in-Line Package



TOP VIEW

Order Number MM54C989D or MM74C989D
See NS Package D16C

Order Number MM74C989N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 5.5V
Standby V_{CC} Range	1.5V to 5.5V
Absolute Maximum V_{CC}	7.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C989	4.7	5.5	V
MM74C989	4.75	5.25	V
Temperature (T_A)			
MM54C989	−55	+125	°C
MM74C989	−40	+85	°C

DC Electrical Characteristics MM54C989/MM74C989

(Min/max limits apply across the temperature and power supply range indicated).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA	2.4			V
		I_O = −150 μA	V_{CC}−0.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 360 μA			0.4	V
	Output Current in High Impedance State	V_O = 5V		0.005	1	μA
		V_O = 0	−1	−0.005		μA
I_{CC}	Supply Current (Active)	$\overline{ME}$ = 0, V_{CC} = 5V		0.05	150	μA
	Supply Current (Stand-By)	$\overline{ME}$ = 5V			3	μA

AC Electrical Characteristics MM54C989/MM74C989

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

PARAMETER		MIN	TYP	MAX	UNITS
t_{ACC}	Access Time From Address		140	500	ns
t_{PD}	Propagation Delay From $\overline{ME}$		110	360	ns
t_{SA}	Address Input Set-Up Time	140	30		ns
t_{HA}	Address Input Hold Time	20	15		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	80		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	100		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	20		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE, C_L = 5 pF, R_L = 10k, (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity, Any Input, (Note 2)		5		pF
C_{OUT}	Output Capacity, Any Output, (Note 2)		8		pF
C_{PD}	Power Dissipation Capacity, (Note 3)		350		pF

AC Electrical Characteristics (Continued)

MM54C989: $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$. $C_L = 50$ pF
MM74C989: $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.75V$ to $5.25V$. $C_L = 50$ pF

PARAMETER		MM54C989		MM74C989		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time From Address		500		620	ns
t_{PD1}, t_{PD0}	Propagation Delay From $\overline{ME}$		350		430	ns
t_{SA}	Address Input Set-Up Time	150		140		ns
t_{HA}	Address Input Hold Time	50		60		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	250		310		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	520		400		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	60		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	220		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE, (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

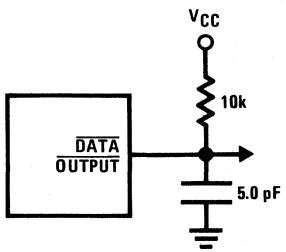
Note 4: See AC test circuit for t_{1H}, t_{0H}.

Truth Table

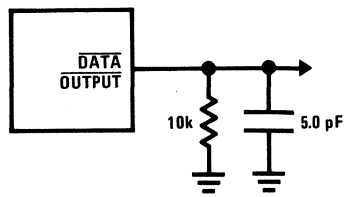
$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

AC Test Circuits

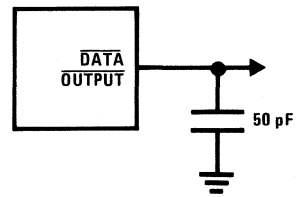
t_{0H}



t_{1H}

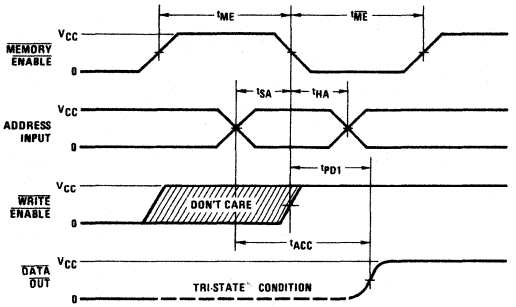


All Other AC Tests

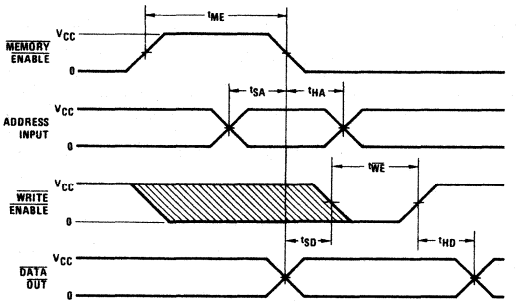


Switching Time Waveforms

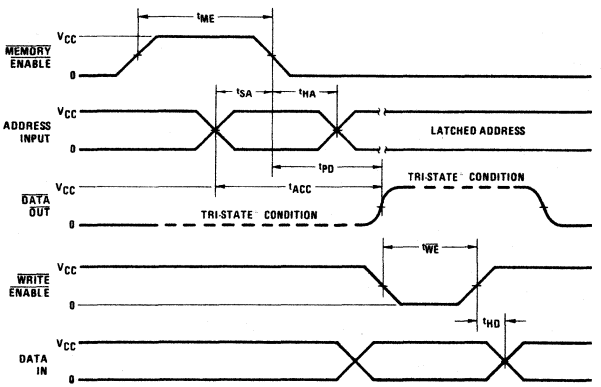
Read Cycle (Note 1)



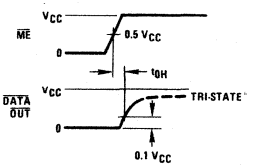
Write Cycle (Note 1)



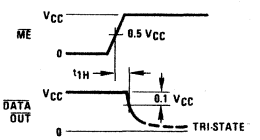
Read-Modify-Write Cycle (Note 1)



t_{0H}



t_{1H}



Note 1: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} ns between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

MM54C200/MM74C200
256-Bit (256 × 1) TRI-STATE® RAM

general description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a write enable line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different than the DM74200 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and write enable high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control, provides for fast access times by not totally disabling the chip.

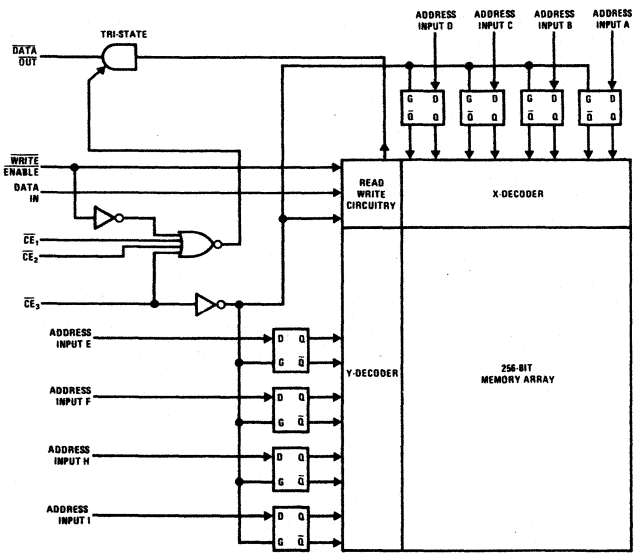
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and write enable low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with write enable low.

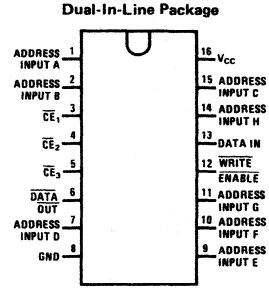
features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW typ
■ Internal address register	

3

logic and connection diagrams





Order Number MM54C200D
or MM74C200D
See NS Package D16C

Order Number MM74C200N
See NS Package N16A

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C200	−55°C to +125°C
MM74C200	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V V_{IN} = 0V	1.0	0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.10	600	μA
CMOS/TTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V	−4.0	−6.0		mA
	T_A = 25°C	−1.8			
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V	−16.0	−25		mA
	T_A = 25°C	−1.50			
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}	5.0	8.0		mA
	T_A = 25°C				
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}	20.0	30		mA
	T_A = 25°C				

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Access Time From Address (t_{ACC})	V_{CC} = 5.0V		450	900	ns
	V_{CC} = 10V		200	400	ns
Propagation Delay From $\overline{CE}_3$ (t_{pd})	V_{CC} = 5.0V		360	700	ns
	V_{CC} = 10V		120	300	ns
Propagation Delay From $\overline{CE}_1$ or $\overline{CE}_2$ ($t_{p\overline{CE}1}$)	V_{CC} = 5.0V		250	500	ns
	V_{CC} = 10V		85	200	ns
Address Setup Time (t_{SA})	V_{CC} = 5.0V	200	80		ns
	V_{CC} = 10V	100	30		ns
Address Hold Time (t_{HA})	V_{CC} = 5.0V	50	15		ns
	V_{CC} = 10V	25	5		ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V	300	160		ns
	V_{CC} = 10V	150	70		ns
$\overline{CE}_3$ Pulse Widths (t_{CE})	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	160	80		ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity in TRI-STATE (C_{OUT})	(Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		400		pF

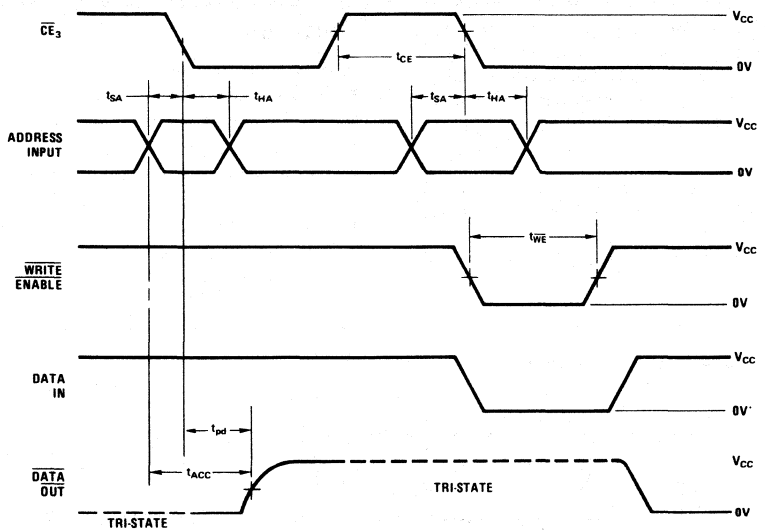
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

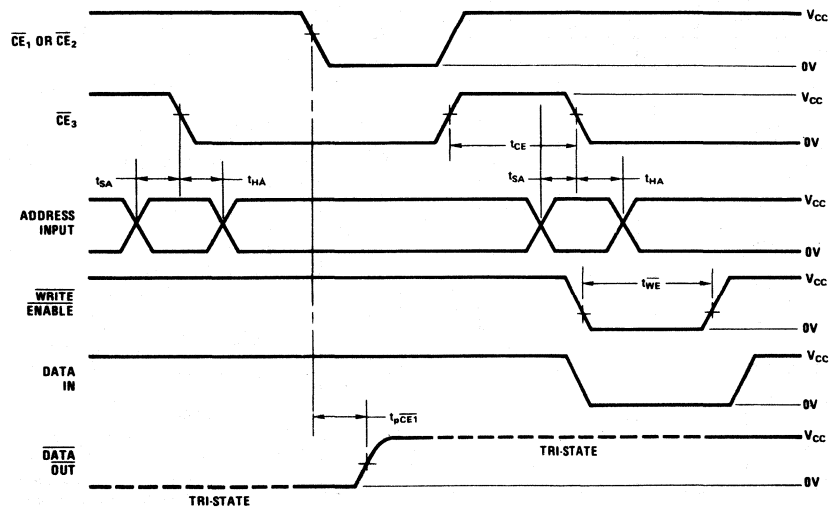
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

National Semiconductor

MM54C910/MM74C910
256-Bit (64 × 4) TRI-STATE® RAM

general description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a write enable, and a memory enable line. The six address lines are internally decoded to select one of 64 word locations. An internal address register, latches the address information on the positive to negative transition of memory enable. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of memory enable, and (t_{HA}) after the positive to negative transition of memory enable. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if write enable goes low while memory enable is low. Write enable must be held low for t_{WE} and data must remain stable t_{HD} after write enable returns high.

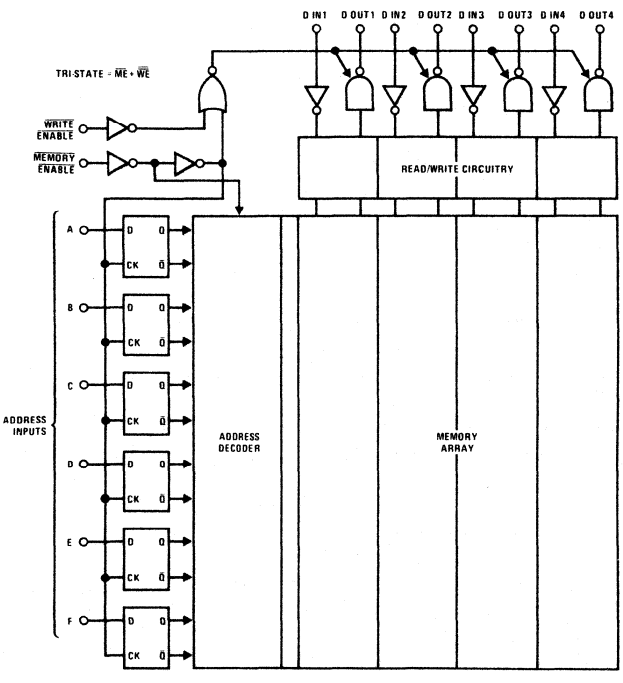
Read Operation: Data is nondestructively read from a memory location by an address operation with write enable held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

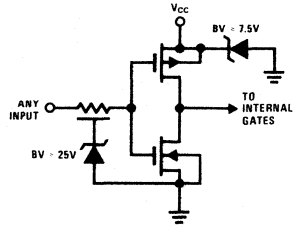
features

- Supply voltage range — 3V to 5.5V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250 nW/package typ (chip enabled or disabled)
- Fast access time — 250 ns typ at 5V
- TRI-STATE outputs
- High voltage inputs

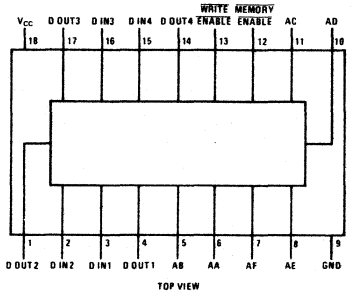
logic and connection diagrams



Input Protection



Dual-In-Line Package



Order Number MM54C910D or MM74C910D
See NS Package D18A

Order Number MM74C910N
See NS Package N18A

absolute maximum ratings (Note 1)

Voltage At Any Output Pin	−0.3V to V_{CC} +0.3V
Voltage At Any Input Pin	−0.3V to +15V
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 5.5V
Standby V_{CC} Range	1.5V to 5.5V
Absolute Maximum V_{CC}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

dc electrical characteristics MM54C910/MM74C910

(Min/max limits apply across the temperature and power supply range indicated).

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 15V		0.005	2	μA
		V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −150μA	V_{CC}−0.5			V
		I_O = −400μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
	Output Current in High	V_O = 5V		0.005	1	μA
	Impedence State	V_O = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V		0.05	300	μA

ac electrical characteristics MM54C910/MM74C910

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

	PARAMETER	MIN	TYP	MAX	UNITS
t_{ACC}	Access Time from Address		250	500	ns
t_{PD}	Propagation Delay from $\overline{ME}$		180	360	ns
t_{SA}	Address Input Set-Up Time	140	70		ns
t_{HA}	Address Input Hold Time	20	10		ns
t_{ME}	Memory Enable Pulse Width	200	100		ns
$t_{\overline{ME}}$	Memory $\overline{\text{Enable}}$ Pulse Width	400	200		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{OH}	Delay to TRI-STATE (Note 4)		100	200	ns
	CAPACITANCE				
C_{IN}	Input Capacity				
	Any Input (Note 2)		5		pF
C_{OUT}	Output Capacity				
	Any Output (Note 2)		9		pF
C_{PD}	Power Dissipation Capacity (Note 3)		350		pF

ac electrical characteristics (con't)

C_L = 50 pF

PARAMETER		MM54C910 T_A = −55°C to +125°C V_{CC} = 4.5V to 5.5V		MM74C910 T_A = −40°C to +85°C V_{CC} = 4.75V to 5.25V		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time from Address		860		700	ns
t_{PD1}, t_{PD0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
t_{WE}	$\overline{\text{Write Enable}}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

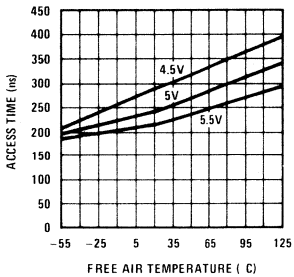
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: See ac test circuit for t_{1H}, t_{0H}.

typical performance characteristics

Typical Access Time vs Ambient Temperature

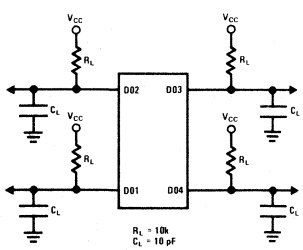


truth table

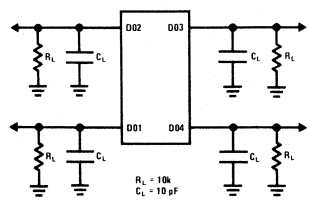
$\overline{ME}$	$\overline{WE}$	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

ac test circuits

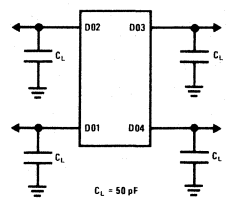
t_{0H}



t_{1H}

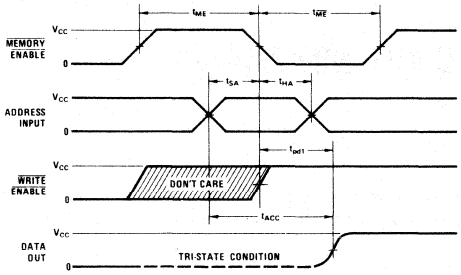


All Other AC Tests

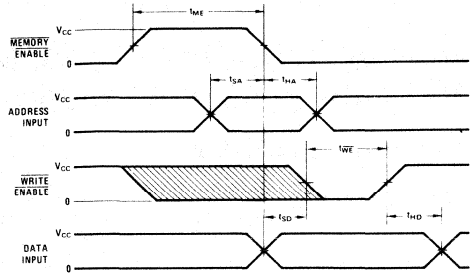


switching time waveforms

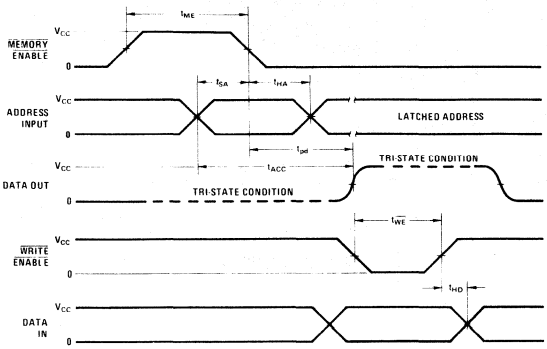
Read Cycle
(See Note 1)



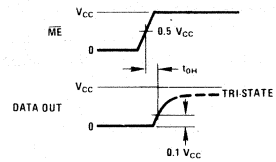
Write Cycle
(See Note 1)



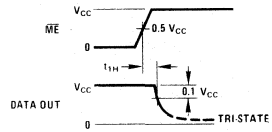
Read Modify Write Cycle
(See Note 1)



t_{0H}



t_{1H}



Note 1: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} nanoseconds between every address change.
Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

CMOS RAMs

MM54C920/MM74C920, MM54C921/MM74C921 1024-Bit (256 × 4) Static RAM

General Description

The MM54C920/MM74C920 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs, $\overline{CES}$ and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads thereby is reduced to 18.

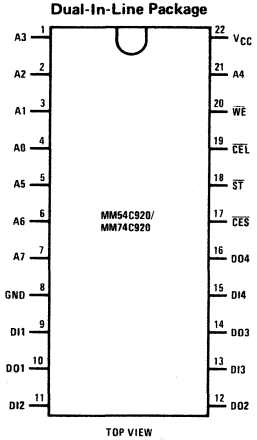
Complete address decoding as well as 2-chip select functions, $\overline{CEL}$ and $\overline{CES}$, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make these RAMs ideal elements for use in microprocessor, minicomputer as well as main frame memory applications.

Features

- 256 x 4-bit organization
- Access time
  - 250 ns max MM74C920, MM74C921
  - 275 ns max MM54C920, MM54C921
  - 300 ns max MM74C921-3
- TRI-STATE outputs
- Low power
- On-chip registers
- Single 5V supply
- Data retained with V_{CC} as low as 2V

Connection Diagrams

Dual-In-Line Package



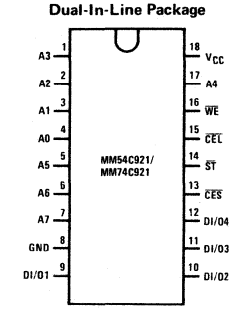
TOP VIEW

Order Number MM54C920D, MM74C920D or MM74C920D-3
See NS Package D22B

Order Number MM54C920J, MM74C920J or MM74C920J-3
See NS Package J22A

Order Number MM74C920N or MM74C920N-3
See NS Package N22A

Dual-In-Line Package



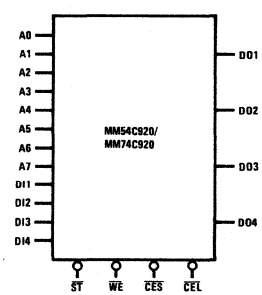
TOP VIEW

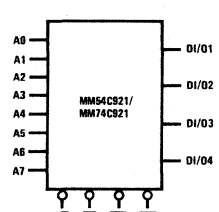
Order Number MM54C921D, MM74C921D or MM74C921D-3
See NS Package D18A

Order Number MM54C921J, MM74C921J or MM74C921J-3
See NS Package J18A

Order Number MM74C921N or MM74C921N-3
See NS Package N18A

Logic Symbols





Functional Description

The functional description will reference the logic diagram of the MM54C920/MM74C920 shown in *Figure 1*. Input addresses and $\overline{CES}$ are clocked into the input latches by the falling edge of $\overline{STROBE}$. Input set-up and hold times must be observed on these signals (see timing diagrams). The true and complement address information is fed to the row and column decoders which access the selected 4-bit memory word.

The addressed word (4 bits) is fed to 4 sense amplifiers through the column decoders. The information from the sense amplifiers is latched into the output register when $\overline{STROBE}$ rises. The register drives the TRI-STATE output buffers.

Chip select inputs, $\overline{CEL}$ and $\overline{CES}$, have identical functions except that $\overline{CES}$ (Chip Enable Stored) is clocked into a latch on the falling edge of $\overline{STROBE}$; $\overline{CEL}$ (Chip Enable Level) is not.

Note that set-up and hold times must be observed on $\overline{CES}$. Because $\overline{CEL}$ is not clocked by $\overline{STROBE}$, it may fall after $\overline{STROBE}$ has fallen without affecting access time provided that the t_{OE} requirement is met.

The outputs are in a high impedance state when the chip is not selected ($\overline{CES}$ or $\overline{CEL}$ high) or when writing ($\overline{WE}$ low). Note that the information stored in the output latches will be changed whenever $\overline{STROBE}$ falls, regardless of the logic states of $\overline{WE}$, $\overline{CEL}$ or $\overline{CES}$.

The switching time waveforms in *Figures 2, 3 and 4* define the read, write, and output enable/disable parameters respectively.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, $\overline{ST}$ logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram*

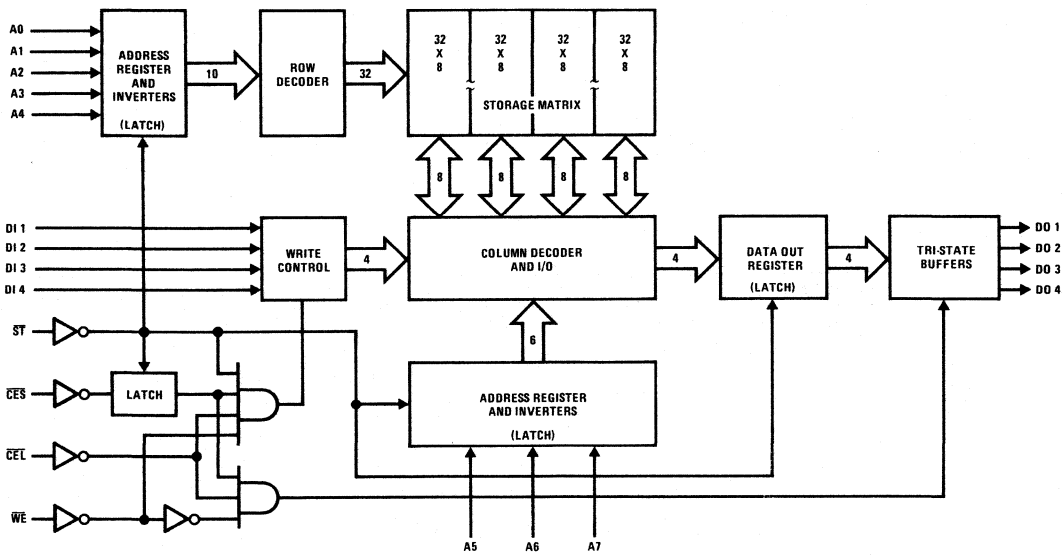


FIGURE 1. MM54C920/MM74C920

*The logic diagram for the MM54C921/MM74C921 is identical to this except that data inputs (DI1–DI4) are connected to data outputs (DO1–DO4).

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C920, MM54C921	4.5	5.5	V
MM74C920, MM74C921	4.5	5.5	V
MM74C920-3, MM74C921-3	4.75	5.25	V
Ambient Temperature (T_A)			
MM54C920, MM54C921	−55	+125	°C
MM74C920, MM74C921	−40	+85	°C
MM74C920-3, MM74C921-3	0	+70	°C

DC Electrical Characteristics (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MM54C920 MM54C921		MM74C920 MM74C921		MM74C920–3 MM74C921–3		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V_{CC}−1.5	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.1		V_{CC}−0.1		V_{CC}−0.1		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, $\overline{CEL} = V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_{CC}	Supply Leakage Current	$V_{IN} = V_{CC}$, $\overline{ST}$ = 0V, V_O = 0V		20		10		100	μA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	$\overline{CEL} = V_{CC}$ = 2V, Typical at 25°C		0.01(typ)		0.01(typ)		0.01(typ)	μA

Capacitance (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		4	7	pF
C_O	Output Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		6	9	pF
$C_{I/O}$	Data Input/Output Capacitance	MM54C921/MM74C921 Only		8	12	pF

Note 1: "Absolute Maximum Ratings" are those values above which the device may be permanently damaged. They do not mean the device may be operated at these values.

Note 2: These limits apply over the entire operating range specified in the "Operating Conditions" unless otherwise stated.

Note 3: $\overline{CEL} = V_{CC} - 2V$ or = 2V, whichever is greater.

Note 4: Capacitance is guaranteed by periodic testing.

Truth Table

$\overline{ST}$	$\overline{CES}$*	$\overline{CEL}$	$\overline{WE}$	DI*	FUNCTION
X	X	1	X	X	Output in Hi-Z state
0	1	X	X	X	Output in Hi-Z state
X	X	X	0	X	Output in Hi-Z state
0	0	0	0	0	Write "0", output in Hi-Z state
0	0	0	0	1	Write "1", output in Hi-Z state
0	0	0	1	X	Read data, output enabled

*Set-up and hold times must be met
X = don't care

AC Electrical Characteristics (Note 5)

SYMBOL	PARAMETER	MM54C920 MM54C921		MM74C920 MM74C921		MM74C920–3 MM74C921–3		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		275		250		325	ns
t_{ACS}	Access Time From Strobe		250		225		300	ns
t_{AS}	Address Set-Up Time	25		25		25		ns
t_{AH}	Address Hold Time	25		25		25		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{ST}}$	$\overline{ST}$ Pulse Width (Negative)	150		130		165		ns
t_{ST}	ST Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time	100		90		90		ns
t_{DH}	Data Hold Time	60		60		60		ns

Note 5: These limits apply over the operating range specified in the "Operating Conditions" with $t_{RISE} = t_{FALL} = 5$ ns, load = 1 TTL gate + 50 pF.

Switching Time Waveforms

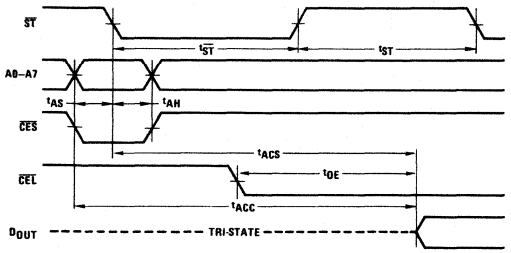
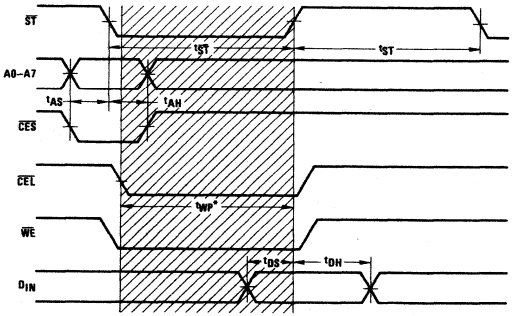
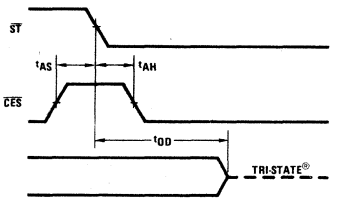


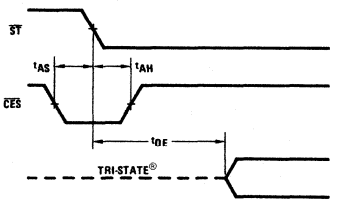
FIGURE 2. Read Cycle ($\overline{WE}$ = V_{IH})



*t_{WP} (the Write Pulse Width) is the time $\overline{ST}$, $\overline{CEL}$ and $\overline{WE}$ are coincidentally low

FIGURE 3. Write Cycle





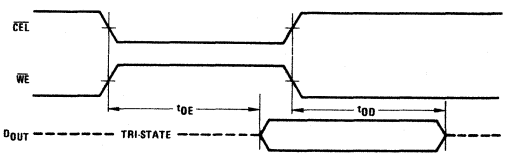
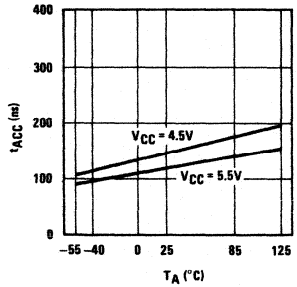


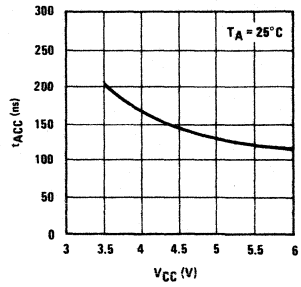
FIGURE 4. Output Enable/Disable

Typical Performance Characteristics

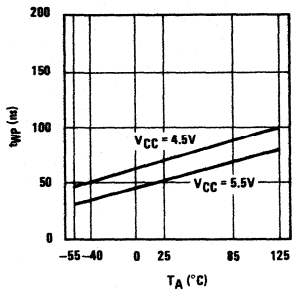
Access Time vs Ambient Temperature



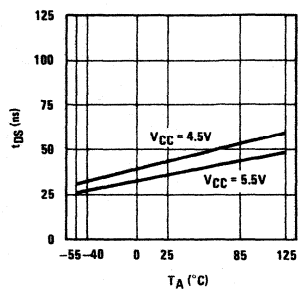
Access Time vs Power Supply Voltage



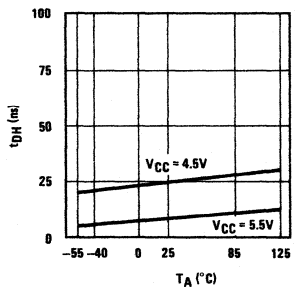
Minimum Write Pulse Width vs Ambient Temperature



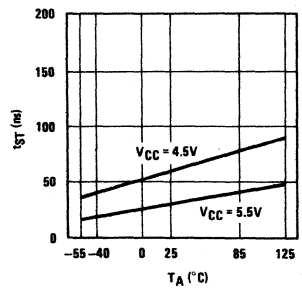
Data-In Setup Time vs Ambient Temperature



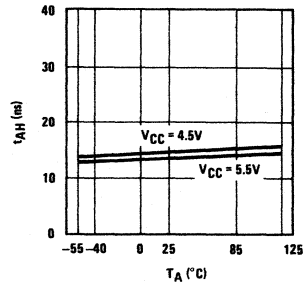
Data In Hold Time vs Ambient Temperature



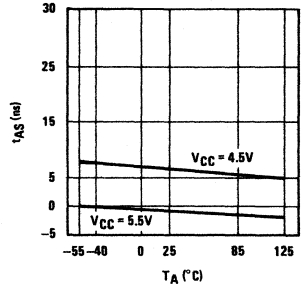
Minimum ST Pulse Width (Positive) vs Ambient Temperature



Address Hold Time vs Ambient Temperature

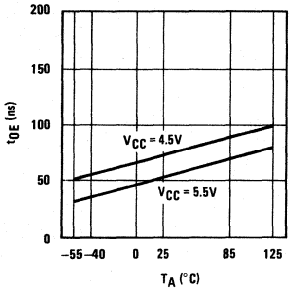


Address Setup Time vs Ambient Temperature

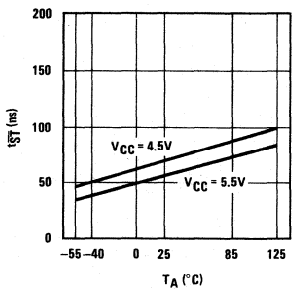


Typical Performance Characteristics (Continued)

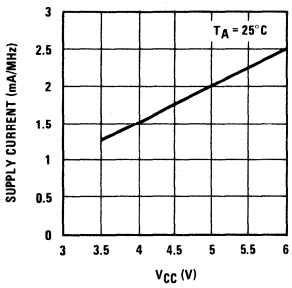
Output Enable Time vs Ambient Temperature



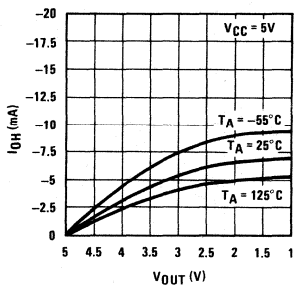
Minimum $\overline{ST}$ Pulse Width (Negative) vs Ambient Temperature



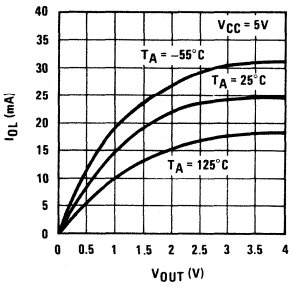
Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, V_{IL} = 0V)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



National Semiconductor

MM54C929/MM74C929, MM54C930/MM74C930 1024-Bit (1024 × 1) Static RAMs

General Description

The MM54C929/MM74C929 and the MM54C930/MM74C930 1024 x 1 random access read/write memories are manufactured using silicon-gate CMOS technology. These RAMs are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input $\overline{CS1}$ serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, 3-chip select functions (MM54C930/MM74C930) and TRI-STATE® output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are internally connected together, providing a single chip-select input $\overline{CS}$.

Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor, minicomputer and main-frame-memory applications.

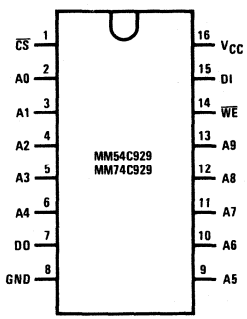
Features

- Fast access—250 ns max
- TRI-STATE outputs
- Low power—10 μA max standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with V_{CC} as low as 2V
- Can be operated common I/O

3

Connection Diagrams

Dual-In-Line Package



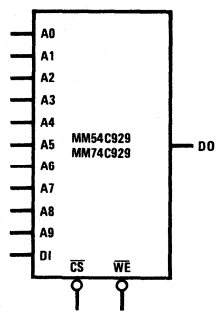
TOP VIEW

Order Number MM54C929D, MM74C929D or MM74C929D-3
See NS Package D16C

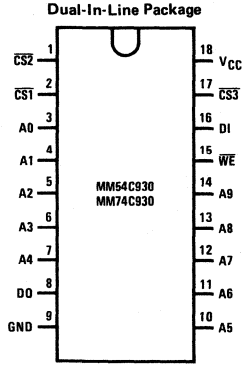
Order Number MM54C929J, MM74C929J or MM74C929J-3
See NS Package J16A

Order Number MM74C929N or MM74C929N-3
See NS Package N16A

Logic Symbols



Dual-In-Line Package

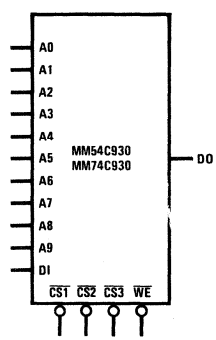


TOP VIEW

Order Number MM54C930D, MM74C930D or MM74C930D-3
See NS Package D18A

Order Number MM54C930J, MM74C930J or MM74C930J-3
See NS Package J18A

Order Number MM74C930N or MM74C930N-3
See NS Package N18A



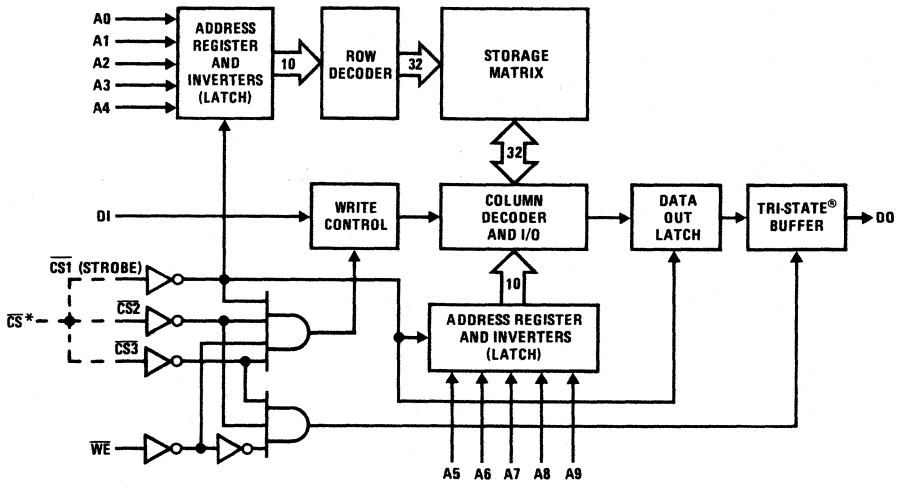
Functional Description

Address inputs are clocked into the input latches by the falling edge of chip strobe $\overline{CS1}$; set-up and hold times must be observed on these input signals (see timing diagram). The true and complement address information is fed to the row and column decoders which select one of the 1024-bit locations. The addressed bit is fed, via a sense amplifier, to the output register and TRI-STATE buffer. The information is latched into the output register on the rising edge of chip strobe $\overline{CS1}$. The output is in a high impedance state when the chip is not selected ($\overline{CS2}$ or $\overline{CS3}$ high) or when writing ($\overline{WE}$ low). Output buffer control is independent of chip strobe $\overline{CS1}$.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, strobe ($\overline{CS}$ for the MM74C929 and $\overline{CS1}$ for the MM74C930) logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram*



*The MM74C930 has 3 chip selects $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$. The MM74C929 has these internally connected together providing a single chip select input $\overline{CS}$.

FIGURE 1

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
MM54C929, MM54C930	−55°C to +125°C
MM74C929, MM74C930	−40°C to +85°C
MM74C929-3, MM74C930-3	0°C to +70°C
Package Dissipation	500 mW
Lead Temperature (Soldering 10 seconds)	300°C

DC Electrical Characteristics V_{CC} = 5V ±10%, T_A = Operating Range, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = 1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.1		V_{CC}−0.1		V_{CC}−0.1		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2.0 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \le V_{IN} \le V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_O	Output Leakage	$0V \le V_O \le V_{CC}$, (Note 2)	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_{CC}	Supply Leakage Current	$V_{IN} = V_{CC}$, V_O = 0V		20		10		100	μA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	V_{CC} = 2V, T_A = 25°C, (Note 2)		0.01 (typ)		0.01 (typ)		0.1 (typ)	μA

Note 1: V_{CC} = 5V ±5%.
Note 2: $\overline{CS2} = \overline{CS3} = V_{CC}$ or $\overline{CS} = V_{CC}$.
Note 3: $\overline{CS2}$ or $\overline{CS3}$ or $\overline{CS} = V_{CC} - 2V$ or = 2V, whichever is greater.

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = Operating Range, unless otherwise noted

TTL Interface ($V_{IH} = V_{CC} - 2V$, V_{IL} = 0.8V, Input $t_{RISE} = t_{FALL}$ = 5 ns, Load = 1 TTL Gate + 50 pF)

SYMBOL	PARAMETER	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		265		240		315	ns
t_{ACS},t_{ACS1}	Access Time From $\overline{CS}$, $\overline{CS1}$		250		225		300	ns
t_{AS}	Address Set-Up Time	15		15		15		ns
t_{AH}	Address Hold Time	50		50		50		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{CS}}$,$t_{\overline{CS1}}$ (Note 4)	$\overline{CS}$, $\overline{CS1}$ Pulse Width (Negative)	150		130		165		ns
t_{CS},t_{CS1}	$\overline{CS}$, $\overline{CS1}$ Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time, (Note 5)	150		140		140		ns
t_{DH}	Data Hold Time, (Note 5)	0		0		0		ns

Note 4: Greater than minimum $\overline{CS}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation.

Note 5: t_{DS} and t_{DH} are referenced to the low-to-high transition of $\overline{CS1}$ or $\overline{CS2}$ or $\overline{CS3}$ or $\overline{WE}$, whichever switches first, for the MM54C930/MM74C930 and are referenced to the $\overline{CS}$ or $\overline{WE}$ low-to-high transition, whichever switches first, for the MM54C929/MM74C929.

Capacitance (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0, f = 1 MHz, T_A = 25°C	4	7	pF
C_O	Output Capacitance	V_{IN} = 0, f = 1 MHz, T_A = 25°C	6	9	pF
$C_{\overline{CS}}$	Chip Select Capacitance	MM54C929/MM74C929, MM74C929-3	8	12	pF

Note 6: Capacitance maximum is guaranteed by periodic testing.

Truth Tables

MM54C929/MM74C929

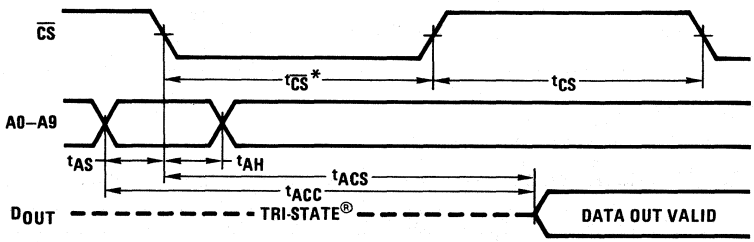
$\overline{CS}$	$\overline{WE}$	DI	FUNCTION
1	X	X	Output in Hi-Z State
X	0	X	Output in Hi-Z State
0	0	0	Write "0," Output in Hi-Z State
0	0	1	Write "1," Output in Hi-Z State
0	1	X	Read Data, Output Enabled

X = Don't care

MM54C930/MM74C930

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{WE}$	DI	FUNCTION
X	1	X	X	X	Output in Hi-Z State
X	X	1	X	X	Output in Hi-Z State
X	X	X	0	X	Output in Hi-Z State
0	0	0	0	0	Write "0," Output in Hi-Z State
0	0	0	0	1	Write "1," Output in Hi-Z State
0	0	0	1	X	Read Data, Output Enabled

Switching Time Waveforms



*Greater than minimum $\overline{CS}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation, *(Figure 4a)*.

FIGURE 2a. MM54C929/MM74C929 Read Cycle

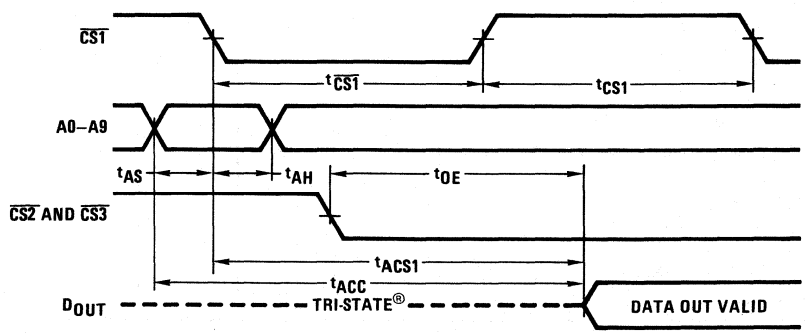
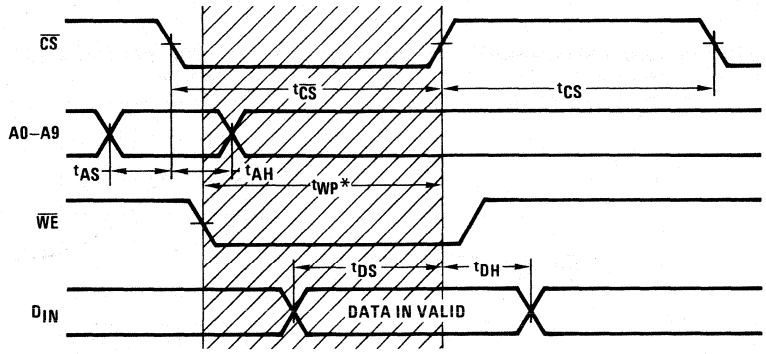


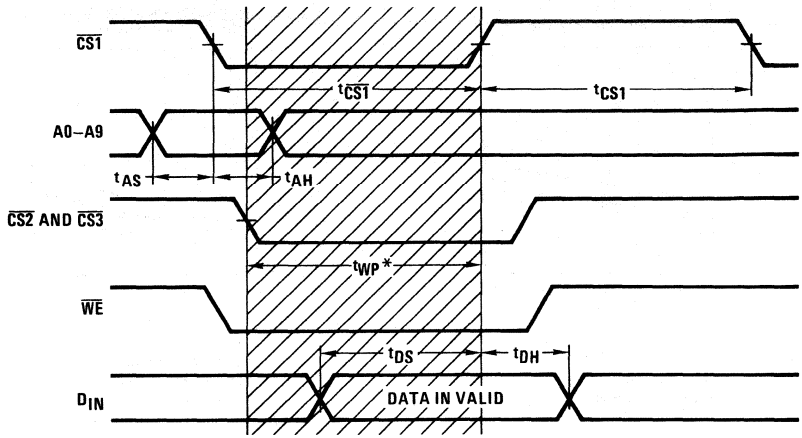
FIGURE 2b. MM54C930/MM74C930 Read Cycle

Switching Time Waveforms (Continued)



*t_{WP} (the Write Pulse width) is the time $\overline{CS}$ and $\overline{WE}$ are coincidentally low

FIGURE 3a. MM54C929/MM74C929 Write Cycle



*t_{WP} (the Write Pulse width) is the time $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{WE}$ are coincidentally low

FIGURE 3b. MM54C930/MM74C930 Write Cycle

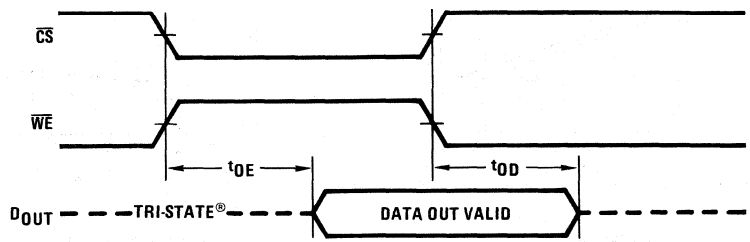


FIGURE 4a. MM54C929/MM74C929

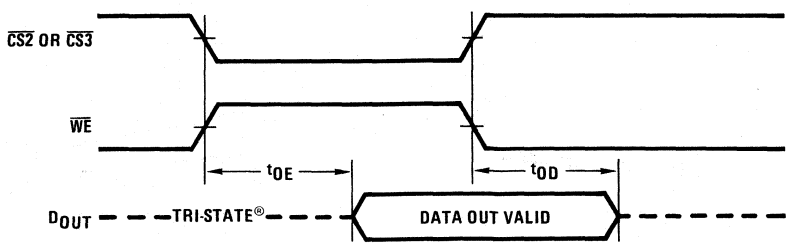
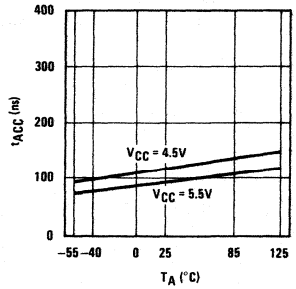


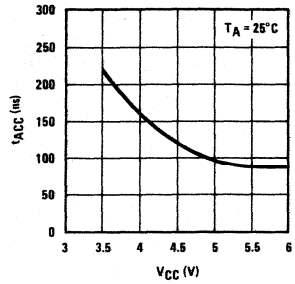
FIGURE 4b. MM54C930/MM74C930

Typical Performance Characteristics

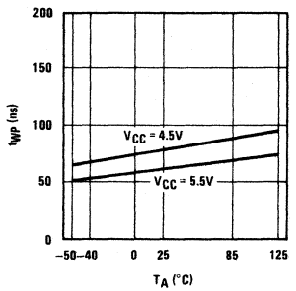
Access Time vs Ambient Temperature



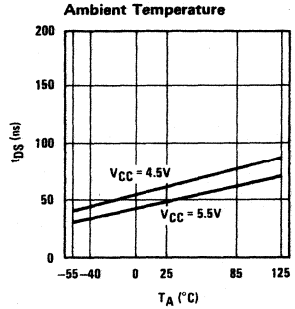
Access Time vs Power Supply Voltage



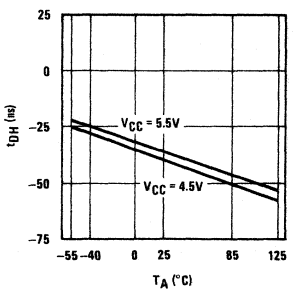
Minimum Write Pulse Width vs Ambient Temperature



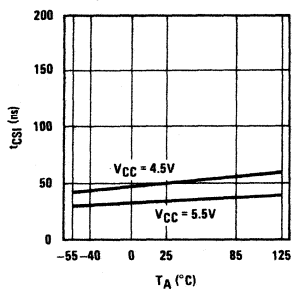
Data-In Set-Up Time vs Ambient Temperature



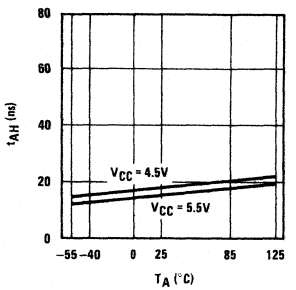
Data-In Hold Time vs Ambient Temperature



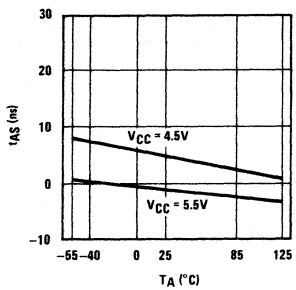
Minimum $\overline{CS}$I Pulse Width (Positive) vs Ambient Temperature



Address Hold Time vs Ambient Temperature

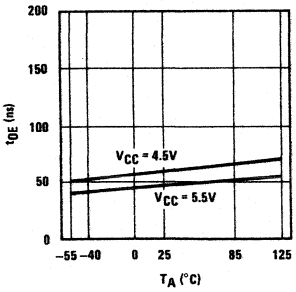


Address Set-Up Time vs Ambient Temperature

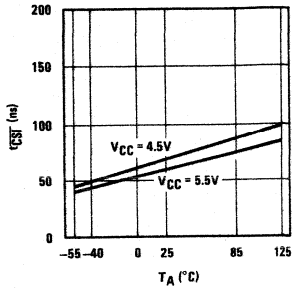


Typical Performance Characteristics (Continued)

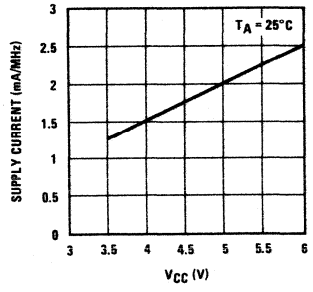
Output Enable Time vs Ambient Temperature



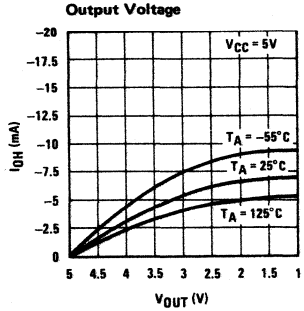
Minimum $\overline{CS1}$ Pulse Width (Negative) vs Ambient Temperature



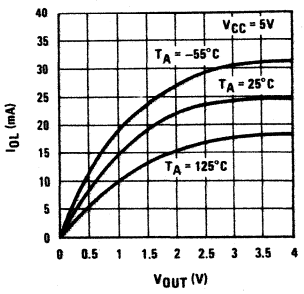
Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, V_{IL} = 0V)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



Section 4

Charge Coupled Devices

4

Recent advances in NMOS technology have made it possible to produce charge coupled devices of 65,536 bit density. These devices offer a new set of points in the tradeoff matrix used to optimize system cost/performance/bit density. For example, a "disk-cache" approach may now be practical for minicomputer secondary storage. National's memory line includes the MM2464, organized 256 x 256 for a broad range of applications. Consult your National representative if you need applications or other assistance.

National Semiconductor

Charge Coupled Devices
PRELIMINARY

MM2464 65,536-Bit CCD TTL Compatible (Charge Coupled Device)

General Description

The MM2464 is a TTL compatible 65,536-bit CCD (Charge Coupled Device) memory organized as 256 recirculating shift registers 256 bits in length. The output of each of the 256 charge coupled loops is accessible via an 8-bit address port at a 2.5 MHz rate. Two clock inputs (SE and SYNC) shift all 256 loops simultaneously at rates up to 1 MHz. The short loop length allows an average latency time of 130 μs.

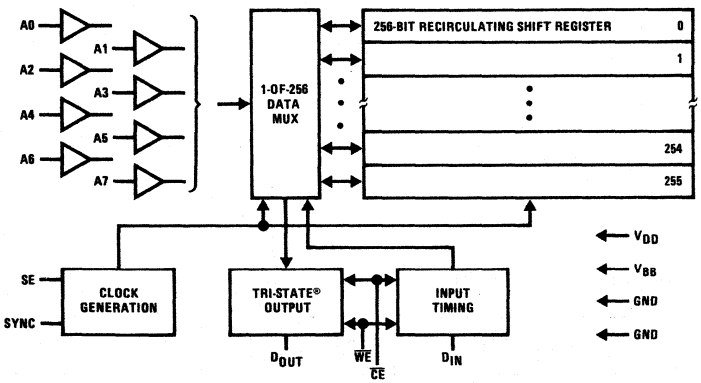
The MM2464 may be used in either a page or serial mode for Read or Write. Clock speeds may be kept at a low level while in page mode or during refresh, thus reducing power dissipation. A high speed shift or search mode may be used for optimum latency times. Subsequent to applying power, 10,000 shift cycles are required to stabilize internal voltage references. Thereafter, these references are maintained by normal operation of the device.

The MM2464 is manufactured using a modified version of National's N-channel silicon gate process used for 16k dynamic R/W memories.

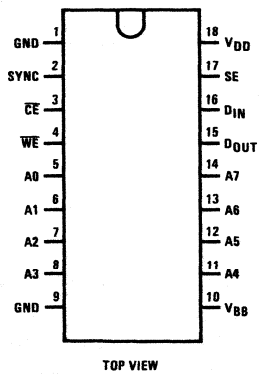
Features

- TTL compatible input and output levels on all I/O lines and clocks
- Standard 0.3 inch width 18-pin package
- TRI-STATE® output
- Pin and function compatible with Intel 2464
- Page mode operation at 285 ns access time
- Short latency time (130 μs average)
- High data rate (2.5 MHz)

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM2464D
See NS Package D18A

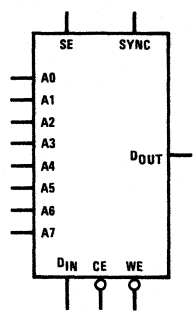
Truth Table

$\overline{CE}$	$\overline{WE}$	OPERATION	OUTPUT STATE
H	X	Deselected	Hi-Z
L	L	Output Disabled	Hi-Z
L	↑	Write	Hi-Z
L	H	Read	Data Out

Pin Description

A0–A7	Address inputs
D_{IN}	Data in
D_{OUT}	Data out
$\overline{WE}$	Write enable
$\overline{CE}$	Chip enable
SE	Sense enable
SYNC	Synchronize
V_{DD}	12V
V_{BB}	−5V
GND	Ground

Logic Symbol



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin Except V_{BB}	−0.3V to +16V
V_{DD} and GND with Respect to V_{BB}	−0.3V to +20V
Operating Temperature Range	0°C to +70°C
Temperature under Bias	−10°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating temperature range, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
I_{IL}	Low Level Input Current	$V_{IL\ MIN} \leq V_{IL} \leq V_{IL\ MAX}$	−10	±1	10	μA
I_{IH}	High Level Input Current	$V_{IH\ MIN} \leq V_{IH} \leq V_{IH\ MAX}$	−10	±1	10	μA
I_{LO}	Output Leakage Current	$GND \leq V_{OUT} \leq 5V$	−10	±1	10	μA
V_{IL}	Input Low Voltage	All Inputs	−0.3		0.8	V
V_{IH}	Input High Voltage	All Inputs	2.2		5.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		5.5	V

Capacitance Characteristics T_A = 25°C, f = 1.0 MHz (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
C_{IN}	Input Capacitance	All Inputs V_{IN} = 0V		5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Typical characteristics are for V_{DD} = 12V, V_{BB} = −5V, T_A = 25°C and specified loading.

Operating Power Characteristics

T_A within operating temperature range, V_{DD} = 12 ±5%, V_{BB} = −5 ±5%.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
$I_{DD\ AVG}$	Average Operating V_{DD} Supply Current	(Note 4)				mA
I_{DD1}	I_{DD} Component Relating to $\overline{CE}$			11	18	mA
I_{DD2}	I_{DD} Component Relating to SE Frequency			25	38	mA/MHz
I_{DD3}	I_{DD} Component Relating to $t_{SSY\ 1}$			0.9	1.5	mA
I_{DD4}	I_{DD} Constant Current Drain Component			2.8	4.5	mA
I_{BB1}	V_{BB} Standby Current			5	50	μA
I_{BB2}	V_{BB} Average Active Current			200	400	μA

Note 4: $I_{DD\ AVG}$ is dependent on system configuration and may be determined through the use of the equation below.

$$I_{DD\ AVG} = \frac{T_{CE}}{T} I_{DD1} + \frac{N}{T} I_{DD2} + \frac{T_{SSY\ 1}}{T} I_{DD3} + I_{DD4}$$

Where:

T is an arbitrary time period reflecting all modes of device operation over which the waveform is cyclic.

$\frac{T_{CE}}{T} I_{DD1}$ represents the current drained by enabling the device. T_{CE} is the total time $\overline{CE}$ is active.

$\frac{N}{T} I_{DD2}$ represents the current drained during clocking of the device. N is the number of times SE is pulsed during period T.

$\frac{T_{SSY\ 1}}{T} I_{DD3}$ is directly proportional to the percentage of time between the rising edge of the SE pulse preceding SYNC and the rising edge of SYNC. It is therefore advisable to keep this time to a minimum within the limits expressed in this data sheet.

I_{DD4} represents the constant current drain of the MM2464.

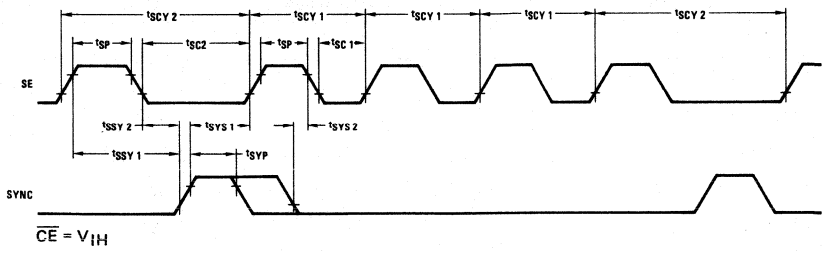
AC Electrical Characteristics T_A within operating temperature range, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SEARCH OR REFRESH MODE						
t_{SCY1}	SE Cycle Time with No SYNC Pulse, (Note 5)	Input Pulse Levels = 0.4V and 2.4V, Input Rise and Fall Times = 10 ns, Input and Output Timing Levels = 0.8V and 2.2V, Output Load = 1 TTL Gate Plus C_L = 100 pF	750		10^5	ns
t_{SCY2}	SE Cycle Time with SYNC Pulse		1000		10^5	ns
t_{SP}	SE Pulse Width		630			ns
t_{SC1}	SE OFF Time with No SYNC Pulse, (Note 5)		100			ns
t_{SC2}	SE OFF Time with SYNC Pulse		350			ns
t_{SSY1}	SE ON to SYNC ON Time				10^5	ns
t_{SSY2}	SE OFF to SYNC ON Time		0			ns
t_{SYS1}	SYNC ON to SE ON Time, (Note 6)		340		TBD	ns
t_{SYS2}	SYNC OFF to SE OFF Time		50			ns
t_{SYP}	SYNC Pulse Width		150			ns
t_{REF}	Time Between Refresh (256 SE Cycles), (Note 6)				TBD	ms
PAGE OR SERIAL MODE						
t_{SCY1}	SE Cycle Time with No SYNC Pulse	Input Pulse Levels = 0.4V and 2.4V, Input Rise and Fall Times = 10 ns, Input and Output Timing Levels = 0.8V and 2.2V, Output Load = 1 TTL Gate Plus C_L = 100 pF	750		10^5	ns
t_{SCY2}	SE Cycle Time with SYNC Pulse		1000			ns
t_{SP}	SE Pulse Width		630			ns
t_{SC1}	SE OFF Time with No SYNC Pulse		100			ns
t_{SC2}	SE OFF Time with SYNC Pulse		350			ns
t_{SSY1}	SE to SYNC ON Time				10^5	ns
t_{SSY2}	SE OFF to SYNC ON Time		0			ns
t_{SYS1}	SYNC ON to SE ON Time, (Note 6)		340		TBD	ns
t_{SYS2}	SYNC OFF to SE OFF Time		50			ns
t_{SYP}	SYNC Pulse Width		150			ns
t_{SCE}	SE ON to $\overline{CE}$ ON		355			ns
t_{CESY}	$\overline{CE}$ OFF to SYNC ON Time		0			ns
t_{CES}	$\overline{CE}$ OFF to SE ON Time		0			ns
t_{REF}	Time Between Refresh (256 SE Cycles) (Note 6)				TBD	ms

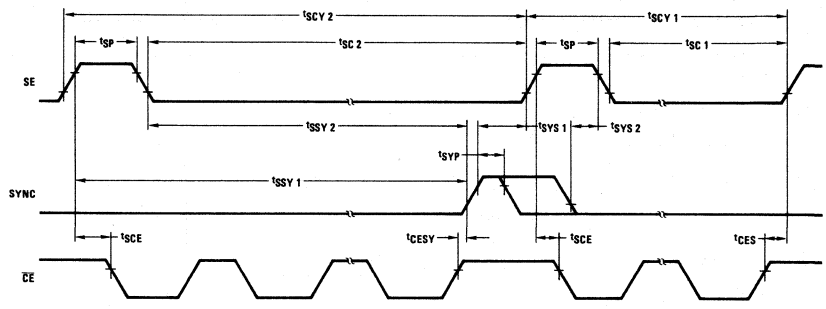
Note 5: To achieve constant 1 MHz operation set; $t_{SCY\,1} = t_{SCY\,2} = 1000$ ns and, $t_{SC\,1} = t_{SC\,2} = 350$ ns.
Note 6: TBD = to be determined. For a preliminary design parameter, use t_{REF} = 2 ms.

Switching Time Waveforms

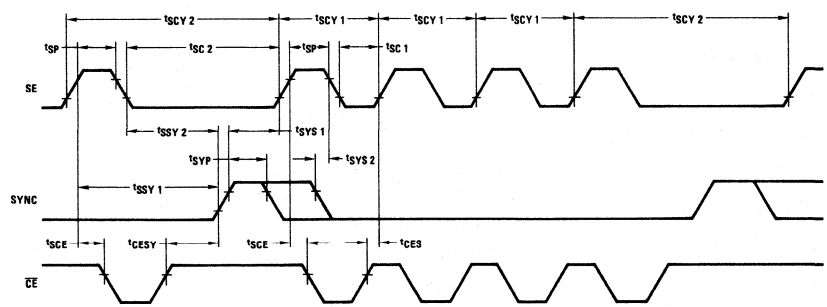
Search or Refresh Mode



Page Mode



Serial Mode



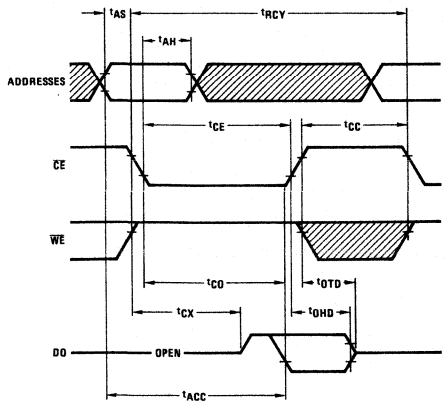
AC Electrical Characteristics (Continued)

T_A within operating range, V_{DD} = 12 ±5%, V_{BB} = −5 ±5%

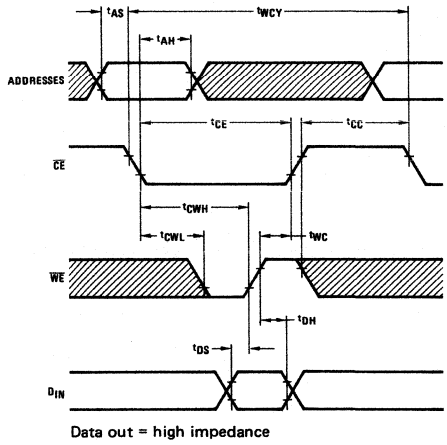
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ CYCLE						
t_{ACC}	Address to Output Access Time				285	ns
t_{RCY}	Read Cycle Time		400			ns
t_{AS}	Address Set-Up Time		0			ns
t_{AH}	Address Hold Time	Input Pulse Levels = 0.4V and 2.4V,	80			ns
t_{CE}	$\overline{CE}$ ON Time	Input Rise and Fall Times = 10 ns,	285			ns
t_{CC}	$\overline{CE}$ OFF Time	Input and Output Timing Levels =	95			ns
t_{CX}	$\overline{CE}$ to Output Active	0.8V and 2.2V, Output Load =	10			ns
t_{CO}	$\overline{CE}$ to Output Valid	1 TTL Gate Plus C_L = 100 pF			275	ns
t_{OHD}	Output Hold from Deselect		10			ns
t_{OTD}	Output Hi-Z from Deselect				60	ns
WRITE CYCLE						
t_{WCY}	Write Cycle Time		400			ns
t_{AS}	Address Set-Up Time		0			ns
t_{AH}	Address Hold Time		80			ns
t_{CE}	$\overline{CE}$ ON Time	Input Pulse Levels = 0.4V and 2.4V,	285			ns
t_{CC}	$\overline{CE}$ OFF Time	Input Rise and Fall Times = 10 ns,	95			ns
t_{CWL}	$\overline{CE}$ to $\overline{WE}$ Low	Input and Output Timing Levels =			10	ns
t_{CWH}	$\overline{CE}$ to $\overline{WE}$ High	0.8V and 2.2V, Output Load =	155			ns
t_{WC}	Write to $\overline{CE}$ OFF Time	1 TTL Gate Plus C_L = 100 pF	100			ns
t_{DS}	Data Set-Up Time		0			ns
t_{DH}	Data Hold Time		80			ns
READ-MODIFY-WRITE CYCLE						
t_{ACC}	Address to Output Access Time				285	ns
t_{RWC}	RMW Cycle Time		600			ns
t_{AS}	Address Set-Up Time		0			ns
t_{AH}	Address Hold Time		80			ns
t_{CRW}	$\overline{CE}$ Width During RMW		485			ns
t_{CC}	$\overline{CE}$ OFF Time	Input Pulse Levels = 0.4V and 2.4V,	95			ns
t_{CX}	$\overline{CE}$ to Output Active	Input Rise and Fall Times = 10 ns,	10			ns
t_{CO}	$\overline{CE}$ to Output Valid	Input and Output Timing Levels =			275	ns
t_{OHW}	Output Hold From $\overline{WE}$	0.8V and 2.2V, Output Load =	10			ns
t_{OTW}	Output Hi-Z from $\overline{WE}$	1 TTL Gate Plus C_L = 100 pF			60	ns
t_{WP}	Write Pulse Width		100			ns
t_{WC}	Write to $\overline{CE}$ OFF Time		100			ns
t_{DS}	Data Set-Up Time		0			ns
t_{DH}	Data Hold Time		80			ns

Switching Time Waveforms (Continued)

Read Cycle

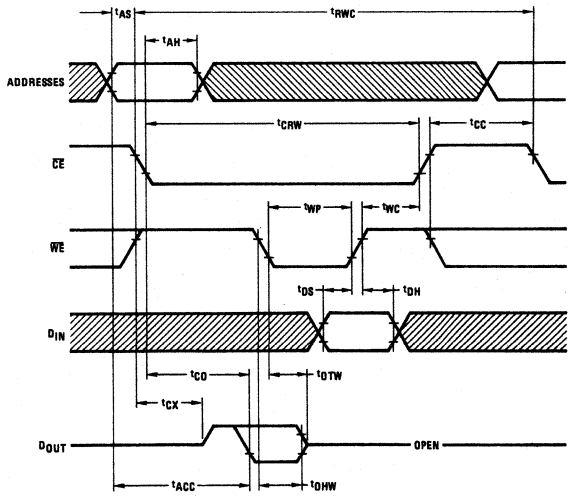


Write Cycle



Data out = high impedance

Read-Modify-Write Cycle



Section 5

MOS EPROMs

5

Customer-reprogrammable read-only memory has made a remarkable impact upon the art of logic design. National's EPROMs make practical new applications of microprocessors. National is a volume production source of the products included here, and is developing larger EPROMs for tomorrow's applications.

National Semiconductor

MM1702A 2048-Bit (256 × 8) UV Erasable PROM

general description

The MM1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The MM1702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The MM1702AQ is packaged in a 24-pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The MM1702AD is packaged in a 24-pin dual-in-line package with a metal lid and is not erasable.

The circuitry of the MM1702A is entirely static; no clocks are required.

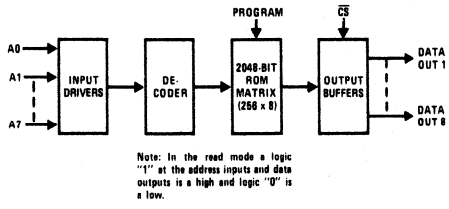
A pin-for-pin metal mask programmed ROM, the MM1302 is ideal for large volume production runs of systems initially using the MM1702A.

The MM1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

features

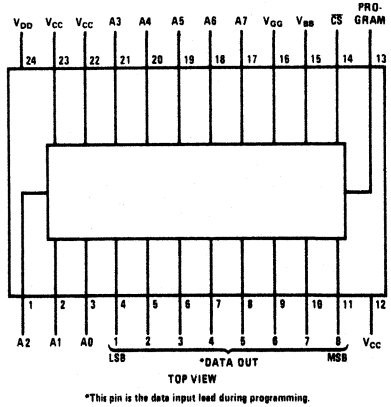
- Fast programming—30 seconds for all 2048 bits
- All 2048 bits guaranteed programmable—100% factory tested
- Fully decoded, 256 x 8 organization
- Static MOS—no clocks required
- Inputs and outputs DTL and TTL compatible
- TRI-STATE® output—OR-tie capability
- Simple memory expansion—chip select input lead
- Direct replacement for the Intel 1702A

block and connection diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



*This pin is the data input lead during programming.

Order Number MM1702AQ
See NS Package J24C

Pin Names

A0—A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT\,1} - D_{OUT\,8}$	Data Outputs

Pin Connections*

MODE/PIN	12 (V_{CC})	13 (PROGRAM)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

*The external lead connections to the MM1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1—8 are pins 4—11 respectively.

absolute maximum ratings (Note 1)

Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Power Dissipation	2W
Read Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	+0.5V to −20V
Program Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	−48V
Lead Temperature (Soldering, 10 seconds)	300°C

read operation dc characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C. (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Load Current	V_{IN} = 0.0V			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2			1	μA
I_{DDO}	Power Supply Current	V_{GG} = V_{CC}, $\overline{CS}$ = V_{CC} −2 I_{OL} = 0.0 mA, T_A = 25°C, (Note 2)		5	10	mA
I_{DD1}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 25°C		35	50	mA
I_{DD2}	Power Supply Current	$\overline{CS}$ = 0.0, I_{OL} = 0.0 mA, T_A = 25°C		32	46	mA
I_{DD3}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 0°C		38.5	60	mA
I_{CF1}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		8	14	mA
I_{CF2}	Output Clamp Current	V_{OUT} = −1.0, T_A = 25°C			13	mA
I_{GG}	Gate Supply Current				1	μA
V_{IL1}	Input Low Voltage for TTL Interface		−1.0		V_{CC}−4.1	V
V_{IL2}	Input Low Voltage for MOS Interface		V_{DD}		V_{CC}−6	V
V_{IH}	Address and Chip Select Input High Voltage		V_{CC}−2		V_{CC}+0.3	V
I_{OL}	Output Sink Current	V_{OUT} = 0.45V	1.6	4		mA
I_{OH}	Output Source Current	V_{OUT} = 0.0V	−2.0			mA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		−0.7	0.45	V
V_{OH}	Output High Voltage	I_{OH} = −100μA	3.5	4.5		V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2: Power-Down Option: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option, please specify MM1702AL.

read operation ac characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNITS
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous Read Data Valid			100	ns
t_{ACC}	Address to Output Delay		0.7	1	μs
t_{DVGG}	Clocked V_{GG} Set-Up (Note 1)	1			μs
t_{CS}	Chip Select Delay			100	ns
t_{CO}	Output Delay From $\overline{CS}$			900	ns
t_{OD}	Output Deselect			300	ns
t_{OHC}	Data Out Hold in Clocked V_{GG} Mode (Note 1)			5	μs

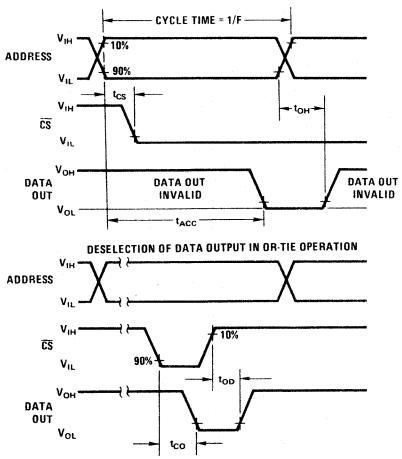
capacitance characteristics $T_A = 25°C$ (Note 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	All Unused	$V_{IN} = V_{CC}$		8	15	pF
C_{OUT}	Output Capacitance	Pins Are	$\overline{CS} = V_{CC}$		10	15	pF
C_{VGG}	V_{GG} Capacitance (Note 1)	At ac Ground	$V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$			30	pF

Note 3: This parameter is periodically sampled and is not 100% tested.

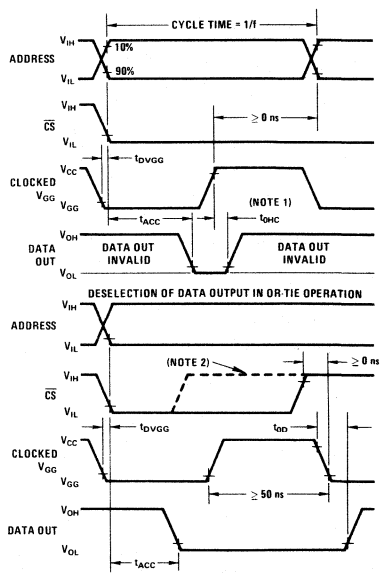
read operation switching time waveforms

(a) Constant V_{GG} Operation



Conditions of Test:
Input pulse amplitudes: 0–4V, t_r, $t_f \leq 50$ ns. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leq 15$ ns), $C_L = 15$ pF.

(b) Power-Down Option (Note 1)



Note 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Note 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

programming operation dc characteristics

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI1P}	Address and Data Input Load Current	$V_{IN} = -48V$			10	mA
I_{LI2P}	Program and V_{GG} Load Current	$V_{IN} = -48V$			10	mA
I_{BB}	V_{BB} Supply Load Current	(Note 5)		10	100	mA
I_{DDP}	Peak I_{DD} Supply Load Current	$V_{DD} = V_{PROG} = -48V$ $V_{GG} = -35V$ (Note 4)		200	300	mA
V_{IHP}	Input High Voltage				0.3	V
V_{IL1P}	Pulsed Data Input Low Voltage		−46		−48	V
V_{IL2P}	Address Input Low Voltage		−40		−48	V
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage		−46		−48	V
V_{IL4P}	Pulsed Input Low V_{GG} Voltage		−35		−40	V

Note 4: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300 mA for greater than 100μs. Average power supply current I_{DDP} is typically 40 mA at 20% duty cycle.

Note 5: The V_{BB} supply must be limited to 100 mA max current to prevent damage to the device.

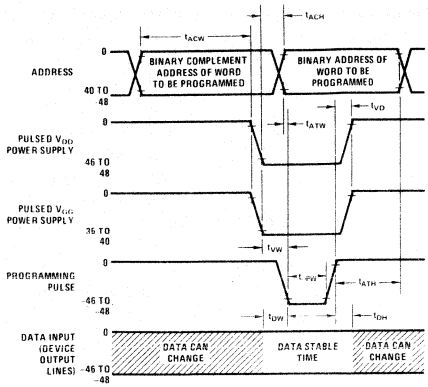
programming operation ac characteristics

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Duty Cycle (V_{DD}, V_{GG})				20	%
$t_{\phi PW}$	Program Pulse Width	$V_{GG} = -35V$, $V_{DD} = V_{PROG} = -48V$			3	ms
t_{DW}	Data Set-Up Time		25			μs
t_{DH}	Data Hold Time		10			μs
t_{VW}	V_{DD}, V_{GG} Set-Up		100			μs
t_{VD}	V_{DD}, V_{GG} Hold		10		100	μs
t_{ACW}	Address Complement Set-Up	(Note 6)	25			μs
t_{ACH}	Address Complement Hold	(Note 6)	25			μs
t_{ATW}	Address True Set-Up		10			μs
t_{ATH}	Address True Hold		10			μs

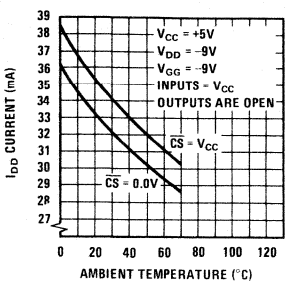
Note 6: All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0–255) must be programmed as shown in the timing diagram until data reads true, then over-programmed 4 times that amount. (Symbolized by x + 4x.)

programming operation switching time waveforms

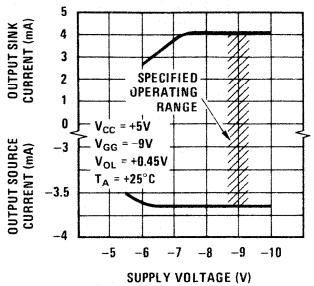


typical performance characteristics

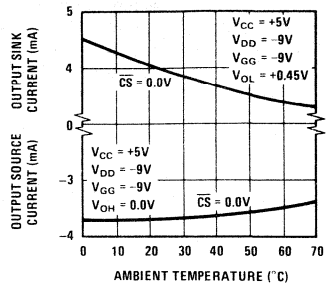
I_{DD} Current vs Temperature



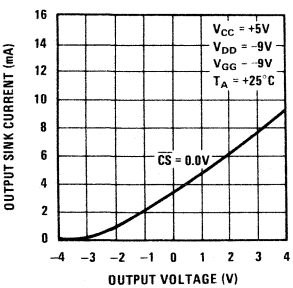
Output Current vs V_{DD} Supply Voltage



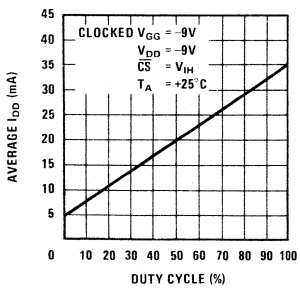
Program Waveforms



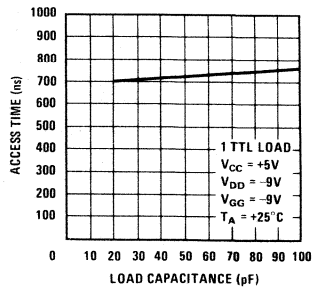
Output Sink Current vs Output Voltage



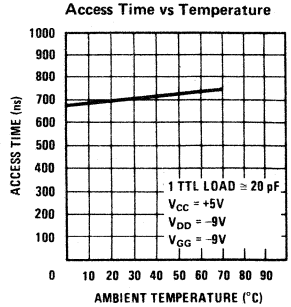
Average Current vs Duty Cycle for Clocked V_{GG} (Note 1)



Access Time vs Load Capacitance



Access Time vs Temperature



5

operation of the MM1702A in program mode

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1's" (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table for logic levels). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25μs after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10μs before the program pulse is applied. The addresses should be programmed in the sequence 0–255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (–48V) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 4-4). All eight bits of one word are programmed simultaneously be setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

MM1702A erasing procedure

The MM1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 6W sec/cm^2. Examples of ultraviolet sources which can erase the MM1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the MM1702A to be erased should be placed about one inch away from the lamp tubes. There exists no absolute rule for erase time. Establish a worst case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. (May be expressed as x + 2x.)

National Semiconductor

MM2708, MM2708-1 8192-Bit (1024 × 8) UV Erasable PROMs

General Description

The MM2708, MM2708-1 are high speed 8192 UV erasable and electrically reprogrammable EPROMs ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

The MM2708, MM2708-1 are packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices by following the programming procedure.

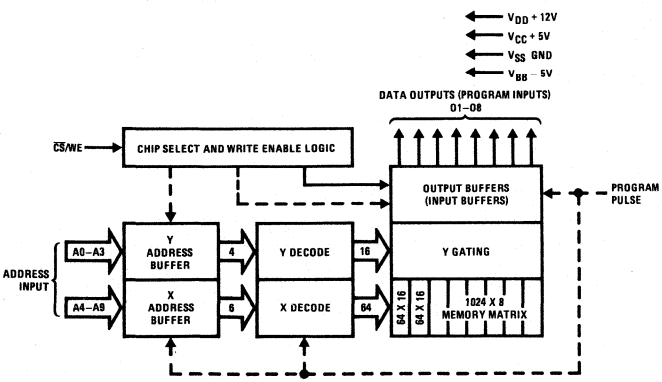
These EPROMs are fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

Features

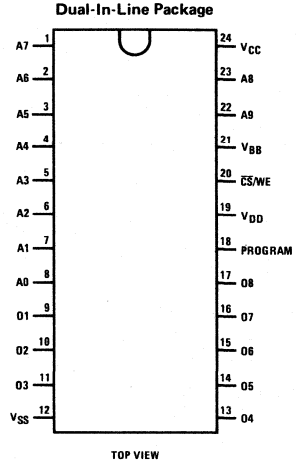
- 1024 x 8 organization
- 800 mW max
- Low power during programming
- Access time – MM2708, 450 ns; MM2708-1, 350 ns
- Standard power supplies: 12V, 5V, –5V
- Static–no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

5

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM2708Q or MM2708Q-1
See NS Package J24CQ

Pin Connection During Read or Program

MODE	PIN NUMBER						
	9–11, 13–17	12	18	19	20	21	24
Read	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

Pin Description

A0–A9	Address inputs
O1–O8	Data outputs
CS/WE	Chip select/write enable input

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
V_{DD} with Respect to V_{BB}	20V to −0.3V
V_{CC} and V_{SS} with Respect to V_{BB}	15V to −0.3V
All Input or Output Voltages with Respect to V_{BB} During Read	15V to −0.3V
$\overline{CS}$/WE Input with Respect to V_{BB} During Programming	20V to −0.3V
Program Input with Respect to V_{BB}	35V to −0.3V
Power Dissipation	1.5 W
Lead Temperature (Soldering, 10 seconds)	300°C

Read Operation

DC Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted, (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Sink Current	V_{IN} = 5.25V or V_{IN} = V_{IL}		1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V		1	10	μA
I_{DD}	V_{DD} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		44	65	mA
I_{CC}	V_{CC} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		7	10	mA
I_{BB}	V_{BB} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		34	45	mA
V_{IL}	Input Low Voltage		V_{SS}		0.65	V
V_{IH}	Input High Voltage		3.0		V_{CC}+1	V
V_{OH1}	Output High Voltage	I_{OH} = −100 μA	3.7			V
V_{OH2}	Output High Voltage	I_{OH} = −1 mA	2.4			V
V_{OL}	Output Low Votlage	I_{OL} = 1.6 mA			0.45	V
P_D	Power Dissipation				800	mW

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted

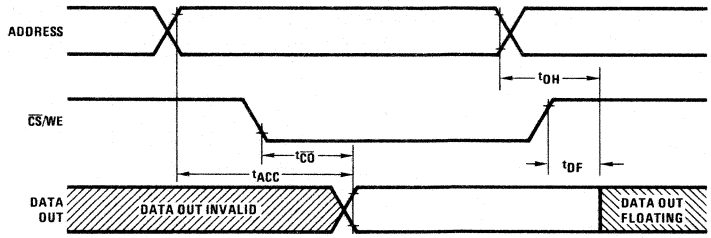
PARAMETER		CONDITIONS	MM2708		MM2708-1		UNITS
			MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	Output Load: 1 TTL Gate and C_L = 100 pF, Input Rise and Fall Times ≤ 20 ns: Timing Measurement Reference Levels: 0.8V and 2.8V for Inputs; 0.8V and 2.4V for Outputs, Input Pulse Levels: 0.65V to 3V		450		350	ns
t_{CO}	Chip Select to Output Delay			120		120	ns
t_{DF}	Chip Deselect to Output Delay		0	120		120	ns
t_{OH}	Address to Output Hold		0		0		ns
CAPACITANCE (Note 2)							
C_{IN}	Input Capacitance	V_{IN} = 0V, T_A = 25°C, f = 1 MHz		6		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz		12		12	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing. T_A = 25°C, f = 1 MHz

Note 3: Typical conditions are for operation at: T_A = 25°C, V_{CC} = 5V, V_{DD} = 12V, V_{BB} = −5V, and V_{SS} = 0V.

Switching Time Waveforms



Programming Instructions

Initially, and after each erasure, all bits of the MM2708, MM2708-1 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the $\overline{CE}$/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (O1—O8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x $t_{PW} \geq 100$ ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops through all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Characteristics

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted

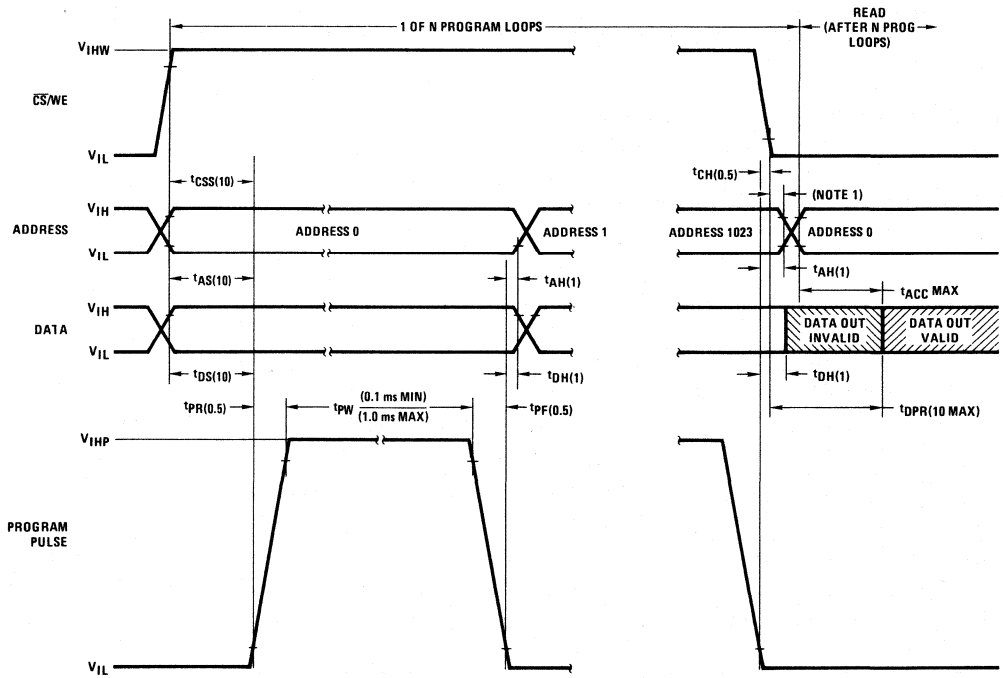
DC Programming Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current	V_{IN} = 5.25V			10	μA
I_{IPL}	Program Pulse Source Current				3	mA
I_{IPH}	Program Pulse Sink Current				20	mA
I_{DD}	V_{DD} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		44	65	mA
I_{CC}	V_{CC} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		7	10	mA
I_{BB}	V_{BB} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		34	45	mA
V_{IL}	Input Low Level (Except Program)		V_{SS}		0.65	V
V_{IH}	Input High Level, All Addresses and Data		3.0		V_{CC}+1	V
V_{IHW}	$\overline{CS}$/WE Input High Level	Referenced to V_{SS}	11.4		12.6	V
V_{IHP}	Program Pulse High Level	Referenced to V_{SS}	25		27	V
V_{ILP}	Program Pulse Low Level	$V_{IHP} - V_{ILP}$ = 25V Min	V_{SS}		1	V

AC Programming Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{AS}	Address Set-Up Time		10			μs
t_{CSS}	$\overline{CS}$/WE Set-Up Time		10			μs
t_{DS}	Data Set-Up Time		10			μs
t_{AH}	Address Hold Time		1			μs
t_{CH}	$\overline{CS}$/WE Hold Time		0.5			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Chip Deselect to Output Float Delay		0		120	μs
t_{DPR}	Program to Read Delay				10	μs
t_{PW}	Program Pulse Width		0.1		1.0	ms
t_{PR}	Program Pulse Rise Time		0.5		2.0	μs
t_{PF}	Program Pulse Fall Time		0.5		2.0	μs

Programming Waveforms

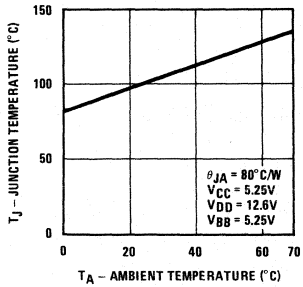


Note 1: The $\overline{CS}$/WE transition must occur after the program pulse transition and before the address transition.

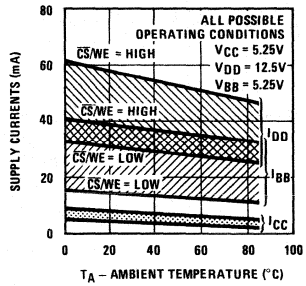
Note 2: Numbers in parentheses indicate minimum timing in microseconds unless otherwise specified.

Typical DC Performance Characteristics

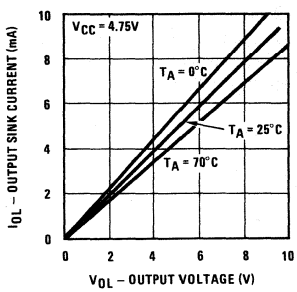
Maximum Junction Temperature vs Ambient Temperature



Range of Supply Currents vs Temperature

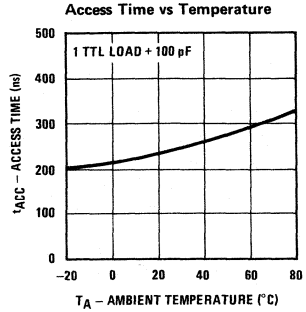


Output Sink Current vs Output Voltage

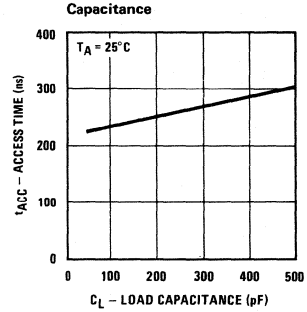


Typical AC Performance Characteristics

Access Time vs Temperature



Access Time vs Load Capacitance



National Semiconductor

MM4203/MM5203 2048-Bit (256 × 8 or 512 × 4) UV Erasable PROM

general description

The MM4203/MM5203 is a 2048-bit static read-only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words or 512-4-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

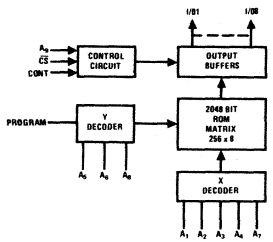
features

- Field programmable
- Bipolar compatibility — +5V, −12V operation
- High speed operation — 1μs max access time
- Pin compatible with MM5213, MM5231 mask programmable ROMs
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e. 253.7 n.m.)
- Chip select output control
- 256 x 8 or 512 x 4 organization

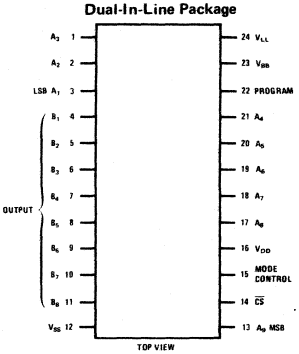
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

block and connection diagrams



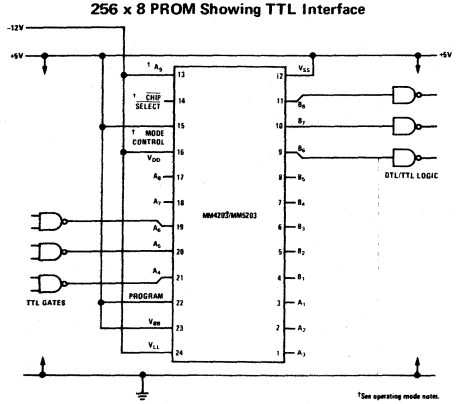
Dual-In-Line Package



Order Number MM4203Q or MM5203Q
See NS Package J24CQ

typical applications

256 x 8 PROM Showing TTL Interface



Operating Modes

256 x 8 ROM connection (shown)
Mode Control — HIGH (V_{SS})
A_9 — LOW

512 x 4 ROM connections
Mode Control — LOW (GND or V_{DD})
A_9 — Logic HIGH enables the odd (B_1, B_3..B_7) outputs
— Logic LOW enables the even (B_2, B_4..B_8) outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

Programming is accomplished in 256 x 8 mode only.

Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+.3V to −20V	Storage Temperature Range	−65°C to 125°C
Power Dissipation	1W	Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range MM4203	−55°C to 85°C		
MM5203	0°C to 70°C		

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{DD} = V_{LL} = −12V, ±5%, V_{BB} = PROGRAM = V_{SS} unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current, I_{LI}	V_{IN} = 0V			1	μA
Output Leakage, I_{LO}	V_{OUT} = 0V $\overline{CS}$ = V_{SS} - 2.0			1	μA
Power Supply Current, I_{SS}	T_A = 25°C $\overline{CS}$ = V_{SS} - 2.0		35	55	mA
Input LOW Voltage, V_{IL}		V_{SS} - 10		V_{SS} - 4.0	V
Input HIGH Voltage, V_{IH}		V_{SS} - 2.0		V_{SS} + .3	V
Output LOW Voltage, V_{OL}	1.6 mA sink −12.6V < V_{LL} < −3V			.40	V
Output Clamp Current, I_{CF}	V_{LL} = −3.0V V_{OUT} = −1.0V (Note 8) T_A = 0°C		3.5	6.0	mA
	V_{LL} = −12.6V V_{OUT} = −1.0V (Note 8) T_A = 0°C		8.0	15.0	mA
Output HIGH Voltage, V_{OH}	0.8 mA source	2.4			V
Data Hold Time, T_{OH}	(Min Access Time) Figures 1 & 2			100	ns
Access Time, T_{ACC}	T_A = 25°C Figures 1 & 2 (Note 6)		.700	1	μs
Chip Select Time, T_{CO}	Figures 1 & 3			500	ns
Chip Deselect Time, T_{OD}	Figures 1 & 3			500	ns
Allowable Chip Select Delay, t_{CS}	Figures 1 & 2 Allowable delay in selecting chip after change of address without affecting access time.			100	ns
Input Capacitance, C_{IN}	V_{IN} = V_{SS}		8	15	pF
Output Capacitance, C_{OUT}	V_{OUT} = V_{SS} f = 1.0 MHz (Note 2)		8	15	pF
	$\overline{CS}$ = V_{SS} - 2.0				

programming characteristics (see Figure 4)

T_A = 25°C, V_{SS} = 0V, V_{BB} = +12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address and Data Input Load Current, I_{LD}	V_{IN} = −50V		0	10	mA
Program Load Current, I_{LP}	V_{IN} = −50V		0	10	mA
V_{BB} Supply Load Current, I_{LB}			0	10	mA
Peak I_{DD} Supply Load Current I_{LDD} (Note 3)	V_{DD} = $V_{program}$ = −50V		650		mA
Input High Voltage, V_{IHP}		−2		+.3	V
Address and Data Input Low Voltage, V_{ILP}		−50		−40	V
Pulsed Input Low Voltage:					
V_{DD}, and Program, V_{DLP}		−50		−48	V
V_{LL}	(Note 5)	−50		0	V
V_{DD} Pulse Duty Cycle				2	%
Program Pulse Width, t_{PW} (Note 4)	V_{DD} = $V_{program}$ = −50V			20	ms
Data and Address Set Up Time, t_{DW}		1			μs
Data and Address Hold Time, t_{DH}		0			μs
Pulsed V_{DD} Supply Overlap, t_{SS}		1		100	μs
Pulsed V_{DD} Supply Overlap, t_{SH}		−.1		3	ms
V_{DD}, Program, Address, and Input Rise and Fall Times				1	μs

Note 1: During programming, data is always applied in the 256 x 8 mode, regardless of the logic state of A_9 and MODE CONTROL.
Note 2: Capacitances are not tested on a production basis but are periodically sampled.
Note 3: I_{DDP} flows only during program period t_{PWP}. Average power supply current I_{LDD} is typically 15 mA at 2% duty cycle.
Note 4: Maximum duty cycle of t_{PW} should not be greater than 2% of cycle time so that power dissipation is minimized. The program cycle should be repeated until the data reads true, then over-program three times that number of cycles (symbolized as X+3X programming.
Note 5: V_{LL} is not needed during programming but may be tied to V_{DD} for convenience.
Note 6: T_{ACC} = 1000 ns + 25(N-1) where N is the number of chips wired-OR together.
Note 7: Measured under continuous operation.
Note 8: I_{CF} flows out the V_{LL} pin, it does not flow out the V_{DD} pin.

access time diagrams

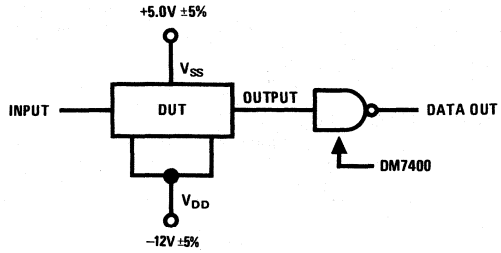


Figure 1

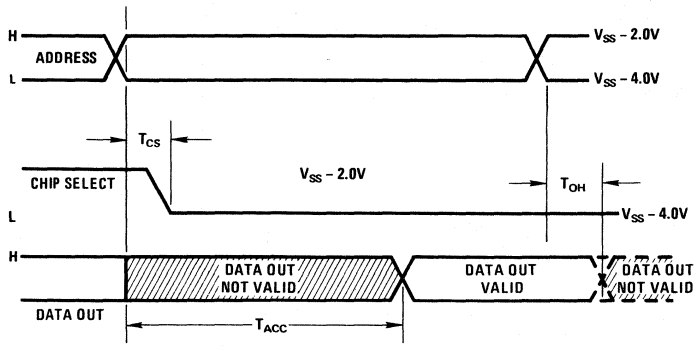


Figure 2

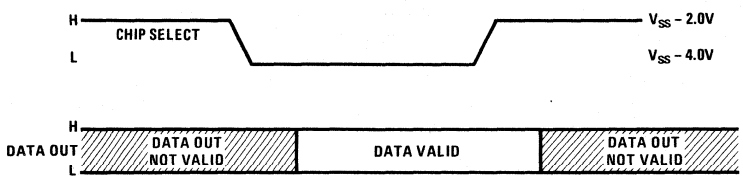


Figure 3

program waveforms

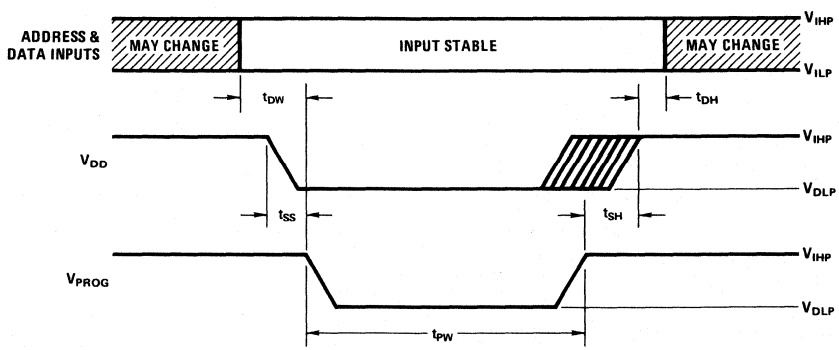


Figure 4

operation of the MM4203/MM5203 in program mode

Initially, all 2048 bits of the MM4203/MM5203 are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations. (Note 1)

Word address selection is done by the same decoding circuitry used in the Read mode. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A LOW data input level (−50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the V_{DD} pulse (amplitude and width as specified on page 4) should be limited to 2%. The address should be applied for at least 1 μs before application of the Program pulse. In programming mode, data inputs 1–8 are pins 4–11 respectively regardless of the logic state of A_9 and mode control. Chip select should be disabled (HIGH).

Positive logic is used during the read mode for addresses and data out. Address 0 corresponds to all address inputs at V_{IL} and address 255_{10} corresponds to all address inputs at V_{IH}. A "1" or a P at a data output corresponds to V_{OH}. A "0" or an N at a data output corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address 0 corresponds to all address inputs at V_{ILP} and address 255_{10} corresponds to all address inputs at V_{IHP}.

Negative logic is used during the programming mode for data in. A "1" or a P at a data input corresponds to V_{ILP}. A "0" or an N at a data input corresponds to V_{IHP}.

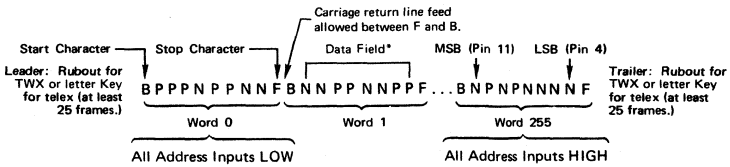
MODE	DATA AND ADDRESS LINES		V_{SS}	V_{BB}	V_{DD}	PROGRAM	$\overline{CS}$	V_{LL}
	HIGH	LOW						
Read	V_{SS} − 2.0	V_{SS} − 4.0	+5	V_{SS}	−12	V_{SS}	V_{SS} − 4V	−3V to −12V
Program	V_{SS} −2.0	V_{SS} − 40	GND	+12	−48 (Pulse)	−48 (Pulse)	GND	GND to −50V

erasing procedure

The MM4203Q/MM5203Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worst-case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-2 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4203/MM5203 should be placed about one inch away from the lamp for about 20–30 minutes.

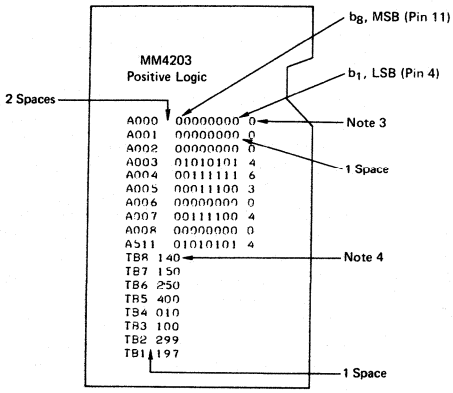
preferred tape format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 256 words must be entered, beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

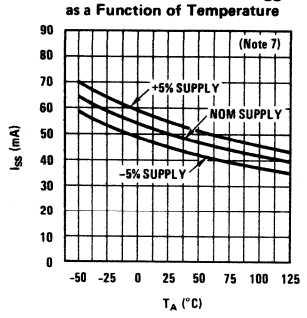
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

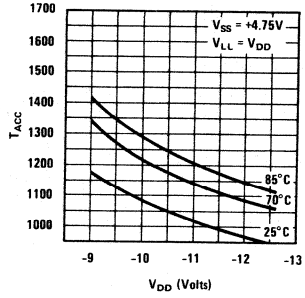
Note 4: The total number of "1" bits in each output column or bit position.

typical performance characteristics

Maximum Supply Current I_{SS} as a Function of Temperature



Maximum Access Time (T_{ACC}) as a Function of V_{DD} Supply Voltage



MM4204/MM5204 4096-Bit (512 × 8) UV Erasable PROM

General Description

The MM4204/MM5204 is a 4096-bit static read only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, Power Saver, is provided which gives a 5:1 decrease in power when the memory is not being accessed.

- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications
- Compatible with SC/MP II N-channel microprocessor

Features

- Field programmable
- Fast program time: ten seconds typical for 4096 bits
- Fast access time

MM4204	1.25 μs
MM5204	1 μs

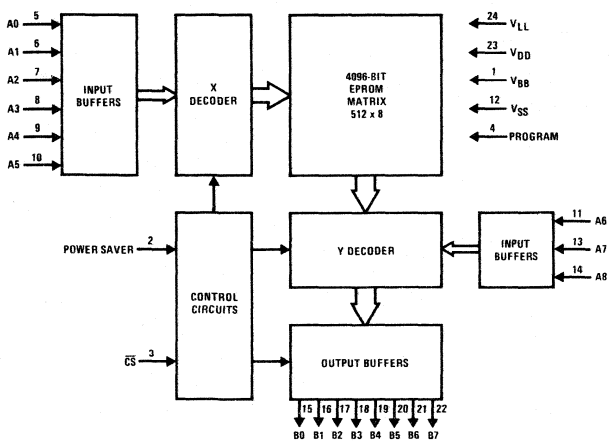
- DTL/TTL compatibility
- Standard power supplies 5V, −12V

Applications

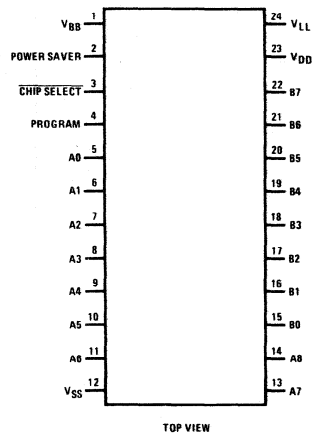
- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

5

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4204D or MM5204D
See NS Package D24C

Order Number MM4204Q or MM5204Q
See NS Package J24CQ

Absolute Maximum Ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Operating Temperature Range	
MM5204	0°C to +70°C
MM4204	−55°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28	40.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			50.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		6.0	8.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			42	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			52	mA
I_{SS}		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			12	mA

AC Electrical Characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time					
	MM5204	T_A = 70°C, *(Figure 1)*, (Note 4)		0.75	1.0	μs
	MM4204	T_A = 85°C, *(Figure 1)*, (Note 4)			1.25	μs
t_{PO}	Power Saver Set-Up Time					
	MM5204	*(Figure 1)*			1.8	μs
	MM4204	*(Figure 1)*			2.0	μs
t_{CO}	Chip Select Delay					
	MM5204	*(Figure 1)*			500	ns
	MM4204	*(Figure 1)*			600	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
t_{ODP}	Power Saver Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

Programmer Electrical Characteristics

$T_A = 25°C$, $V_{SS} = \overline{CS}$ = Power Saver = 0V, V_{LL} = 0V to −14V, unless otherwise specified, *(Figure 2)*, (Note 5).

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = −18V			−10	mA
I_{ALD}	Address Input Load Current	V_{IN} = −50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{LBB}	V_{BB} Load Current				50	mA
I_{LDD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			−200	mA
V_{IHP}	Address Data and Power Saver Input High Voltage		−2.0		0.3	V
V_{ILP}	Address Input Low Voltage		−50		−11	V
	Data Input Low Voltage		−18		−11	V
V_{DHP}	V_{DD} and Program High Voltage		−2.0		0.5	V
V_{DLP}	V_{DD} and Program Low Voltage		−50		−48	V
V_{BLP}	V_{BB} Low Voltage		0		0.4	V
V_{BHP}	V_{BB} High Voltage		11.4		12.6	V
V_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{DS}	Data and Address Set-Up Time		40			μs
t_{DH}	Data and Address Hold Time		0			μs
t_{SS}	Pulsed V_{DD} Set-Up Time		40		100	μs
t_{SH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set-Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set-Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_R, t_F	V_{DD}, Program, Address and Data Rise and Fall Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used except on data inputs during programming
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 700 ns + 25 (N-1) where N is the number of devices wire—OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5X programming).

Note 6: The EPROM is initially programmed with all "0's." A V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

Note 7: Typical values are for nominal voltages and $T_A = 25°C$, unless otherwise specified.

Erase Specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm^2.

Programming

The MM4204/MM5204 is normally shipped in the unprogrammed state. All 4096-bits are at logic "0" state. The table of electrical programming characteristics and *Figure 2* give the conditions for programming of the device. In the program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A0—A8. Data inputs are B0—B7 and write operation is controlled by pulsing the Program input. Since the EROM is initially shipped with all "0's," a V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

Programming (Continued)

National offers programmer options with both the IMP16-P and the PACE IPC-16P Microprocessor Development Systems.

Microprocessor System	Programmer Part Number
IMP16-P	IMP16-P/805
IPC-16P	IPC-16P/805

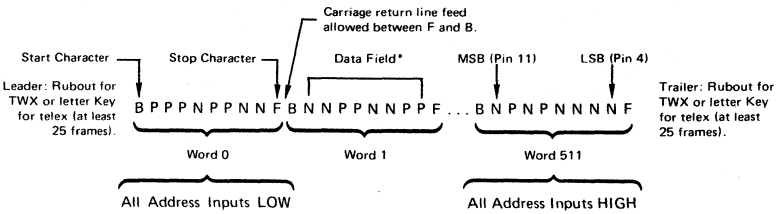
Contact the local sales office for further information. There are also several commercial programmers available such as the Data I/O Model V.

Most National distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed:

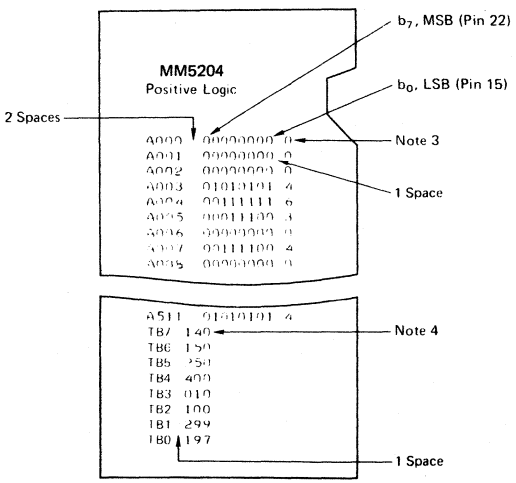
Preferred Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

Alternate Format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

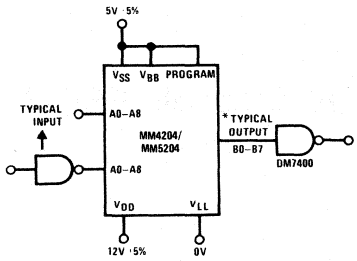
Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

Erasing Procedure

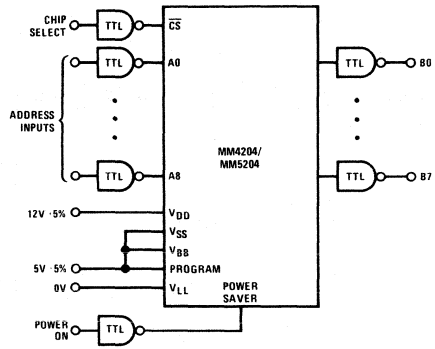
The MM4204Q/MM5204Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worse case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-52 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4204/MM5204 should be placed about one inch away from the lamp for about 20–30 minutes.

AC Test Circuit

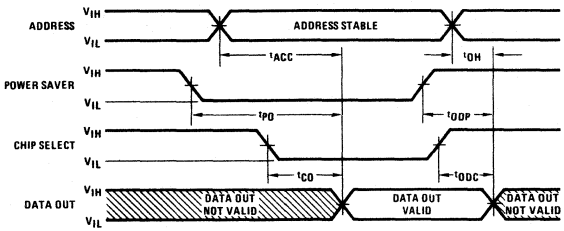


*t_{ACC}, t_{OH}, t_{CD}, and t_{OD} measured at output of MM4204/MM5204.

Typical Application



Switching Time Waveforms



Note. All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns

FIGURE 1. Read Operation

Programming Waveforms

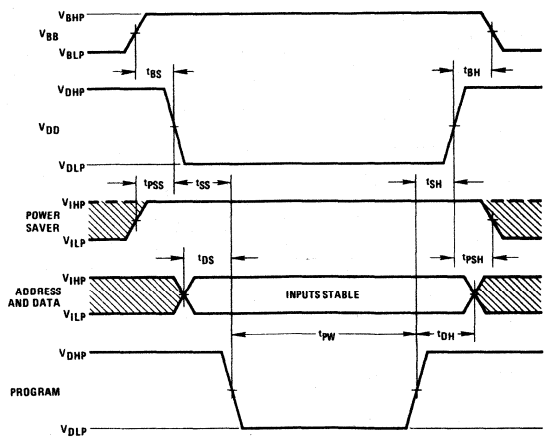


FIGURE 2. Programming Waveforms

5

National Semiconductor

MM5204-1 4096-Bit (512 × 8) UV Erasable PROM

General Description

The MM5204-1 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, "Power Saver", is provided which gives a 5:1 decrease in power when the memory is not being accessed.

- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications
- Compatible with SC/MP II N-channel microprocessor

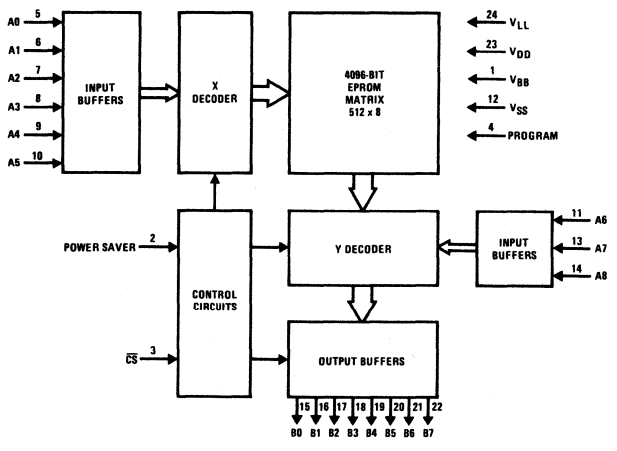
Features

- Field programmable
- Fast program time: ten seconds typical for 4096 bits
- Fast access time
  MM5204-1 700 ns
- DTL/TTL compatibility
- Standard power supplies 5V, −12V

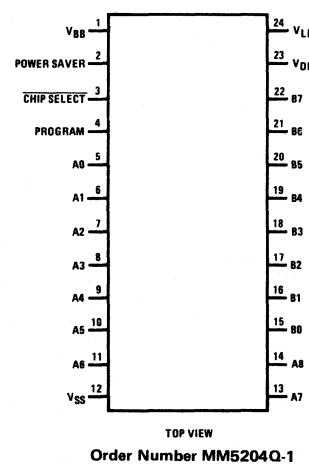
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5204Q-1
See NS Package J24CQ

Absolute Maximum Ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Operating Temperature Range	
MM5204-1	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	T_A = 0°C, $\overline{CS}$ = V_{IH},				
		Power Saver = V_{IL}		28	40.0	mA
		Power Saver = V_{IH}		6.0	8.0	mA
I_{SS}	V_{SS} Current	T_A = 0°C, $\overline{CS}$ = V_{IH}				
		Power Saver = V_{IL}			42	mA
		Power Saver = V_{IH}			10	mA

AC Electrical Characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time	T_A = 70°C, *(Figure 1)*, (Note 4)			700	ns
t_{PO}	Power Saver Set-Up Time	*(Figure 1)*			1.4	μs
t_{CO}	Chip Select Delay	*(Figure 1)*			250	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time	*(Figure 1)*	30	200	500	ns
t_{ODP}	Power Saver Deselect Time	*(Figure 1)*	30	200	500	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

Programmer Electrical Characteristics

$T_A = 25°C$, $V_{SS} = \overline{CS}$ = Power Saver = 0V, V_{LL} = 0V to −14V, unless otherwise specified, *(Figure 2)*, (Note 5).

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = −18V			−10	mA
I_{ALD}	Address Input Load Current	V_{IN} = −50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{LBB}	V_{BB} Load Current				50	mA
I_{LDD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			−200	mA
V_{IHP}	Address Data and Power Saver Input High Voltage		−2.0		0.3	V
V_{ILP}	Address Input Low Voltage		−50		−11	V
	Data Input Low Voltage		−18		−11	V
V_{DHP}	V_{DD} and Program High Voltage		−2.0		0.5	V
V_{DLP}	V_{DD} and Program Low Voltage		−50		−48	V
V_{BLP}	V_{BB} Low Voltage		0		0.4	V
V_{BHP}	V_{BB} High Voltage		11.4		12.6	V
V_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{DS}	Data and Address Set-Up Time		40			μs
t_{DH}	Data and Address Hold Time		0			μs
t_{SS}	Pulsed V_{DD} Set-Up Time		40		100	μs
t_{SH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set-Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set-Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_r, t_f	V_{DD}, Program, Address and Data Rise and Fall Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used except on data inputs during programming
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 700 ns + 25 (N-1) where N is the number of devices wire—OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5X programming).

Note 6: The EPROM is initially programmed with all "0's." A V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

Note 7: Typical values are for nominal voltages and T_A = 25°C, unless otherwise specified.

Erase Specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm^2.

Programming

The MM5204-1 is normally shipped in the unprogrammed state. All 4096 bits are at logic "0" state. The table of electrical programming characteristics and *Figure 2* give the conditions for programming of the device. In the program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A0—A8. Data inputs are B0—B7 and write operation is controlled by pulsing the Program input. Since the EPROM is initially shipped with all "0's", a V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

Programming (Continued)

National offers a programming option with the SC/MP Low Cost Development System (LCDS).

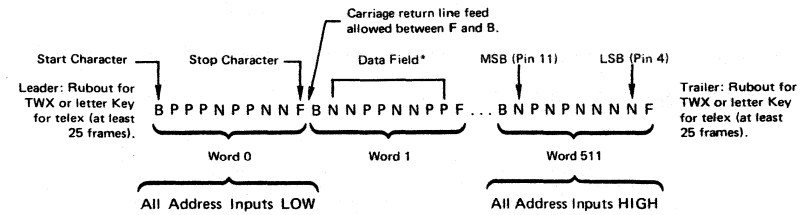
See application note AN-189 for a description, or contact the local sales office for further information. There are also several commercial programmers available.

Most National distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed:

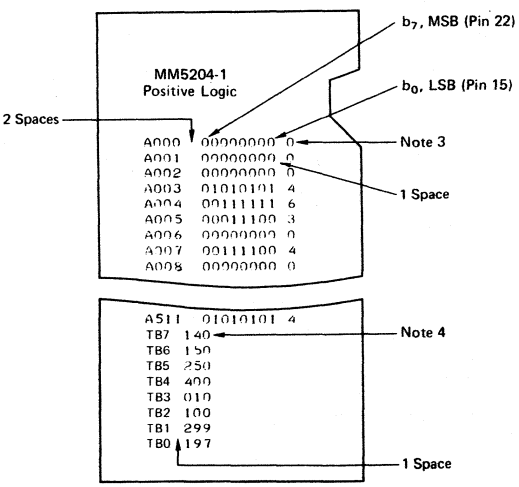
Preferred Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

Alternate Format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

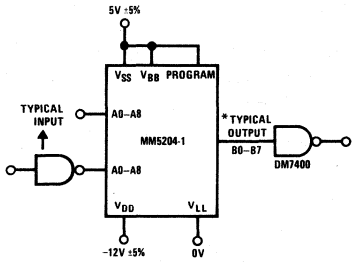
Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

Erasing Procedure

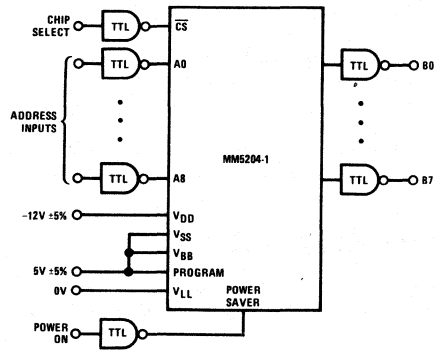
The MM5204-1 may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worst-case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-52 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM5204-1 should be placed about one inch away from the lamp for about 20—30 minutes.

AC Test Circuit

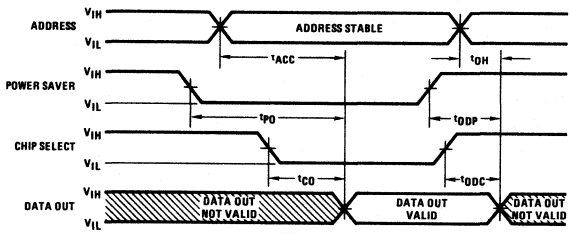


*t_{ACC}, t_{OH}, t_{CD} and t_{OD} measured at output of MM5204-1

Typical Application



Switching Time Waveforms



Note. All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns

FIGURE 1. Read Operation

Programming Waveforms

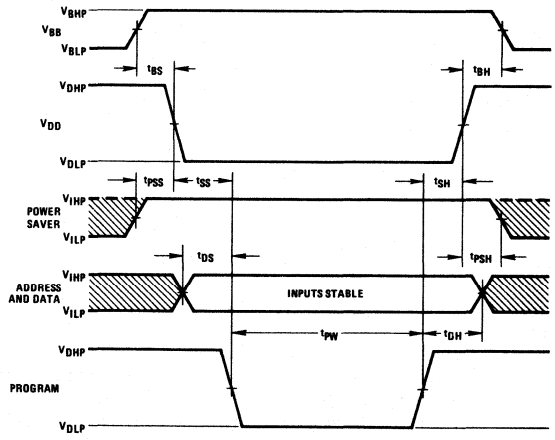


FIGURE 2. Programming Waveforms

Section 6

Bipolar PROMs

6

High speed microcontrol storage is made practical at very low cost through the use of National's bipolar PROMs. This generic family utilizes the latest in Schottky circuitry and Titanium-Tungsten fuse link technology. National offers these and other memory and logic products for state-of-the-art solutions to data processing and control logic design problems. Refer to National's Memory Applications Handbook for suggestions on how to use these devices effectively.

National Semiconductor

DM54S188/DM74S188 256-Bit (32 × 8) Open-Collector PROM

DM54S288/DM74S288 256-Bit (32 × 8) TRI-STATE® PROM

general description

These Schottky PROM memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

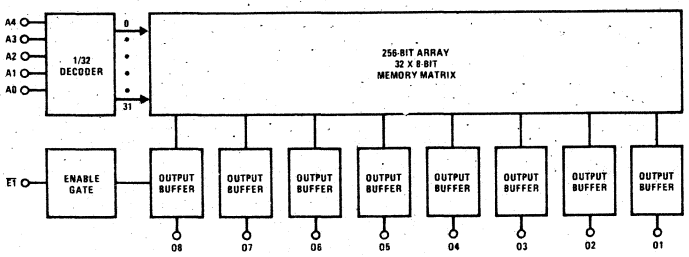
See page 5-36 of the Memory Applications Handbook for detailed programming information.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—35 ns max
  Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming

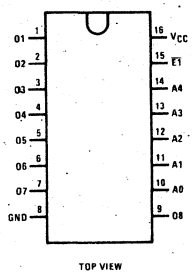
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S188		X	X		N, J
DM74S288		X		X	N, J
DM54S188	X		X		J
DM54S288	X			X	J

block diagram



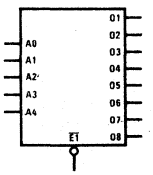
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



Order Number DM54S188J, DM54S288J, DM74S188J or DM74S288J
See NS Package J16A

Order Number DM74S188N or DM74S288N
See NS Package N16A

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S188, DM54S288	4.5	5.5	V
DM74S188, DM74S288	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S188, DM54S288	−55	+125	°C
DM74S188, DM74S288	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S188, 54S288			DM74S188, 74S288			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		70	110		70	110	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S188, 54S288 5V ±10%; −55°C to +125°C			DM74S188, 74S288 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			22	45		22	35	ns
t_{EA}	Enable Access Time			15	30		15	20	ns
t_{ER}	Enable Recovery Time			15	35		15	25	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to either A0 (pin 10) or A4 (pin 14).

National Semiconductor

DM54S287/DM74S287 1024-Bit (256 × 4) TRI-STATE® PROM

DM54S387/DM74S387 1024-Bit (256 × 4) Open-Collector PROM

general description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high state, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

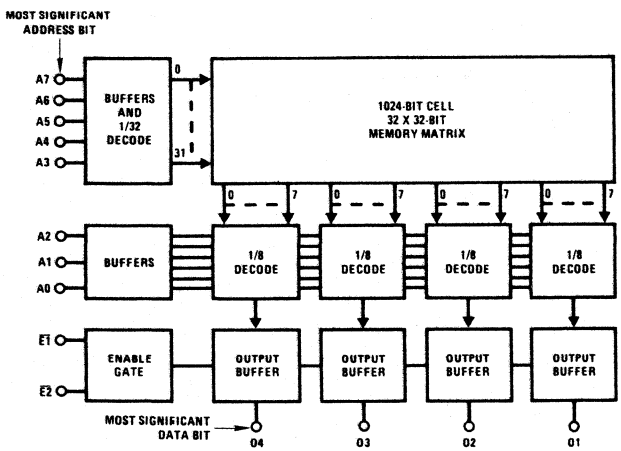
See page 5-36 of the Memory Applications Handbook for detailed programming information.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—50 ns max
  - Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S187 and DM85S97

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S387		X	X		N, J
DM74S287		X		X	N, J
DM54S387	X		X		J
DM54S287	X			X	J

block diagram

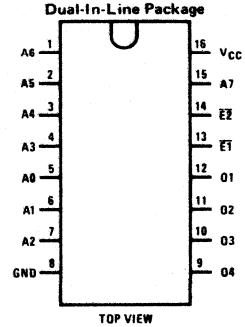


Order Number DM54S287J, DM54S387J, DM74S287J or DM74S387J
See NS Package J16A

Order Number DM74S287N or DM74S387N
See NS Package N16A

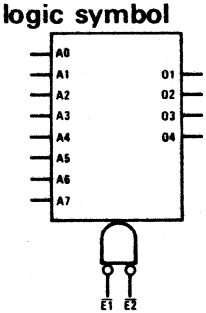
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S387, DM54S287	4.5	5.5	V
DM74S387, DM74S287	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S387, DM54S287	−55	+125	°C
DM74S387, DM74S287	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S387/54S287			DM74S387/74S287			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45V		−80	−250		−80	−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.7V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S387/54S287 5V ±10%; −55°C to +125°C			DM74S387/74S287 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*	10	35	60	10	35	50	ns
t_{EA}	Enable Access Time	*(Figure 2)*	5	15	30	5	15	25	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*	5	15	30	5	15	25	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

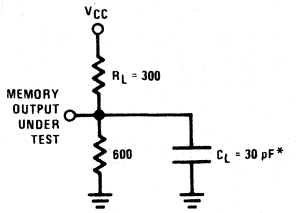
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH} or I_{CEX} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

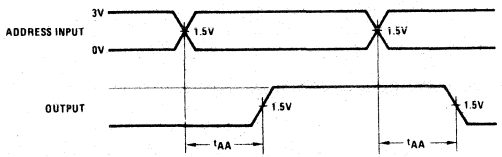


FIGURE 1. Address Access Time

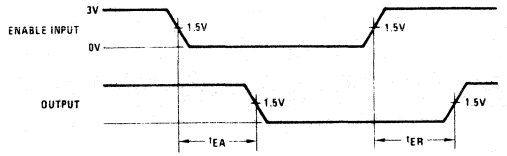
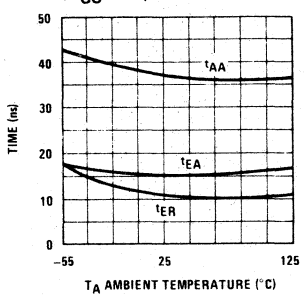


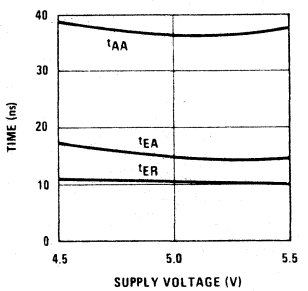
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

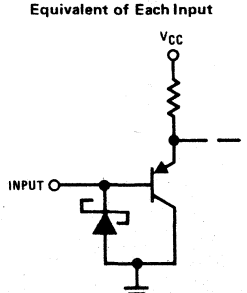


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

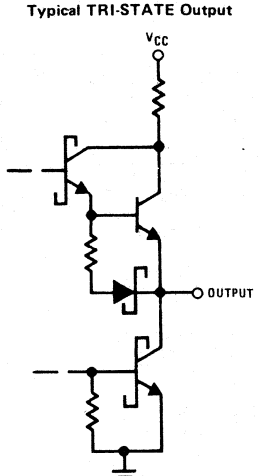


equivalent circuits

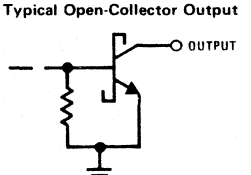
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

Bipolar PROMs
PRELIMINARY

DM54S473/DM74S473 4096-Bit (512 × 8) Open-Collector PROM

DM54S472/DM74S472 4096-Bit (512 × 8) TRI-STATE® PROM

general description

These Schottky PROM memories are organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

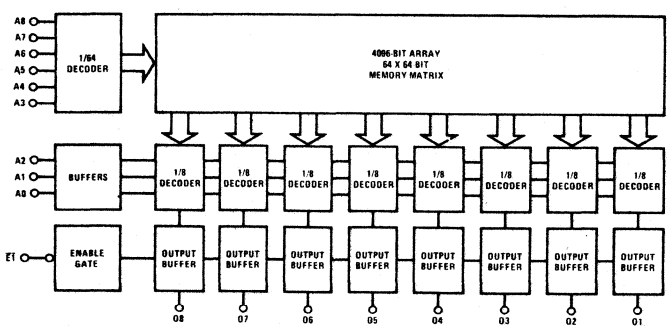
See page 5-36 of the Memory Applications Handbook for detailed programming information.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—60 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 20-pin package

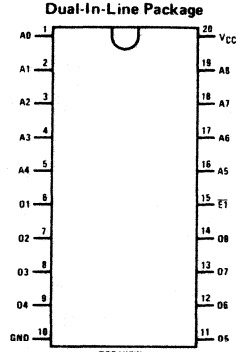
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S473		X	X		N, J
DM74S472		X		X	N, J
DM54S473	X		X		J
DM54S472	X			X	J

block diagram

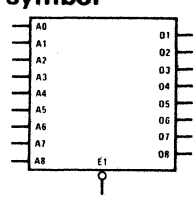


connection diagram

Dual-In-Line Package



logic symbol



Order Number DM54S472J, DM54S473J, DM74S472J or DM74S473J
See NS Package J20B

Order Number DM74S472N or DM74S473N
See NS Package N20A

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S473, DM54S472	4.5	5.5	V
DM74S473, DM74S472	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S473, DM54S472	−55	+125	°C
DM74S473, DM74S472	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S473, 54S472			DM74S473, 74S472			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		120	155		120	155	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S473, 54S472 5V ±10%; −55°C to +125°C			DM74S473, 74S472 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time				75			60	ns
t_{EA}	Enable Access Time				35			30	ns
t_{ER}	Enable Recovery Time				35			30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V.

National Semiconductor

DM54S474/DM74S474 4096-Bit (512 × 8) TRI-STATE® PROM

DM54S475/DM74S475 4096-Bit (512 × 8) Open-Collector PROM

general description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

See page 5-36 of the Memory Applications Handbook for detailed programming information.

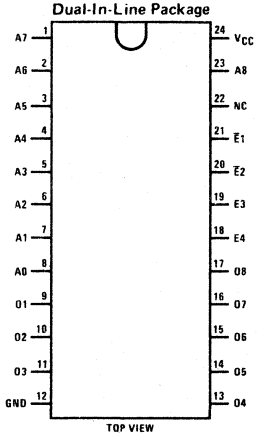
features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—65 ns
  Enable access—35 ns
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM87S95 and DM87S96

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S475		X	X		N, J
DM74S474		X		X	N, J
DM54S475	X		X		J
DM54S474	X			X	J

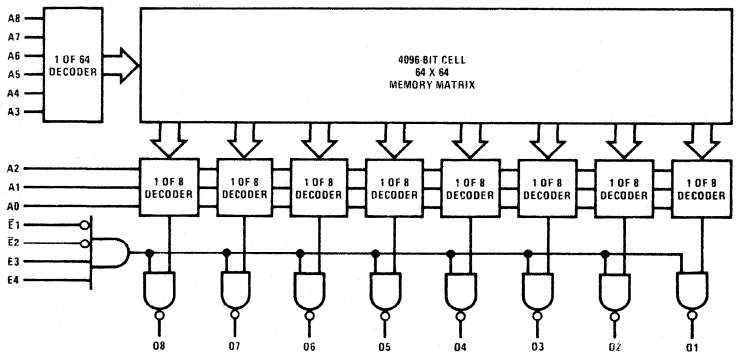
connection diagram

Dual-In-Line Package

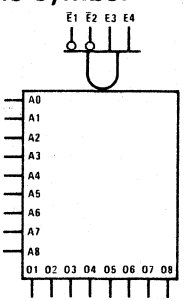


TOP VIEW

block diagram



logic symbol



Order Number DM54S474J, DM54S475J, DM74S474J or DM74S475J
See NS Package J24A

Order Number DM74S474N or DM74S475N
See NS Package N24B

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S474, DM54S475	4.5	5.5	V
DM74S474, DM74S475	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S474, DM54S475	−55	+125	°C
DM74S474, DM74S475	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S474, DM54S475			DM74S474, DM74S475			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	170		115	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S474, DM54S475 5V ±10%; −55°C to +125°C			DM74S474, DM74S475 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*		40	75		40	65	ns
t_{EA}	Enable Access Time	*(Figure 2)*		20	40		20	35	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*		20	40		20	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

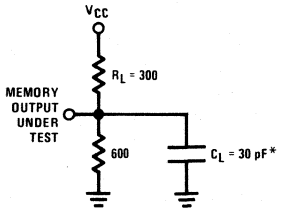
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 1 and pin 6).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

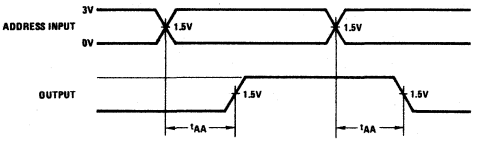


FIGURE 1. Address Access Time

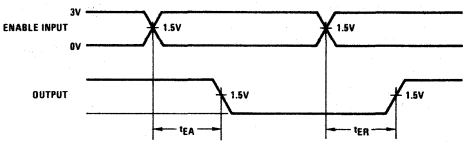
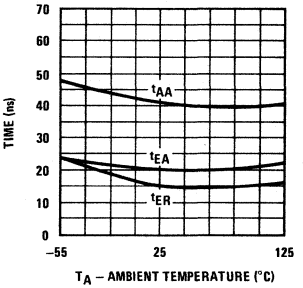


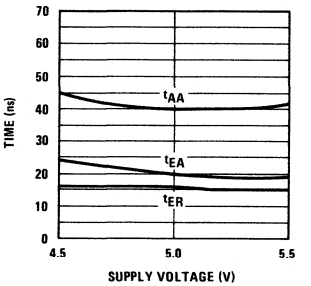
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

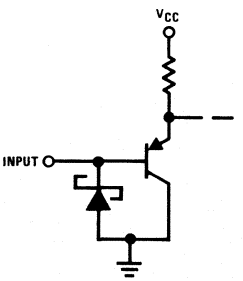


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

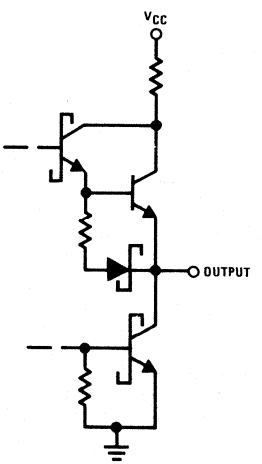


equivalent circuits

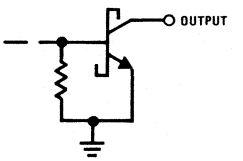
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

DM54S570/DM74S570 2048-Bit (512 × 4) Open-Collector PROM

DM54S571/DM74S571 2048-Bit (512 × 4) TRI-STATE® PROM

general description

These Schottky memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

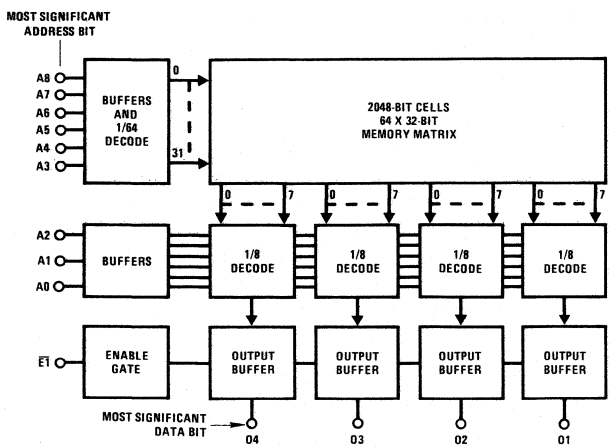
See page 5-36 of the Memory Applications Handbook for detailed programming information.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S270 and DM74S370

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N, J
DM74S571		X		X	N, J
DM54S570	X		X		J
DM54S571	X			X	J

block diagram

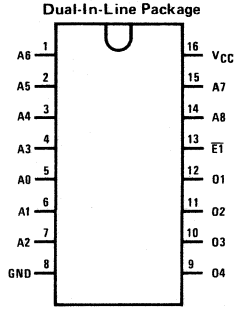


Order Number DM54S570J, DM54S571J, DM74S570J or DM74S571J
See NS Package J16A

Order Number DM74S570N or DM74S571N
See NS Package N16A

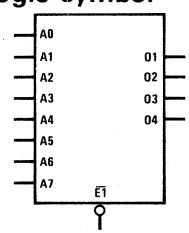
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S570, DM54S571	4.5	5.5	V
DM74S570, DM74S571	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S570, DM54S571	−55	+125	°C
DM74S570, DM74S571	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S570, 54S571			DM74S570, 74S571			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		90	130		90	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S570, 54S571 5V ±10%; −55°C to +125°C			DM74S570, 74S571 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*		40	65		40	55	ns
t_{EA}	Enable Access Time	*(Figure 2)*		20	35		20	30	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*		20	35		20	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

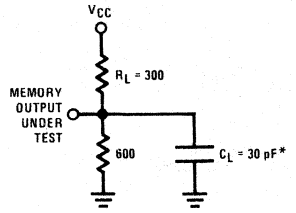
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A8 and A2 (pin 14 and pin 7).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

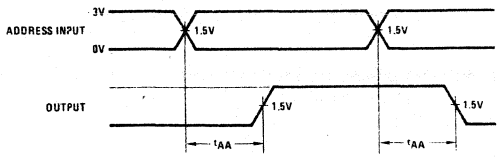


FIGURE 1. Address Access Time

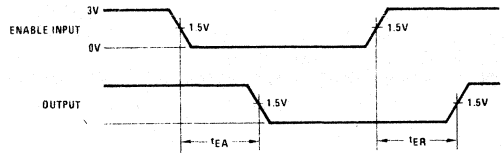
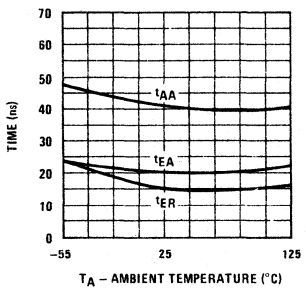


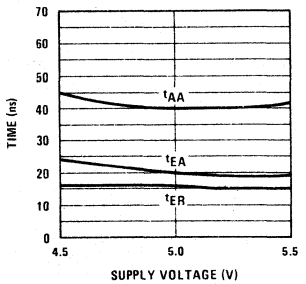
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

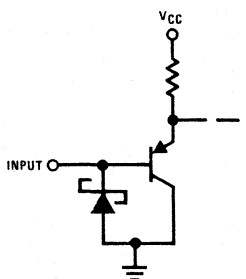


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

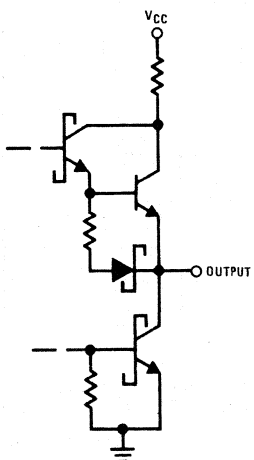


equivalent circuits

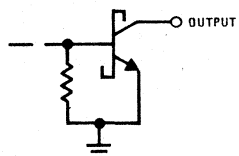
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

DM54S572/DM74S572 4096-Bit (1024 × 4) Open-Collector PROM

DM54S573/DM74S573 4096-Bit (1024 × 4) TRI-STATE® PROM

DM54S574/DM74S574 4096-Bit (1024 × 4) TRI-STATE® PROM

general description

These Schottky PROM memories are organized in the popular 1024 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When the enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

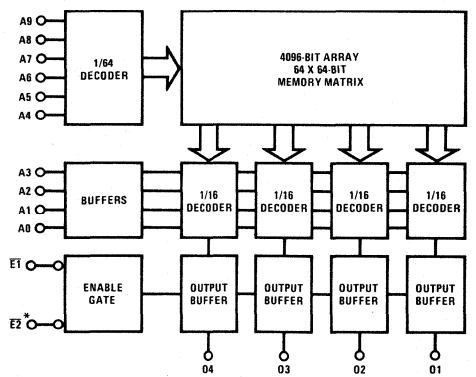
See page 5-36 of the Memory Applications Handbook for detailed programming information.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—60 ns max
  Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 18-pin package

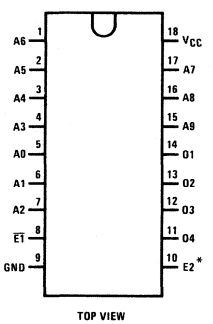
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S572		X	X		N,J
DM74S573		X		X	N,J
DM74S574		X		X	N,J
DM54S572	X		X		J
DM54S573	X			X	J
DM54S574	X			X	J

block diagram



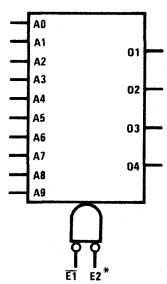
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



*For DM54S574/DM74S574, E2 is active HIGH

Order Number DM54S572J, DM54S573J, DM54S574J, DM74S572J, DM74S573J or DM74S574J
See NS Package J18A

Order Number DM74S572N, DM74S573N or DM74S574N
See NS Package N18A

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S572, DM54S573, DM54S574	4.5	5.5	V
DM74S572, DM74S573, DM74S574	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S572, DM54S573, DM54S574	−55	+125	°C
DM74S572, DM74S573, DM74S574	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S572, 54S573, 54S574			DM74S572, 74S573, 74S574			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		125	140		125	140	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S572, 54S573, 54S574 5V ±10%; −55°C to +125°C			DM74S572, 74S573, 74S574 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	60	ns
t_{EA}	Enable Access Time			25	45		25	35	ns
t_{ER}	Enable Recovery Time			25	45		25	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A5 and A2 (pin 2 and pin 7).

Section 7

Bipolar ROMs

7

National's bipolar ROM family offers a design alternative for high speed non-volatile read-only storage. Depending on number of patterns and number of devices required per pattern, systems cost savings may result from the use of devices in this section. Pin-compatible bipolar PROMs are available (through 4k density) and are described in Section 6 of this databook. Since a custom mask is involved for each pattern ordered, the user should allow sufficient lead time consistent with normal product flow and processing. Contact your National representative with details of your particular needs.

National Semiconductor

DM54S187/DM74S187 1024-Bit (256 × 4) Open-Collector ROM
DM75S97/DM85S97 1024-Bit (256 × 4) TRI-STATE® ROM

general description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high state, it causes all four outputs to go to the "OFF" or high impedance state. The memories are availabie in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

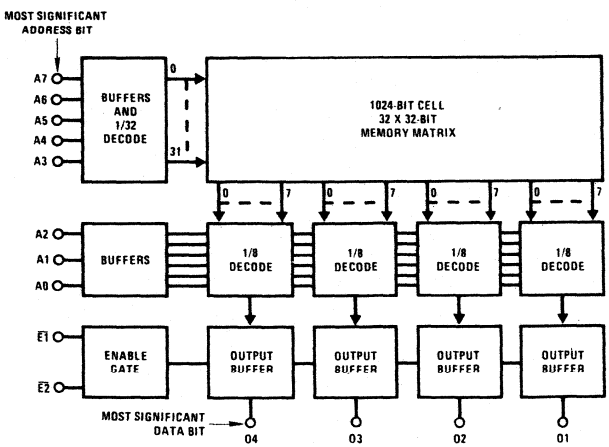
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Schottky-clamped for high speed
  - Address access—50 ns max
  - Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM74S287 and DM74S387

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S187		X	X		N, J
DM85S97		X		X	N, J
DM54S187	X		X		J
DM75S97	X			X	J

block diagram

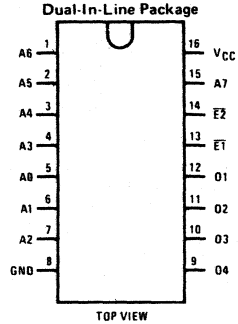


Order Number DM54S187J, DM74S187J, DM75S97J or DM85S97
See NS Package J16A

Order Number DM74S187N or DM85S97N
See NS Package N16A

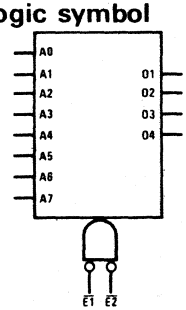
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



7

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S187, DM75S97	4.5	5.5	V
DM74S187, DM85S97	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S187, DM75S97	−55	+125	°C
DM74S187, DM85S97	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S187, 75S97			DM74S187, 85S97			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45V		−80	−250		−80	−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.7V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S187, 75S97 5V ±10%; −55°C to +125°C			DM74S187, 85S97 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*	10	35	60	10	35	50	ns
t_{EA}	Enable Access Time	*(Figure 2)*	5	15	30	5	15	25	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*	5	15	30	5	15	25	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

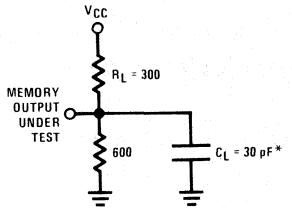
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH} or I_{CEX} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

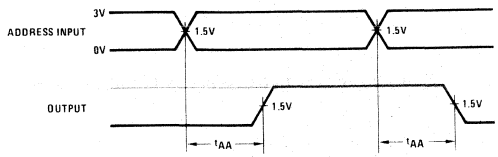


FIGURE 1. Address Access Time

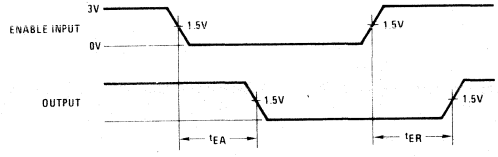
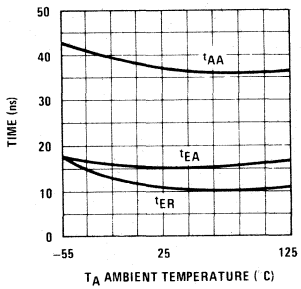


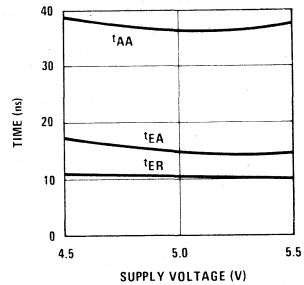
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

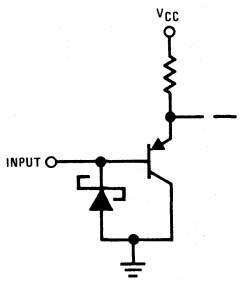


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

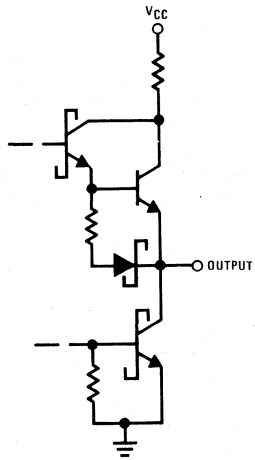


equivalent circuits

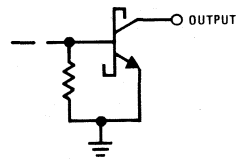
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

DM54S270/DM74S270 2048-Bit (512 × 4) Open-Collector ROM
DM54S370/DM74S370 2048-Bit (512 × 4) TRI-STATE® ROM

general description

These Schottky ROM memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

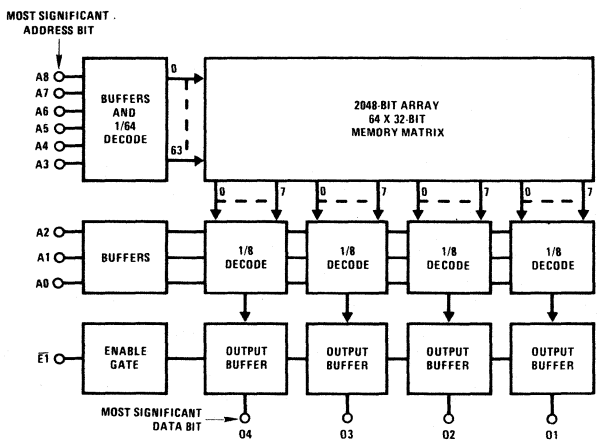
If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM74S570 and DM74S571

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S270		X	X		N, J
DM74S370		X		X	N, J
DM54S270	X		X		J
DM54S370	X			X	J

block diagram

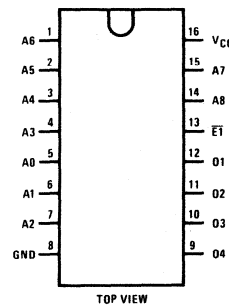


Order Number DM54S270J, DM54S370J, DM74S270J or DM74S370J
See NS Package J16A

Order Number DM74S270N or DM74S370N
See NS Package N16A

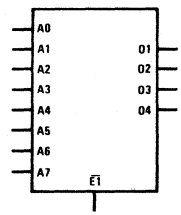
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.2V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S270, DM54S370	4.5	5.5	V
DM74S270, DM74S370	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S270, DM54S370	−55	+125	°C
DM74S270, DM74S370	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 2)

PARAMETER		CONDITIONS	DM54S270, 54S370			DM74S270, 74S370			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 3)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S270, 54S370 5V ±10%; −55°C to +125°C			DM74S270, 74S370 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			37	70		37	55	ns
t_{EA}	Enable Access Time			18	35		18	30	ns
t_{ER}	Enable Recovery Time			18	35		18	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 3: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM75S29/DM85S29 8192-Bit (1024 × 8) Open-Collector ROM
DM75S28/DM85S28 8192-Bit (1024 × 8) TRI-STATE® ROM

general description

These Schottky ROM memories are organized in the popular 1024 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

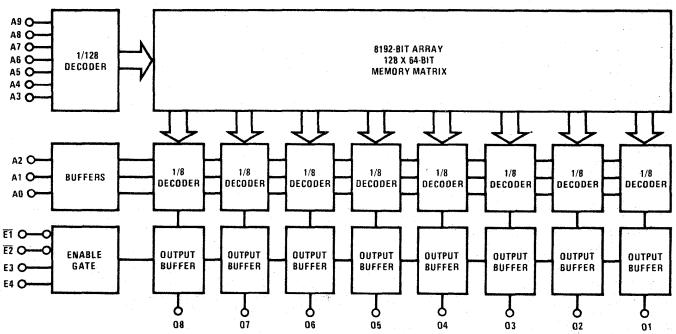
If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  Address access—70 ns max
  Enable access—45 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM87S229 and DM87S228

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM85S29		X	X		N, J
DM85S28		X		X	N, J
DM75S29	X		X		J
DM75S28	X			X	J

block diagram



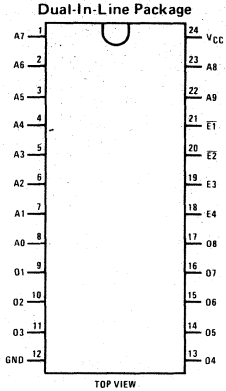
The device is enabled when: $\overline{E1} \cdot \overline{E2} \cdot E3 \cdot E4$

Order Number DM75S28J, DM75S29J, DM85S28J or DM85S29J
See NS Package J24A

Order Number DM85S28N or DM85S29N
See NS Package N24B

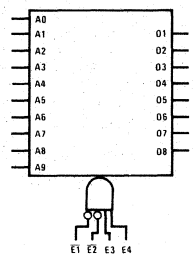
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.2V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM75S29, DM75S28	4.5	5.5	V
DM85S29, DM85S28	4.75	5.25	V
Ambient Temperature (T_A)			
DM75S29, DM75S28	−55	+125	°C
DM85S29, DM85S28	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 2)

PARAMETER		CONDITIONS	DM75S29, 75S28			DM85S29, 85S28			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 12 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		110	160		110	160	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 3)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM75S29, 75S28 5V ±10%; −55°C to +125°C			DM85S29, 85S28 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			47	90		47	70	ns
t_{EA}	Enable Access Time			30	50		30	45	ns
t_{ER}	Enable Recovery Time			30	50		30	45	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 3: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

Bipolar ROMs

DM7575/DM8575, DM7576/DM8576 Programmable Logic Array (PLA)

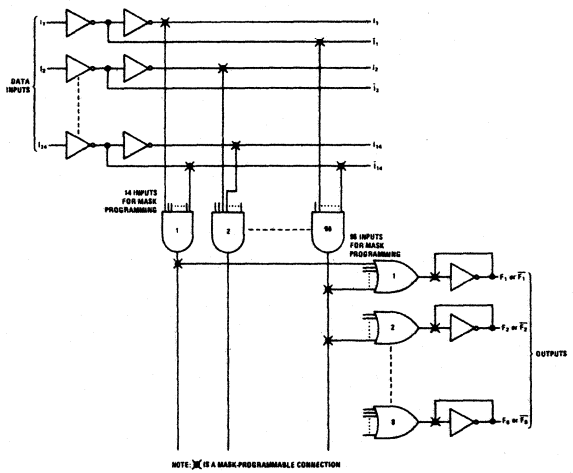
general description

The DM7575/DM8575 and DM7576/DM8576 are mask-programmable logic arrays designed for use in applications where random logic is required. The devices have fourteen data inputs and eight outputs. Each output provides a sum of product terms where each product term can contain any combination of 14 variables or their complements. The total number of product terms which can be provided is 96. Any product term which is repeated is counted only once. Since some functions are more easily represented in their inverted form, an option is provided to allow for either the true or complement of the function on each output. The products are particularly useful in providing control logic for digital systems. The DM7575/DM8575 has a conventional totem-pole output whereas the DM7576/DM8576 is provided with a passive pullup output. This latter configuration is useful in expanding functions by connection of outputs of different packages.

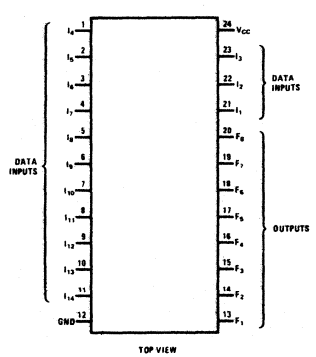
features

- A 2^{14}-by-8 (128K) bit memory would be needed to provide equivalent function
- Typical delay 90 ns
- Typical power dissipation 550 mW
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line Package



Order Number DM7575J, DM8575J, DM7576J or DM8576J
See NS Package J24A
Order Number DM8575N or DM8576N
See NS Package N24B

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7575, DM7576	4.5	5.5	V
DM8575, DM8576	4.75	5.25	V
Temperature (T_A)			
DM7575, DM7576	−55	+125	°C
DM8575, DM8576	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage (DM7575/DM8575 Only)	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V, I_{OUT} = −800μA	2.4			V
Logical "1" Output Current (DM7576/DM8576 Only)	V_{CC} = Max, V_{OUT} = 5.5V			100	μA
Logical "0" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V, I_{OUT} = +12 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.0	mA
Output Short Circuit Current (Note 3) DM7575/76	V_{CC} = Max, V_{OUT} = 0V	−20/−1.75		−55/−3.5	mA
Output Short Circuit Current (Note 3) DM8575/76	V_{CC} = Max, V_{OUT} = 0V	−18/−1.65		−55/−3.3	mA
Supply Current	V_{CC} = Max		110	170	mA
Input Diode Clamp Voltage	V_{CC} = Min, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Data Inputs to Outputs, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω		100	150	ns
Propagation Delay to a Logical "1" from Data Inputs to Outputs, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C		80	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7575/76 and across the 0°C to 70°C range for the DM8575/76. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

standard pattern

1. PART NO. – (DM7575AAA, DM8575AAA, DM7576AAA, DM8576AAA)
2. PATTERN IDENTIFICATION – Hollerith 29 (IBM) to ASCII
3. TOTAL NO. OF UNIQUE PRODUCT TERMS USED – 96
   (Repeated Terms Count Only Once)
4. OUTPUT INVERTER OPTION

F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1
T	T	T	T	T	T	T	T

5. MATRIX

PRODUCT TERM	INPUT DATA													OUTPUT DATA								CHAR. ASSIGN.
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	Space
2	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	1	!
3	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	"
4	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	1	#
5	0	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0	0	$
6	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	0	1	%
7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0	&
8	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	
9	0	0	0	1	0	0	1	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	(
10	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	)
11	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0	1	0	*
12	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1	+
13	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	1	1	0	0	,
14	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	1	–
15	0	0	0	1	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1	1	1	0	
16	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	1	1	/
17	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	1	1
19	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0	2
20	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	3
21	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	4
22	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1	0	1	5
23	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	0	6
24	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	7
25	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	8
26	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	1	9
27	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1	0	1	0	:
28	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	;
29	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	1	1	1	1	0	0	<
30	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	=
31	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	>
32	0	0	0	1	1	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	?
33	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	@
34	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	1	A
35	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	B
36	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	1	C
37	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	1	0	0	D
38	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	E
39	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	F
40	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	G
41	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	H
42	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	I
CARD ZONES			9	8	7	6	5	4	3	2	1	0	11	12	ODD PAR	b_7	b_6	b_5	b_4	b_3	b_2	b_1	ASCII BITS

standard pattern (con't)

PRODUCT TERM	INPUT DATA														OUTPUT DATA								CHAR. ASSIGN.
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
43	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	1	0	J
44	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	1	1	K
45	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	1	1	0	0	L
46	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	1	1	0	1	M
47	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	N
48	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	1	1	1	1	O
49	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	P
50	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	Q
51	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0	R
52	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0	1	1	S
53	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	T
54	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	1	0	1	0	1	U
55	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	1	1	0	V
56	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	1	1	1	W
57	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	X
58	0	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	0	1	Y
59	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	1	0	Z
60	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	1	1	0	1	1	[
61	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	1	0	0	\
62	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	1	1	1	0	1	]
63	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	0	^
64	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	1	1	1	_
65	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	
66	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	0	0	0	1	a
67	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	0	0	1	0	b
68	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	0	0	0	1	1	c
69	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	0	d
70	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	1	0	0	1	0	1	e
71	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1	1	0	0	1	1	0	f
72	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1	1	0	0	1	1	1	g
73	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	0	h
74	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	0	0	1	i
75	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1	0	j
76	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	1	0	1	1	k
77	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	0	1	1	0	0	l
78	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	0	1	1	0	1	m
79	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	1	0	1	1	1	0	n
80	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	o
81	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	p
82	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1	q
83	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	0	r
84	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	0	1	1	s
85	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	1	1	0	1	0	0	t
86	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0	1	0	1	u
87	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	1	0	1	1	0	v
88	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	1	1	1	0	1	1	1	w
89	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	x
90	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	y
91	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	0	z
92	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	1	{
93	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	0	0	!
94	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	1	0	1	}
95	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1	0	~
96	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	DEL
CARD ZONES			9	8	7	6	5	4	3	2	1	0	11	12	ODD PAR	b_7	b_6	b_5	b_4	b_3	b_2	b_1	ASCII BITS

information needed to program the PLA

Information to program the PLA can be supplied in one of two formats:

1. Punched 80-column cards
2. The applicable section of this data sheet (manual entry of information).

punched cards

CARD 1: (Used to determine whether outputs are presented in their true or inverted form. If this card is not used it is assumed that all eight outputs are true.)

Col. 1-6: DM7575 or DM8575 or DM7576 or DM8576.

Col. 7-9: (Blank)

Col. 10-17: Output Data. Outputs are F_8 (most significant) to F_1 (least significant). All eight outputs must be specified.

A 'T' in an output location indicates that the output is true.

A 'C' in an output location indicates that the output is complemented (inverted).

Col. 18-39: (Blank)

Col. 40-75: This space is reserved for any unique letters/numbers desired by the customer (special part number, program number, etc.). However the exact combination of characters must appear on all cards, but only those cards, associated with that particular device.

Col. 76-78: (Blank)

Col. 79-80: 00

CARDS 2-97: Term Data Cards. Used to specify the input and output conditions.

Col. 1-6: DM7575 or DM8575 or DM7576 or DM8576.

Col. 7-9: (Blank)

Col. 10-17: Output Connections. Outputs are F_8 (most significant) to F_1 (least significant). This field describes the outputs on which the product term appears.

A '+' in one of the eight output locations indicates that the term described by the card is one of the "OR" terms in that output.

A '(blank)' in one of the eight output locations indicates that the term described by the card is not one of the "OR" terms in that output.

(Care should be exercised in punching this particular field; since in most cases, unless a product term is repeated, this field will appear as one '+' and seven blanks.)

Col. 18: (Blank)

Col. 19: = (equal sign)

Col. 20: (Blank)

Col. 21-34: Input Data. Inputs are I_{14} (most significant) to I_1 (least significant).

An 'H' in one of the fourteen locations indicates that input appears in the high state in the output term.

An 'L' in one of the fourteen input locations indicates that input appears in the low state in the output term.

An 'X' in one of the fourteen input locations indicates that input does not appear in the output term.

Col. 35-39: (Blank)

Col. 40-75: This space is reserved for any unique letter/number desired by the customer (special part number, program number, etc.) However the exact combination of characters must appear on all cards, but only those cards, associated with that particular device. The purpose of this section is to prevent mixing of cards.

Col. 76-78: (Blank)

Col. 79-80: Product Term Number 01 to 96. (All 96 cards need not be used.) Zero in column 79 may be suppressed.

manual entry

The matrix-blank shown in this data sheet can be used in lieu of punched cards to submit information for programming the PLA.

INSTRUCTIONS

1. Circle the appropriate part number. In the event a catalog part is not being purchased, circle the closest catalog part number. If an electrical screen is required between the military and commerical devices, the military designation should be circled.
2. Customer should write the name of his company.
3. Enter the total number of unique product terms found in all eight outputs. Repeated terms count only once.
4. Output Inverter Option. Under the appropriate output designation specify a 'T' when the high (true) level is desired on the output for the given input conditions. Specify a 'C' if the complement is needed.
5. Matrix
   a. Input data. This block is used to describe what comprises each of the 96 (maximum) product terms. In each row, opposite the appropriate Product Term number, information on the fourteen Input Data locations is entered. Information must be entered on all 14 inputs.
      1). Enter an "H" under the appropriate input designation if that particular input appears in the product term as a high (true) level.
      2). Enter an "L" under the appropriate input designation if that particular input appears in the product term as a low (complemented) level.
      3). Enter an "X" under the appropriate input designation if that particular input does not appear in the product term.

      If less than 96 product terms are used leave all spaces for the unused terms blank.

   b. Output Data. This block is used to describe the outputs on which the product terms appear.
      1). Enter a '+' under the appropriate output designation if the product term is contained in that output's expression.
      2). Leave a location blank if the product term is not contained in that output's expression.

manual date entry
truth table/order blank

1. PART NO. — (DM7575, DM8575, DM7576, DM8576)

2. CUSTOMER IDENTIFICATION –

3. TOTAL NO. OF UNIQUE PRODUCT TERMS USED –
(Repeated Terms Count Only Once)

4. OUTPUT INVERTER OPTION

F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1

5. MATRIX

PRODUCT TERM	INPUT DATA														OUTPUT DATA								
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1		F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
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7

truth table/order blank (con't)

PRODUCT TERM	INPUT DATA															OUTPUT DATA								
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1		F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
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National Semiconductor

DM77S95/DM87S95 4096-Bit (512 × 8) Open-Collector ROM
DM77S96/DM87S96 4096-Bit (512 × 8) TRI-STATE® ROM

general description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

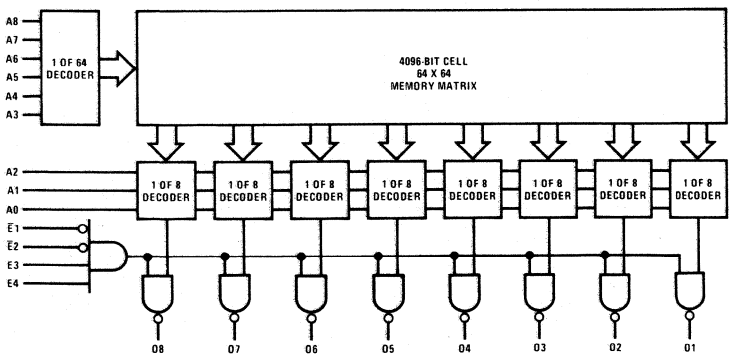
If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  Address access—65 ns
  Enable access—35 ns
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM74S474 and DM74S475

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S95		X	X		N, J
DM87S96		X		X	N, J
DM77S95	X		X		J
DM77S96	X			X	J

block diagram

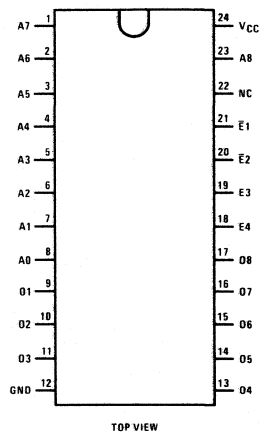


Order Number DM77S95J, DM77S96J
DM87S95J or DM87S96J
See NS Package J24A

Order Number DM87S95N or DM87S96N
See NS Package N24B

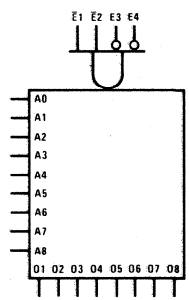
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



7

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM77S95, DM77S96	4.5	5.5	V
DM87S95, DM87S96	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S95, DM77S96	−55	+125	°C
DM87S95, DM87S96	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM77S95, 77S96			DM87S95, 87S96			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	170		115	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM77S95, 77S96 5V ±10%; −55°C to +125°C			DM87S95, 87S96 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	65	ns
t_{EA}	Enable Access Time			20	40		20	35	ns
t_{ER}	Enable Recovery Time			20	40		20	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 1 and pin 6).

Section 8

MOS ROMs

8

Program storage for microprocessors has become the fastest growing area of ROM application. As the performance of microprocessors and the sophistication of users increase, so will the requirements for large amounts of program storage. Also influencing larger ROM sizes is the trend toward higher level languages for microcomputers. The MAXI-ROM is a perfect vehicle for "Silicon Software" — which is National's name for putting high level languages such as INS8080A BASIC, PACE BASIC, and NIBL (National Industrial Basic Language) for the INS8060 (SC/MP) into mask-encoded ROM at a reasonable cost. Refer to National's Memory Applications Handbook for data on using the pin-compatible series of MAXI-ROMs. Refer to this section for data sheets and current Silicon Software.

National Semiconductor

MM1742 2048-Bit (256 × 8) ROM

general description

The MM1742 is a 2048-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 256 8-bit words. Programming of the memory is accomplished by storing a charge in a cell location by applying a −47V pulse. Although a PROM die is used, factory programming is required.

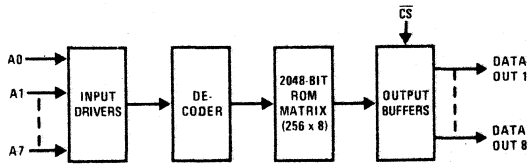
features

- Electrically programmed for fast turn-around
- Fully decoded, 256 x 8 organization
- Bipolar compatible
- TRI-STATE® outputs
- Pin compatible with the MM1702A, C1702A, and C1302.

applications

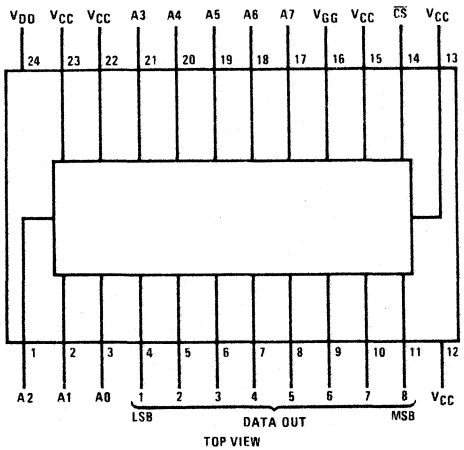
- Code conversion
- Table look-up
- Micro-programming
- Character generator
- Random logic synthesis

block and connection diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



Order Number MM1742J
See NS Package J24A

Pin Names

A0–A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT1} - D_{OUT8}$	Data Outputs

8

absolute maximum ratings (Note 1)

Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Power Dissipation	2W
Read Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	+0.5V to −20V
Lead Temperature (Soldering, 10 seconds)	300°C

dc characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C. (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Load Current	V_{IN} = 0V			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{CC} − 2			1	μA
I_{DD0}	Power Supply Current	V_{GG} = V_{CC}, $\overline{CS}$ = V_{CC} − 2 I_{OL} = 0 mA, T_A = 25°C, (Note 2)		5	10	mA
I_{DD1}	Power Supply Current	$\overline{CS}$ = V_{CC} − 2, I_{OL} = 0 mA, T_A = 25°C		35	50	mA
I_{DD2}	Power Supply Current	$\overline{CS}$ = 0, I_{OL} = 0 mA, T_A = 25°C		32	46	mA
I_{DD3}	Power Supply Current	$\overline{CS}$ = V_{CC} − 2, I_{OL} = 0 mA, T_A = 0°C		38.5	60	mA
I_{CF1}	Output Clamp Current	V_{OUT} = −1V, T_A = 0°C		8	14	mA
I_{CF2}	Output Clamp Current	V_{OUT} = −1V, T_A = 25°C			13	mA
I_{GG}	Gate Supply Current				1	μA
V_{IL1}	Input Low Voltage for TTL Interface		−1		V_{CC}−4.1	V
V_{IL2}	Input Low Voltage for MOS Interface		V_{DD}		V_{CC}−6	V
V_{IH}	Address and Chip Select Input High Voltage		V_{CC}−2		V_{CC}+0.3	V
I_{OL}	Output Sink Current	V_{OUT} = 0.45V	1.6	4		mA
I_{OH}	Output Source Current	V_{OUT} = 0V	−2			mA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		−0.7	0.45	V
V_{OH}	Output High Voltage	I_{OH} = −100μA	3.5	4.5		V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2: Power-Down Option: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option, please specify MM1742ALJ.

ac characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNITS
Freq.	Repetition Rate			1	MHz
t_{0H}	Previous Read Data Valid			100	ns
t_{ACC}	Address to Output Delay		0.7	1	μs
t_{DVGG}	Clocked V_{GG} Set-Up,(Note 1)	1			μs
t_{CS}	Chip Select Delay			100	ns
t_{CO}	Output Delay From $\overline{CS}$			900	ns
t_{OD}	Output Deselect			300	ns
t_{OHC}	Data Out Hold in Clocked V_{GG} Mode, (Note 1)			5	μs

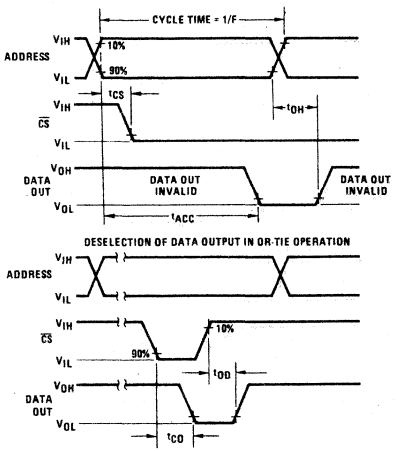
capacitance characteristics $T_A = 25°C$ (Note 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	All Unused	$V_{IN} = V_{CC}$		8	15	pF
C_{OUT}	Output Capacitance	Pins Are	$\overline{CS} = V_{CC}$		10	15	pF
C_{VGG}	V_{GG} Capacitance, (Note 1)	At ac Ground	$V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$			30	pF

Note 3: This parameter is periodically sampled and is not 100% tested.

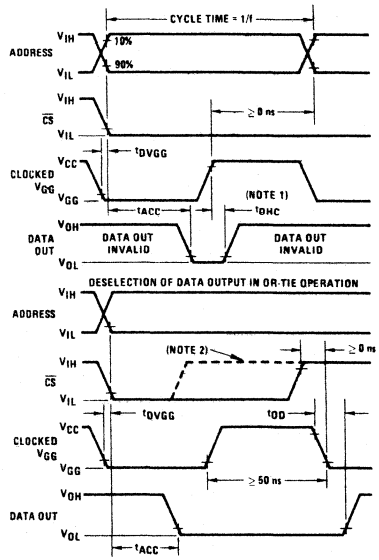
read operation switching time waveforms

(a) Constant V_{GG} Operation



Conditions of Test:
Input pulse amplitudes: 0–4V, t_r, $t_f \leq 50$ ns.
Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leq 15$ ns,) $C_L = 15$ pF.

(b) Power-Down Option (Note 1)

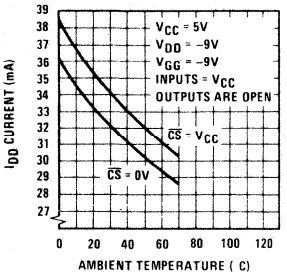


Note 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

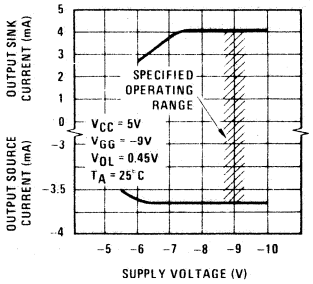
Note 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

typical performance characteristics

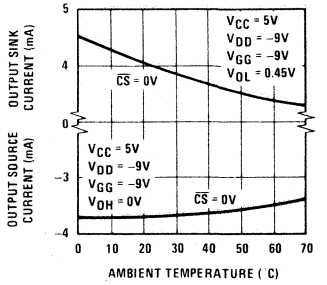
I_{DD} Current vs Temperature



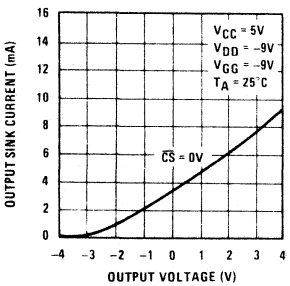
Output Current vs V_{DD} Supply Voltage



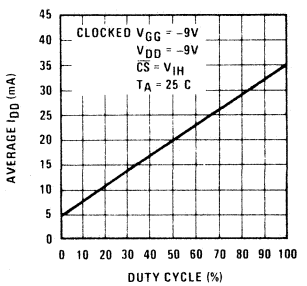
Output Current vs Ambient Temperature



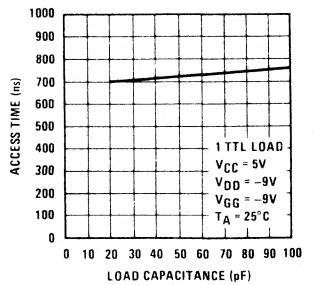
Output Sink Current vs Output Voltage



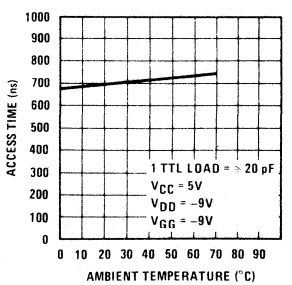
Average Current vs Duty Cycle for Clocked V_{GG} (Note 1)



Access Time vs Load Capacitance



Access Time vs Temperature



National Semiconductor

MM2316A 16,384-Bit (2048 × 8) ROM

general description

The MM2316A is a static MOS 16,384-bit read-only memory organized in a 2048-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode silicon-gate technology which provides complete DTL/TTL compatibility and single power-supply operation.

Three programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing one mask during fabrication.

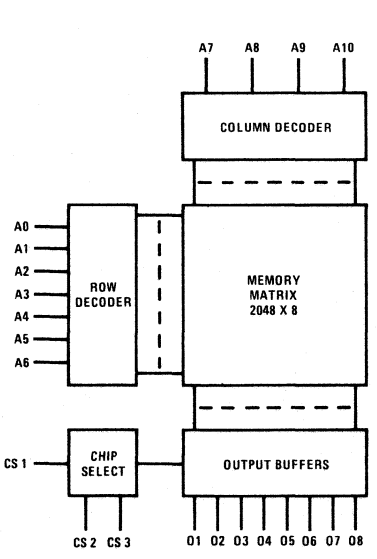
features

- Fully decoded
- Single 5V power supply
- Inputs and outputs TTL compatible
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048 word by 8-bit organization
- Maximum access time—450 ns

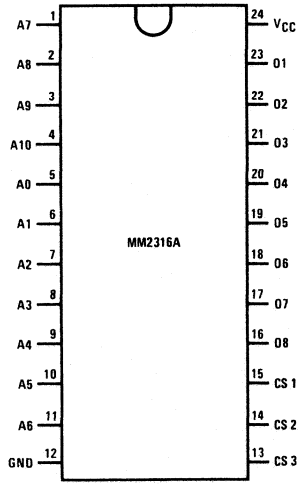
applications

- Microprogramming
- Control logic
- Table look-up

block and connection diagrams



Dual-In-Line Package

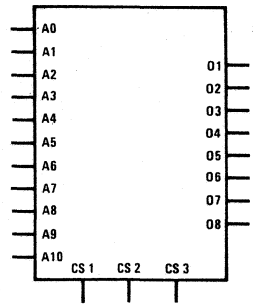


TOP VIEW

Order Number MM2316AJ
See NS Package J24A

Order Number MM2316AN
See NS Package N24A

logic symbol



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise noted).

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Current (I_{LI})	V_{IN} = 0 to V_{CC}			10	μA
Logical "1" Input Voltage (V_{IH})		2.0		V_{CC}+1.0	V
Logical "0" Input Voltage (V_{IL})		−0.5		0.8	V
Logical "1" Output Voltage (V_{OH})	I_{OH} = −100 μA	2.2			V
Logical "0" Output Voltage (V_{OL})	I_{OL} = 2 mA			0.45	V
Output Leakage Current (I_{LOH})	V_{OUT} = 4V, CS = 2.2V			10	μA
Output Leakage Current (I_{LOL})	V_{OUT} = 0.45V, CS = 2.2V			−20	μA
Power Supply Current (I_{CC1})	All Inputs = 5.25V, Data Output Open		40	98	mA

capacitance

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Capacitance (All Inputs) (C_{IN})	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
Output Capacitance (C_{OUT})	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

ac electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise specified).
See ac test circuit and switching time waveforms.

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{ACCESS}	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 1)*			450	ns
t_{SELECT}	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 2)*			300	ns
$t_{DESELECT}$	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 2)*			300	ns

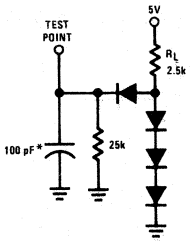
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

ac test circuit and switching time waveforms



*Includes jig capacitance

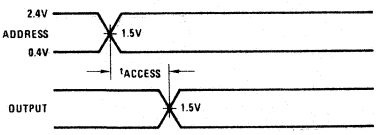


FIGURE 1. Access Time

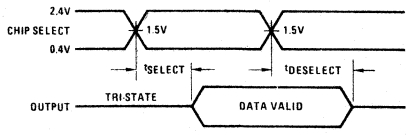


FIGURE 2. Output Enable and Disable

custom ROM programming

Custom ROM programs are submitted to National in three formats: paper tape, punched cards or truth table, with punched cards being the preferred. These programs are converted into machine language and outputted on a magnetic tape. This magnetic tape is used to make the programmable mask and the test tape. The wafers are tested at the wafer level. The wafer is then scribed and the good dice assembled. After assembly, the units are tested using the custom test tape to assure the correct output pattern for every address.

National has programs to convert NEGATIVE logic to POSITIVE or POSITIVE to NEGATIVE so ROMs can be entered in either logic, but the customer must specify which logic definition is used.

PROGRAMMING DEFINITIONS

Logic Definitions

NEGATIVE Logic: "0" = V_H = the more positive voltage. "1" = V_L = the more negative voltage.

POSITIVE Logic: "0" = V_L = the more negative voltage. "1" = V_H = the more positive voltage.

Input/Output Definitions

Address: A0 is the least significant input address.

Outputs: O1 is the least significant output.

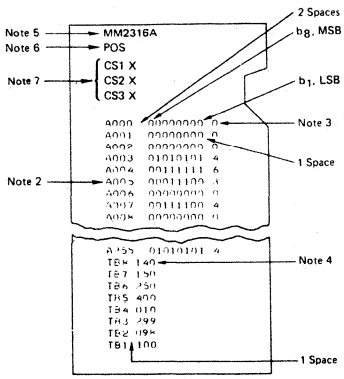
Custom ROM Programming

INFORMATION NEEDED

So that National can better serve its customers, the following information *must* be submitted with each ROM code.

National Semiconductor Corporation 2900 Semiconductor Dr., Santa Clara, CA 95051 Phone (408) 737-5000 TWX 910-339-9240			NATIONAL PART NUMBER
			ROM LETTER CODE (NATIONAL USE ONLY)
NAME			DATE
ADDRESS			CUSTOMER PRINT OR I.D. NO.
CITY		STATE ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE	DATE

tape entry format (Note 1)



MM2316A

8-Bit Tape Format

Note 1: The code is a 7-bit ASCII code on 8 punch tape.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

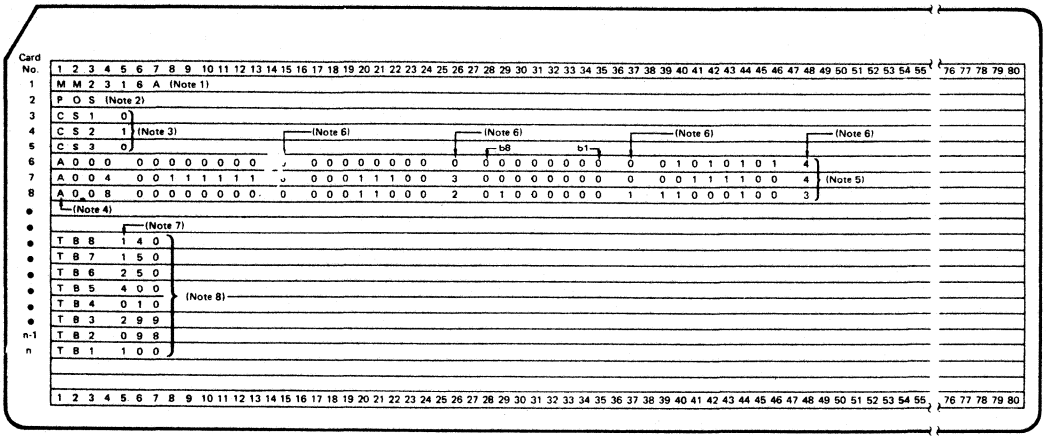
Note 4: The total number of "1" bits in each output column or bit position.

Note 5: Specify product type.

Note 6: Must type POS logic, or NEG logic depending on which is used. Logic on addresses and outputs must be the same (either POS or NEG).

Note 7: Specify the pattern necessary to select the ROM.

card entry format



Note 1: Specify product type.

Note 2: Must type POS logic or NEG logic depending on which is used. Logic on addresses, outputs and chip selects must be the same (either POS or NEG).

Note 3: Specify the chip select logic levels that will enable the ROM.

Note 4: The first ROM input address per card is expressed in decimal form and is preceded by the letter A.

Note 5: Punch four address locations per card, only first location on each card has the address location expressed in decimal form

Note 6: The total number of "1" bits in the output word.

Note 7: Leading zeros must be punched.

Note 8: The total number of "1" bits in each output column or bit position

National Semiconductor

MM4210/MM5210 1024-Bit (256 × 4) ROM

general description

The MM4210/MM5210 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

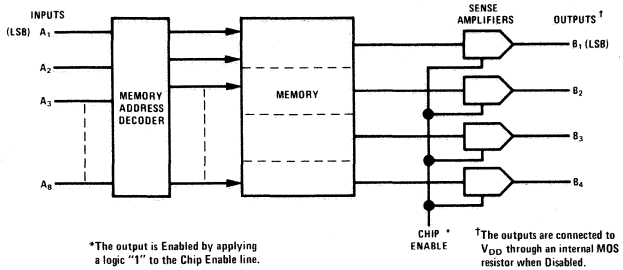
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

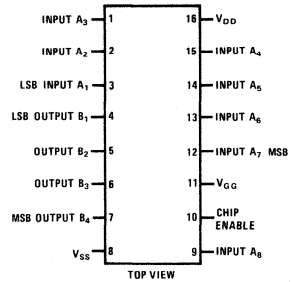
block and connection diagrams



*The output is Enabled by applying a logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

Dual-In-Line Package

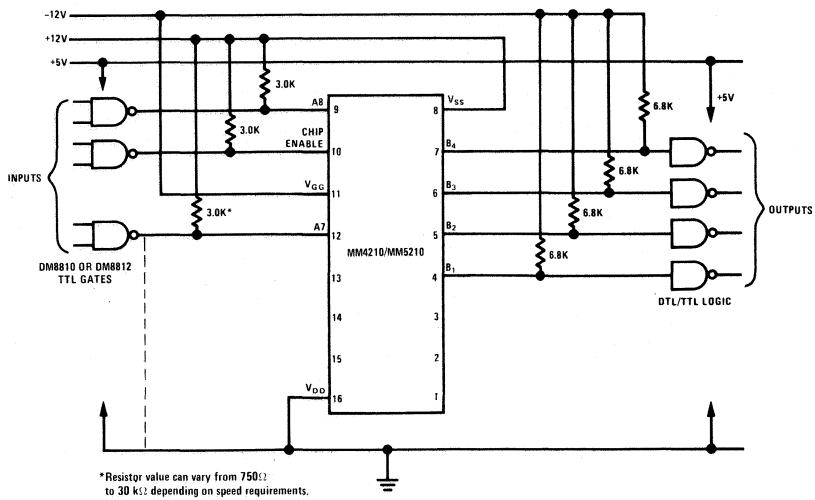


Order Number MM4210J or MM5210J
See NS Package J16A

Order Number MM5210N
See NS Package N16A

typical application

256 x 4 Bit ROM Showing TTL Interface



*Resistor value can vary from 750Ω to 30 kΩ depending on speed requirements.

Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

V_{GG} Supply Voltage	$V_{SS}-30V$
V_{DD} Supply Voltage	$V_{SS}-15V$
Input Voltage	$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature MM4210	$-55^{\circ}C$ to $+125^{\circ}C$
" MM5210	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

electrical characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load			$V_{SS}-9.0$	V
Logical "0"		$V_{SS}-1.0$			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				$V_{SS}-8.0$	V
Logical "0"		$V_{SS}-2.0$			V
Power Supply Current	$T_A = 25^{\circ}C$				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}-12V$			1	μA
Input Capacitance	f = 1.0 MHz $V_{IN} = 0V$		5		pF
Access Time (Notes 2, 3)	$T_A = 25^{\circ}C$				
T_{ACCESS}	(See Timing Diagram) $V_{SS} = +12V$ $V_{GG} = -12V$	150	500	650	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

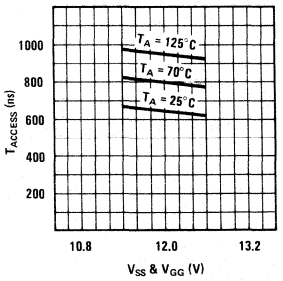
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

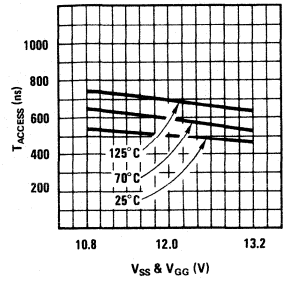
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

performance characteristics

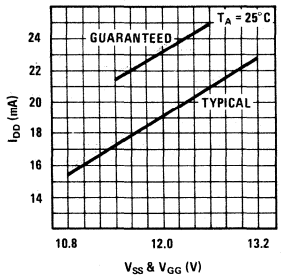
Guaranteed Access Time vs Supply Voltages



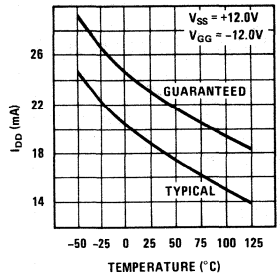
Typical Access Time vs Supply Voltages



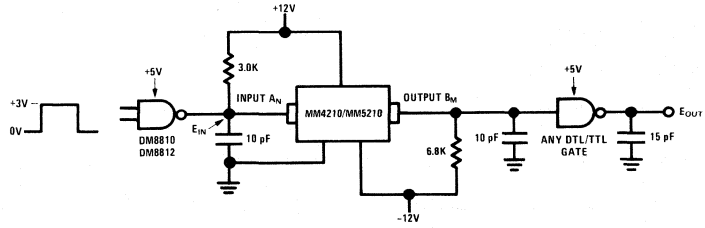
Power Supply Current vs Voltage

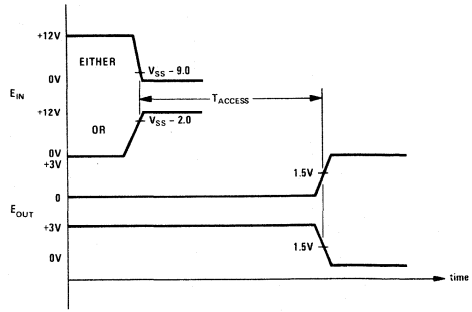


Power Supply Current vs Temperature



timing diagram/address time





8

National Semiconductor

MM4211/MM5211 1024-Bit (256 × 4) ROM

general description

The MM4211/MM5211 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication.

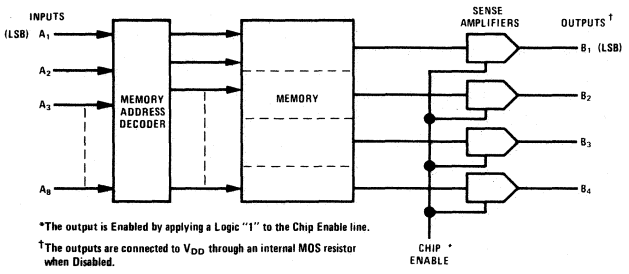
features

- Bipolar compatibility +5V, −12V operation
- High speed operation < 700 ns typ
- Static operation no clocks required
- Common data busing output wire AND capability
- Chip enable output control

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

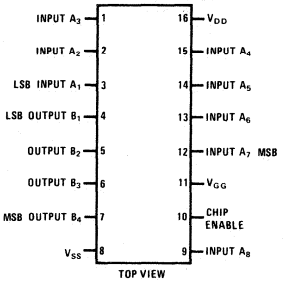
block and connection diagrams



*The output is Enabled by applying a Logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

Dual-In-Line Package

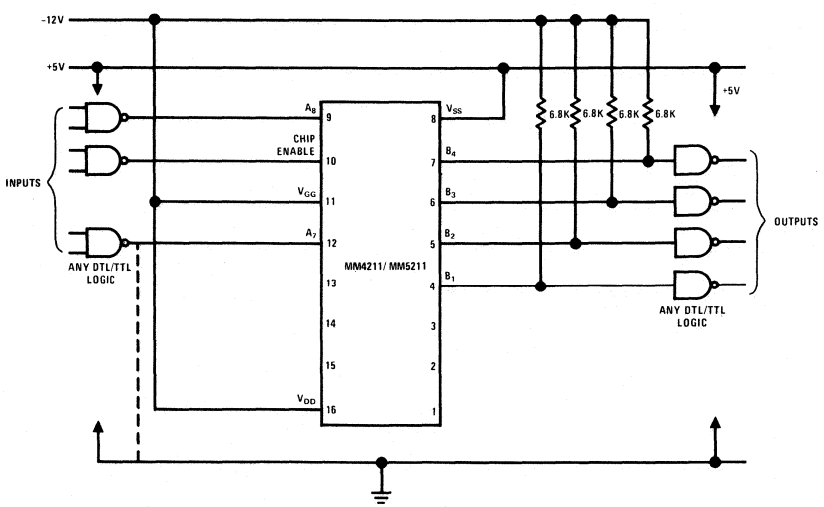


Order Number MM4211J or MM5211J
See NS Package J16A

Order Number MM5211N
See NS Package N16A

typical application

256 x 4 Bit ROM Showing TTL Interface



Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	–65°C to +150°C
Operating Temperature MM4211	–55°C to +125°C
MM5211	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = V_{DD} = –12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8K ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	V_{GG} = V_{DD} = –12V			1	μA
Input Leakage	V_{IN} = V_{SS} – 12V			1	μA
Input Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = 5V V_{GG} = V_{DD} = –12V		700	950	ns
Output AND Connection (Note 3)	6.8K ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

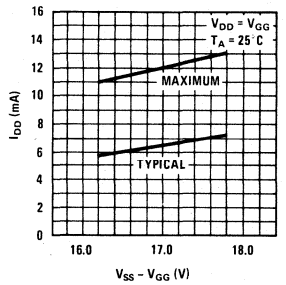
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N –1) (50) ns
Where N = Number of AND connections.

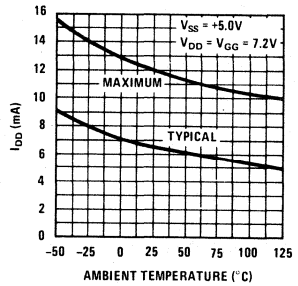
Note 4: Capacitance guaranteed by design.

performance characteristics

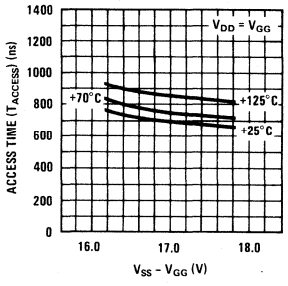
Power Supply Current vs
Power Supply Voltages



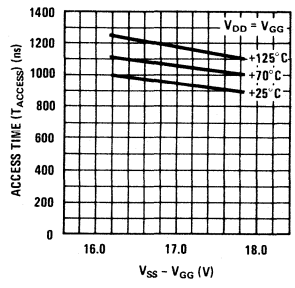
Power Supply Current vs
Ambient Temperature



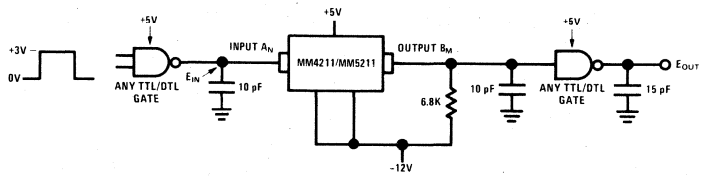
Typical Access Time vs
Power Supply Voltages

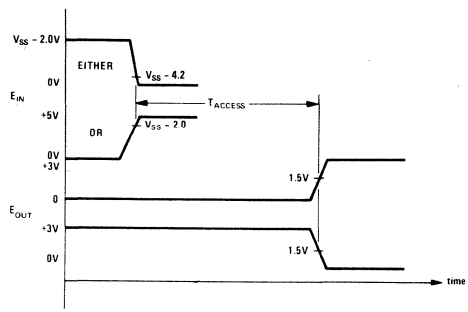


Guaranteed Access Time vs
Power Supply Voltages



timing diagram/address time





National Semiconductor

MM5212 12,288-Bit (1024 × 12) ROM

general description

The MM5212 12,288-bit read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology and ion-implanted resistors. Open drain outputs provide a TTL compatible wire OR capability with the addition of a 6.8 kΩ resistor. The ROM is organized in a 1024 word by 12-bit organization.

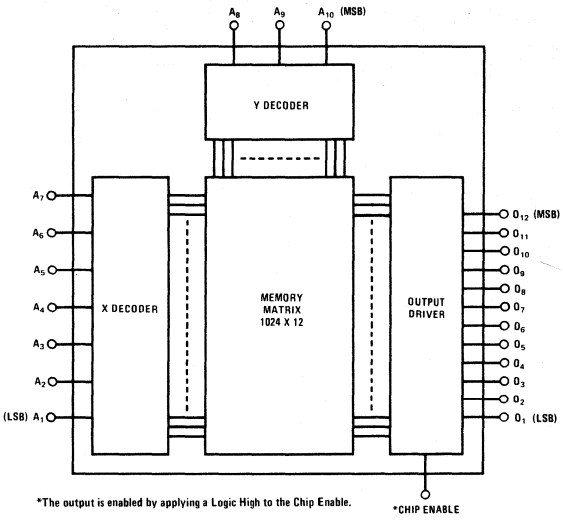
features

- Standard supplies +5.0V, −12V
- Open drain outputs Wire OR capability
- Static operation No clocks
- TTL compatible inputs and outputs

applications

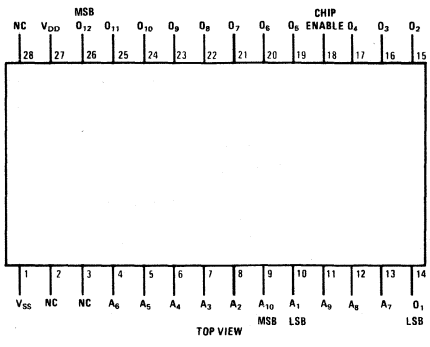
- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

block diagram



connection diagram

Dual-In-Line Package



Note: For programming information see Memory Applications Handbook, page 4-6.

Order Number MM5212AD
See NS Package D28A

Order Number MM5212AN
See NS Package N28A

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.5V to V_{SS} − 22V
Power Dissipation at 25°C Ambient	800 mW
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

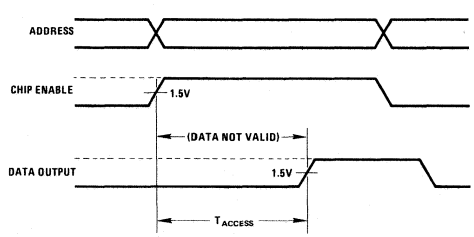
electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels (Note 1)					
Logical High Level (V_{IH})		+2.8			V
Logical Low Level (V_{IL})				+0.8	V
Data Output Levels (Note 1)					
Logical High Level (V_{OH})	6.8 kΩ ±5% to V_{DD} Plus One	+2.4			V
Logical Low Level (V_{OL})	Standard Series 54/74 Gate			+0.4	V
Output Current Capability					
Logical High Level (V_{IH})	V_{OUT} = 2.4V	2.5			mA
Power Supply Current	T_A = 25°C, V_{SS} = +5.0V				
I_{DD}	V_{DD} = −12V		6.0	10.0	mA
Standby Power Dissipation	V_{SS} = +5.0V, V_{DD} = −12V Chip Enable LOW			170.0	mW
Input Leakage	V_{IN} = V_{SS} −10V			1.0	μA
Address Time	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = +5.0V V_{DD} = −12V		3.5	5.0	μs

Note 1: Positive logic definition.

switching time waveforms



National Semiconductor

MM4213/MM5213 2048-Bit (256 x 8 or 512 x 4) ROM

general description

The MM4213/MM5213 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

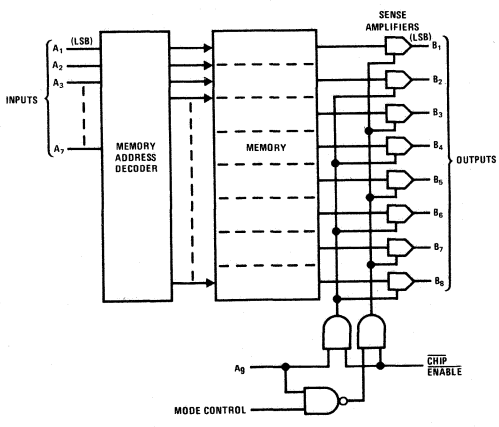
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 600 ns typ
- Pin compatible with MM5203 PROM
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control
- TRI-STATE output

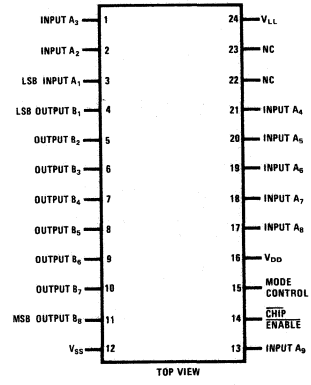
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



Dual-In-Line Package



Order Number MM4213J
or MM5213J
See NS Package J24A

Order Number MM5213N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

V_{LL} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.3)\ V$
Storage Temperature	–65°C to +150°C
Operating Temperature MM4213	–55°C to +125°C
MM5213	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics POSITIVE LOGIC (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Capability					
Logical "1"	V_{OUT} = 2.4V	200			μA
Logical "0"	V_{OUT} = 0.4V	–1.6			mA
Input Voltage Levels					
Logical "0"				V_{SS} – 4.0	V
Logical "1"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{SS} (Note 2)	V_{SS} = +5V $V_{LL} = V_{DD}$ = –12V		20	35	mA
Input Leakage	V_{IN} = –12V			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		5		pF
Address Time					
T_{ACCESS}	T_A = 25°C, V_{SS} = +5.0V $V_{GG} = V_{DD}$ = –12.0V		600	850	ns
Output AND Connections (Note 4)				10	

Note 1: These specifications apply for V_{SS} = +5.0V ±5%, V_{LL} = –12V, and T_A = –55°C to +125°C (MM4213), T_A = –25°C to +70°C (MM5213) unless otherwise specified.

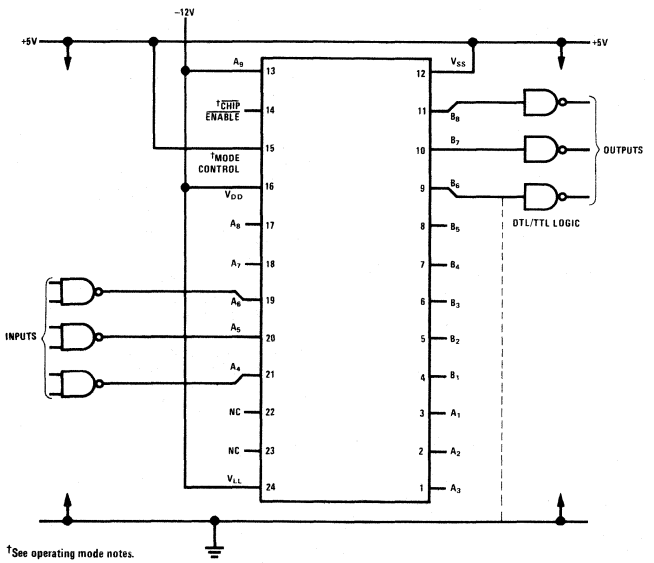
Note 2: Outputs open.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate.

Note 4: The address time in the TTL load configuration follows the equation: T_{ACCESS} = The specified limit + (N – 1) (25) ns. Where N = Number of AND connections.

Note 5: Capacitances are measured on a lot sample basis only.

typical applications (con't)



Operating Modes

256x8 ROM connection (shown)
Mode Control – Logic "1"
A_9 – Logic "0"

512x4 ROM connection
Mode Control – Logic "0"
A_9 – Logic "1" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "0" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "0" is applied to the Chip Enable line.

Mode Control should be "hard wired" to V_{LL} (Logical "0") or V_{SS} (Logical "1").

National Semiconductor

MM4214/MM5214 4096-Bit (512 × 8) ROM

general description

The MM4214/MM5214 4096-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit memory organization.

Customer programs may be submitted for production in a paper tape or punched card format.

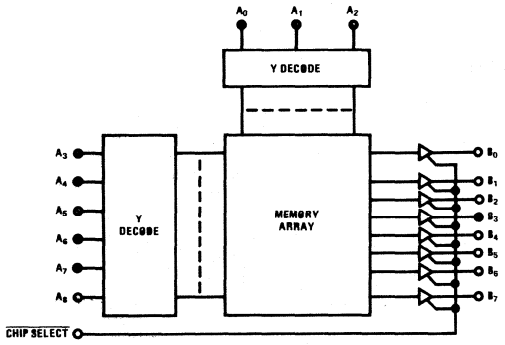
features

- Pin compatible with MM5204 PROM
- Bipolar compatibility — No external components required
- Standard supplies — +5.0V, −12V
- Bus ORable output — TRI-STATE outputs
- Static operation — No clocks required

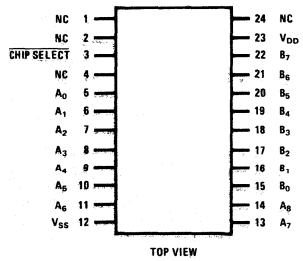
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package

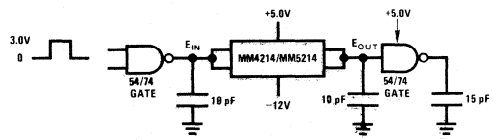


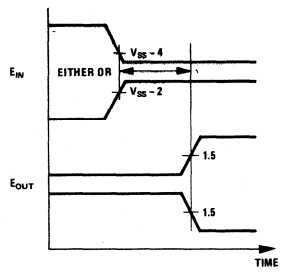
TOP VIEW

Order Number MM4214J or MM5214J
See NS Package J24A

Order Number MM5214N
See NS Package N24B

timing diagram/address time





Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

V_{DD} Supply Voltage V_{SS} − 20V

Input Voltage $(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.03)\ V$

Storage Temperature Range −65°C to +150°C

Operating Temperature Range

MM4214 −55°C to +125°C

MM5214 −25°C to +70°C

Lead Temperature (Soldering, 10 seconds) 300°C

electrical characteristics POSITIVE LOGIC

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical Low Level (V_{IL})	I_L = 1.6 mA Sink			0.4	V
Logical High Level (V_{IH})	I_L = 100μA Source	2.4			V
Input Voltage Levels					
Logical Low Level (V_L)				V_{SS}−4.0	V
Logical High Level (V_H)		V_{SS}−2.0			V
Power Supply Current (I_{SS}) (Note 4)	V_{SS} = 5.0V, V_{DD} = −12V, T_A = 25°C		23	37	mA
Input Leakage	$V_{IN} = V_{SS} - 10V$			1.0	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5.0	10	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4.0	10	pF
Address Time (T_{ACCESS}) (Note 2)	V_{DD} = −12V, V_{SS} = 5.0V, T_A = 25°C	150		1000	ns
Output AND Connections (Note 3)				20	

Note 1: Capacitances are measured periodically only.

Note 2: Address is measured from the change of data on any input or chip enable line to the output of a TTL gate. (See Timing Diagram.)

Note 3: The address time follows the following equation: T_{ACCESS} = The specified limit + (N−1) x 25 ns where N = Number of AND connections.

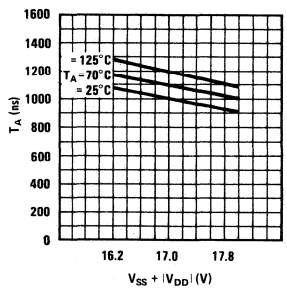
Note 4: Outputs open.

Note 5: Positive true logic notation is used. Logic "1" = most positive voltage level. Logic "0" = most negative voltage level.

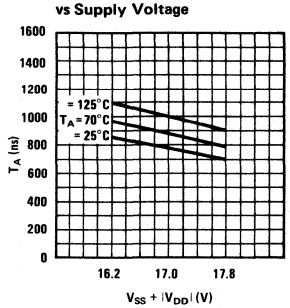
Note 6: Chip is enabled when Chip Select is low.

typical performance characteristics

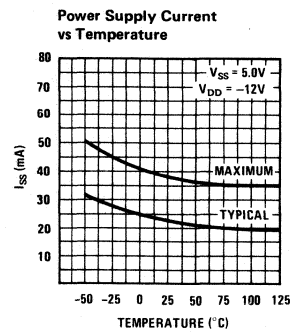
Guaranteed Access Time vs Supply Voltage



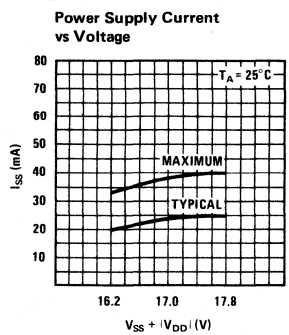
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature



Power Supply Current vs Voltage



National Semiconductor

MM5215 12,288-Bit (1024 × 12) ROM

general description

The MM5215 12,288-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology and ion-implanted resistors. TRI-STATE® outputs provide wire-OR capability without loading common data lines or reducing system access times. The ROM is organized in a 1024 x 12 bit word configuration. The V_{GG} supply may be brought to 0V to reduce internal power dissipation in the non-enabled mode to 10μW/bit.

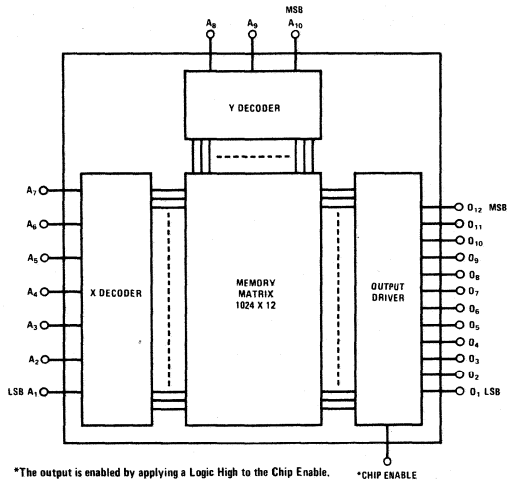
features

- Static operation
- TRI-STATE outputs
- No clocks required
- +12V and −12V supplies
- Pin compatible with E.A. 3800

applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

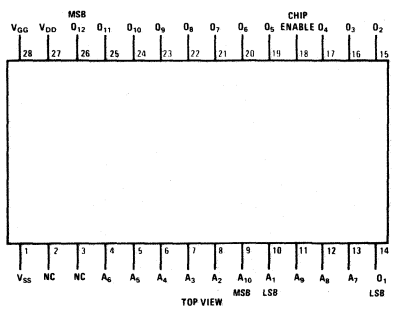
block diagram



*The output is enabled by applying a Logic High to the Chip Enable.

connection diagram

Dual-In-Line Package



Note: For programming information see Memory Applications Handbook, page 4-6.

Order Number MM5215AD
See NS Package D28A

Order Number MM5215AN
See NS Package N28A

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} +0.5V to V_{SS} −30V
Input Voltage	V_{SS} +0 5V to V_{SS} −30V
Power Dissipation at 25°C Ambient	800 mW
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

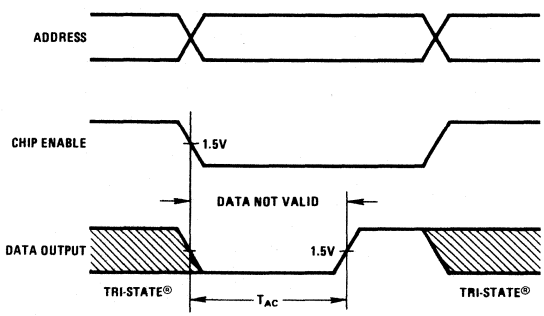
electrical characteristics

T_A within operating temperature range V_{SS} = +12V ±1.0V, V_{DD} = 0V, V_{GG} = −12V ±1.0V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Levels					
Logical "1"	(Note 1)			V_{SS} − 9.0	V
Logical "0"	(Note 1)	V_{SS} − 2.0			V
Output Voltage Levels					
Logical "1"	No Load			V_{DD}	V
Logical "0"	No Load	V_{SS}			V
Output Current					
Logical "1"	V_O = V_{SS}	2.5	15.0		mA
	V_O = V_{SS} − 6.0V	0.7	7.0		mA
Logical "0"	V_O = V_{SS} − 12V	−2.0	−6.5		mA
	V_O = V_{SS} − 6.0V	−1.5	−5.0		mA
Power Supply Current					
I_{SS}	V_{SS} = +13V, V_{DD} = 0V, V_{GG} = −13V			30	mA
I_{GG}	V_{SS} = +13V, V_{DD} = 0V, V_{GG} = −13V			15	mA
Standby Power Dissipation	V_{SS} = +12V, V_{DD} = 0V V_{GG} = 0V, T_A = 25°C			150	mW
	V_{SS} = +12V, V_{DD} = 0V V_{GG} = −12V, T_A = 25°C			300	mW
Address Time					
T_{ACCESS}	T_A = 25°C		1.0	1.5	μs

Note 1: Negative logic definition.

switching time waveforms



National Semiconductor

MM4220/MM5220 1024-Bit (128 x 8 or 256 x 4) ROM

general description

The MM4220/MM5220 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

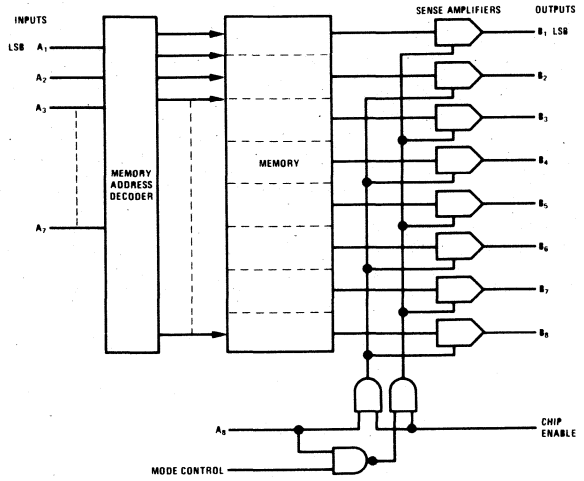
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

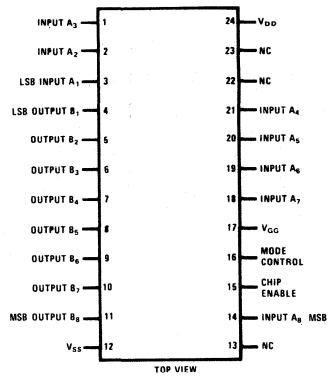
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

block and connection diagrams



Dual-In-Line Package



Order Number MM4220J
or MM5220J
See NS Package J24A

Order Number MM5220N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

8

absolute maximum ratings

V_{GG} Supply Voltage		$V_{SS}-30V$
V_{DD} Supply Voltage		$V_{SS}-15V$
Input Voltage		$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature		$-65°C$ to $+150°C$
Operating Temperature	MM4220	$-55°C$ to $+125°C$
	MM5220	$0°C$ to $+70°C$
Lead Temperature (Soldering, 10 sec)		$300°C$

electrical characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			$V_{SS}-9.0$	V
Logical "0"		$V_{SS}-1.0$			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				$V_{SS}-8.0$	V
Logical "0"		$V_{SS}-2.0$			V
Power Supply Current	$T_A = 25°C$				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}-12V$			1	μA
Input Capacitance	$f = 1.0$ MHz $V_{IN} = 0V$		5		pF
Access Time (Notes 2, 3)	$T_A = 25°C$				
T_{ACCESS}	(See Timing Diagram) $V_{SS} = +12V$ $V_{GG} = -12V$	150	500	650	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

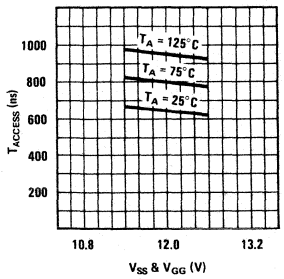
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

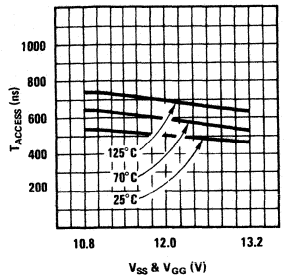
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

performance characteristics

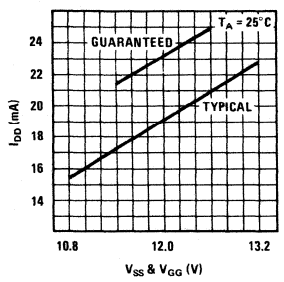
Guaranteed Access Time vs Supply Voltages



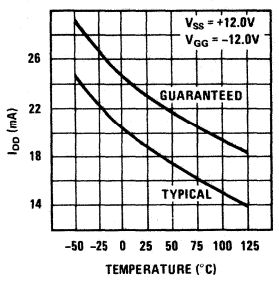
Typical Access Time vs Supply Voltages



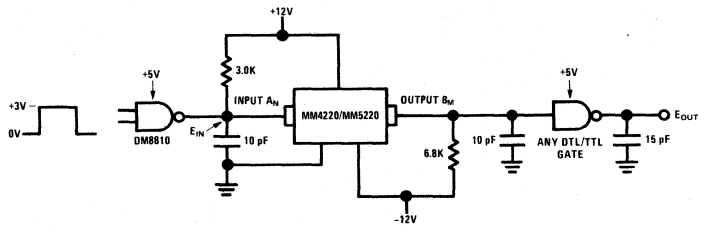
Power Supply Current vs Voltage

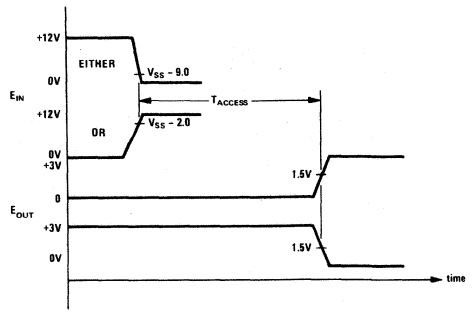


Power Supply Current vs Temperature



timing diagram/address time

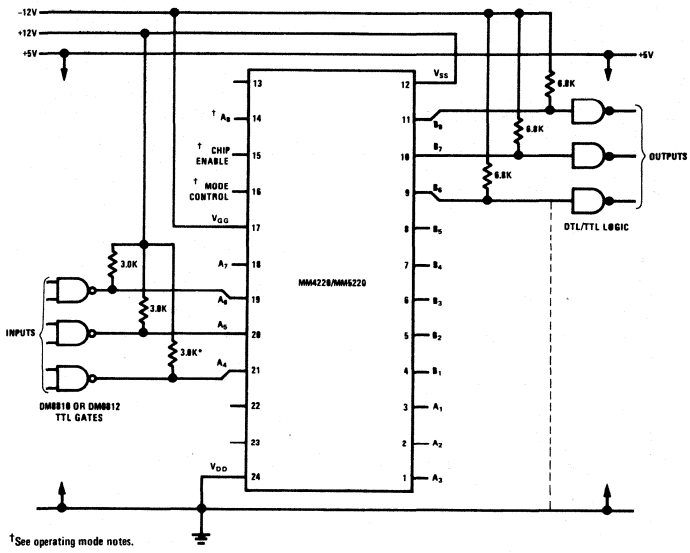




8

typical application

128-8 Bit ROM Showing TTL Interface



†See operating mode notes.

*R values can vary from 740 to 30 kΩ depending on speed requirements.

OPERATING MODES

128x8 ROM connection
Mode Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_8 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

The logic levels are in negative voltage logic notation.

MM4221/MM5221 1024-Bit (128 x 8 or 256 x 4) ROM

general description

The MM4221/MM5221 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

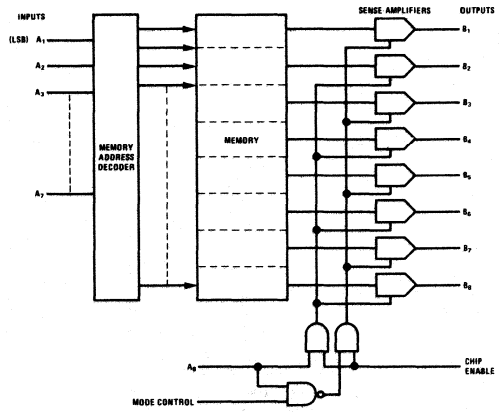
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — <700 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control

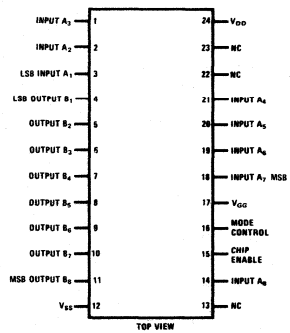
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

block and connection diagrams



Dual-In-Line Package



Order Number MM4221J
or MM5221J
See NS Package J24A

Order Number MM5221N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{DD} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		−65°C to +150°C
Operating Temperature	MM4221	−55°C to +125°C
	MM5221	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = V_{DD} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	V_{GG} = V_{DD} = −12V			1	μA
Input Leakage	V_{IN} = V_{SS} – 12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = 5V, V_{GG} = V_{DD} = −12V		700	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

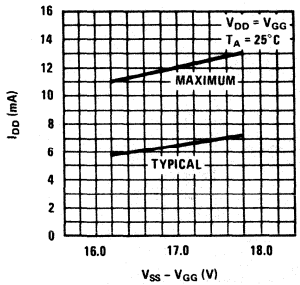
Note 2: Address time is measured from the change of data on any input except mode control or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns
Where N = Number of AND connections.

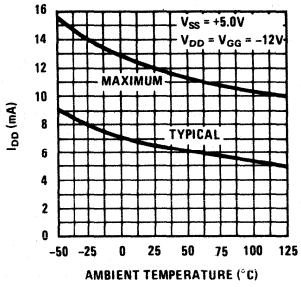
Note 4: Capacitance guaranteed by design.

performance characteristics

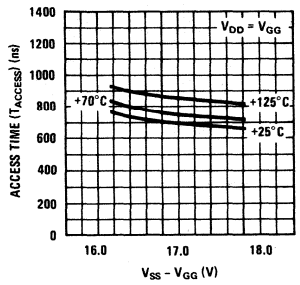
Power Supply Current vs
Power Supply Voltages



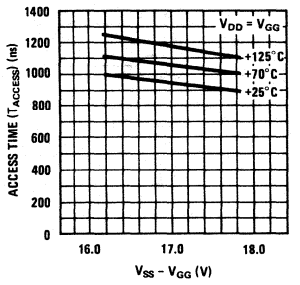
Power Supply Current vs
Ambient Temperature



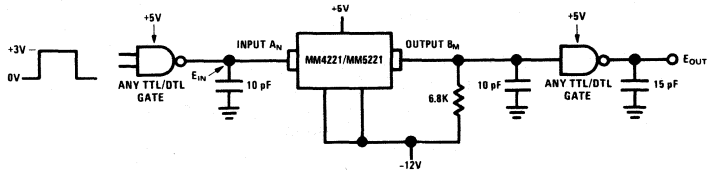
Typical Access Time vs
Power Supply Voltages

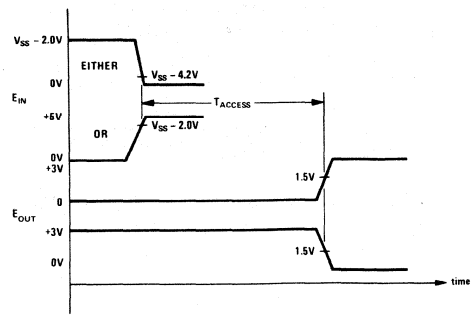


Guaranteed Access Time vs
Power Supply Voltages



timing diagram/address time

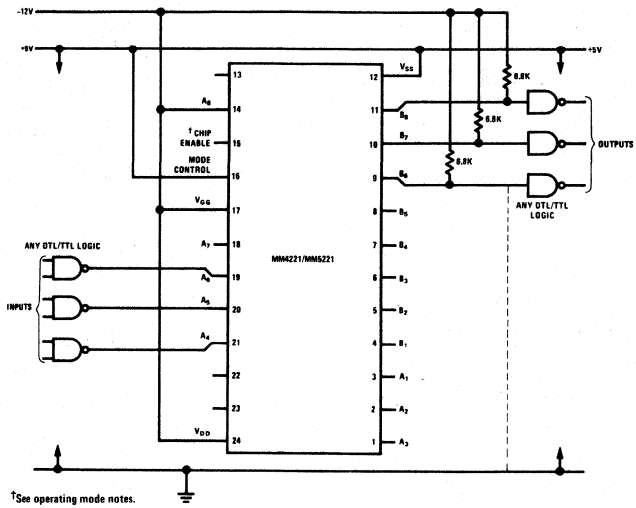




8

typical application

128-8 Bit ROM Showing TTL Interface



OPERATING MODES

128x8 ROM connection
Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Control – Logic "1"
A_8 – Enables the odd ($B_1 \ldots B_7$) or even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to ground through an internal MOS resistor when "Disabled."

Logic levels are negative true MOS logic.

Mode control should be "hard wired" to either V_{DD} (logical "1") or V_{SS} (logical "0").

The logic levels are in negative voltage logic notation.

National Semiconductor

MM4229/MM5229
3072-Bit (256 x 12) Open Drain ROM

general description

The MM4229/MM5229 is a 3072-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized in a 256 x 12 bit word configuration.

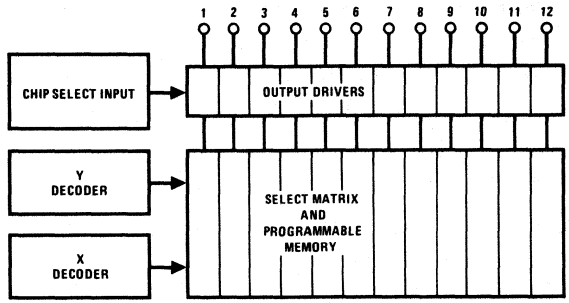
features

- TTL compatible
- Low standby power
- Programmable chip select inputs
- Typical 1.0μs access time
- Open drain outputs allow wire-OR of up to 8 devices

applications

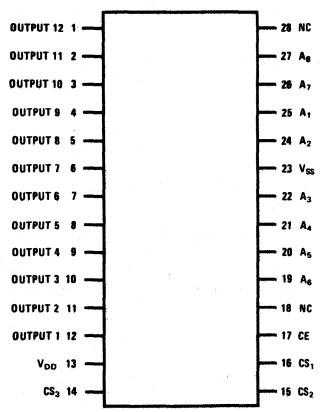
- Code conversion
- Random logic synthesis
- Table look-up
- Microprogramming

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Note: For programming information see Memory Applications Handbook, page 4-6.

Order Number MM4229D or MM5229D
See NS Package D28A

Order Number MM5229N
See NS Package N28A

absolute maximum ratings

All Inputs or Outputs with Respect to the Most Positive Voltage V_{SS} (Substrate)	+0.3V to −20V
Supply Voltage V_{DD} and V_D with Respect to V_{SS} (Substrate)	+3.0V to −20V
Operating Temperature Range	
MM4229	−55°C to +125°C
MM5229	−25°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

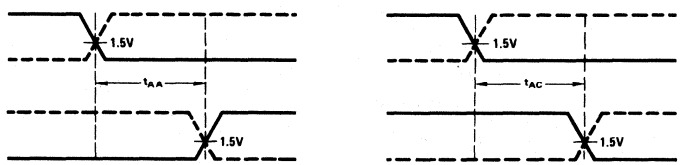
T_A within operating temperature range, V_{DD} = −12V ±10%, V_{SS} = +5V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})	V_{SS} = +4.75V	+2.4			V
Logical Low Level (V_{IL})	V_{SS} = +4.75V			+0.8	V
Data Output Levels					
Logical High Level (V_{OH})	6.8 kΩ ±5% to V_{DD} Plus One	+2.4			V
Logical Low Level (V_{OL})	Standard Series 54/74 Gate			+0.4	V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.6			mA
Data Input Leakage (I_{RI})	$V_{IN} - V_{SS}$ = −5V			2.0	μA
Data Output Leakage (I_{RO})	$V_{OUT} - V_{SS}$ = −5V (Note 1)			2.0	μA
Data Input Capacitance (C_{IN})	$V_{IN} - V_{SS}$ = 0V			5.0	pF
Data Output Capacitance (C_{OUT})	$V_{OUT} - V_{SS}$ = 0V			8.0	pF
Access Time (T_A)					
Address Response (t_{AA})	C_L = 20 pF		1.0	1.4	μs
C Inhibit Response (t_{AC})	C_L = 20 pF		0.8	1.2	μs
Active Power Supply					
V_{DD} Supply (I_{DD})	V_{SS} = +5V, V_1 = 0V		25	32	mA
V_{SS} Supply (I_{SS})	V_{DD} = 12V, T_A = 25°C		25	32	mA
Data Input Currents					
Logical High Level (I_{IH})	$V_{IN} - V_{SS}$ = −2.4V			2.0	μA
Logical Low Level (I_{IL})	$V_{IN} - V_{SS}$ = 5V			2.0	μA
Standby Power Supply					
I_{DD}	V_{SS} = +5V, V_1 = 0V		12	18	mA
I_{SS}	V_{DD} = −12V, T_A = 25°C		12	18	mA

Note 1: Chip inhibited or de-selected.

Note 2: The above logic levels are indicated in negative logic notation.

switching time waveforms



Definitions:

Access Time: Represents the total propagation delay through input translation decode for memory selection and output sense amplification of the memory signal and is measured from the last input transition through 1.5V to the last output transition through 1.5V.

Chip Enable: The output source and sink transistors are turned off in the chip inhibit and chip de-select mode to allow OR-tieing of output for easy memory expansion.

Chip Select: The outputs are enabled and data from the selected memory location will appear at the outputs. The chip select and chip enable inputs are programmable for decoderless word expansion.

National Semiconductor

MM4230/MM5230 2048-Bit (256 x 8 or 512 x 4) ROM

general description

The MM4230/MM5230 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

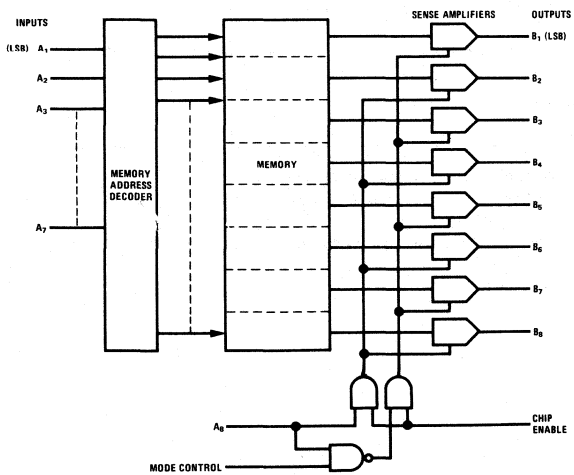
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

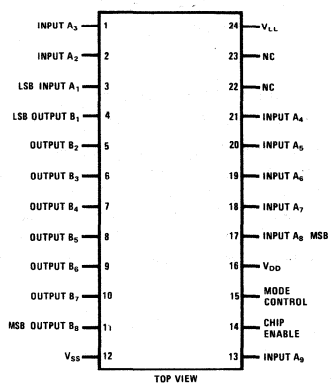
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

block and connection diagrams



Dual-In-Line Package



Order Number MM4230J or MM5230J
See NS Package J24A

Order Number MM5230N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

8

absolute maximum ratings

V_{GG} Supply Voltage		$V_{SS}-30V$
V_{DD} Supply Voltage		$V_{SS}-15V$
Input Voltage		$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature		$-65°C$ to $+150°C$
Operating Temperature	MM4230	$-55°C$ to $+125°C$
	MM5230	$0°C$ to $+70°C$
Lead Temperature (Soldering, 10 sec)		$300°C$

electrical characteristics

T_A within operating temperature range, V_{SS} = +12V ±5% and V_{GG} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			V_{SS} −9.0	V
Logical "0"		V_{SS} −1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} −8.0	V
Logical "0"		V_{SS} −2.0			V
Power Supply Current	$T_A = 25°C$				
V_{SS}			24	40	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}$ −12V			1	μA
Input Capacitance	f = 1.0 MHz V_{IN} = 0V		5		pF
Access Time (Notes 2, 3)	$T_A = 25°C$				
T_{ACCESS}	(See Timing Diagram) V_{SS} = +12V V_{GG} = −12V	150	500	725	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

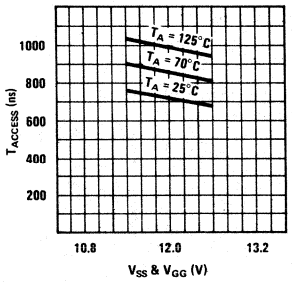
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

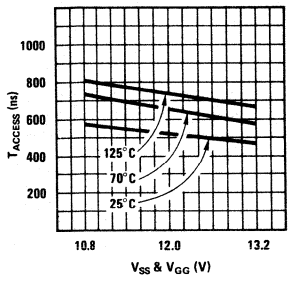
Note 4: The above logic levels are indicated in negative logic notation.

performance characteristics

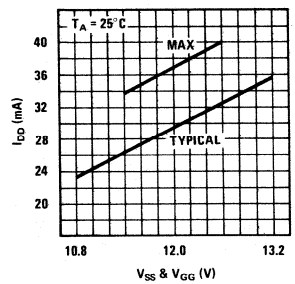
Guaranteed Access Time vs Supply Voltages



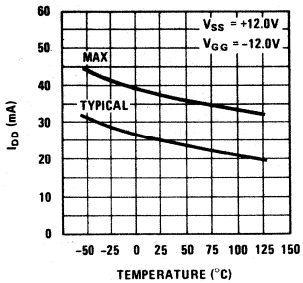
Typical Access Time vs Supply Voltages



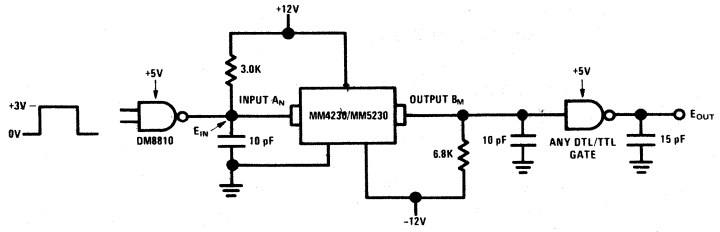
Power Supply Current vs Voltages

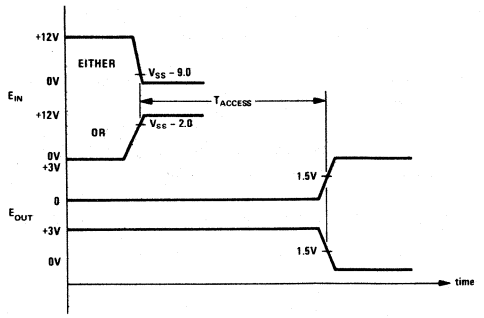


Power Supply Current vs Temperature



timing diagram/address time

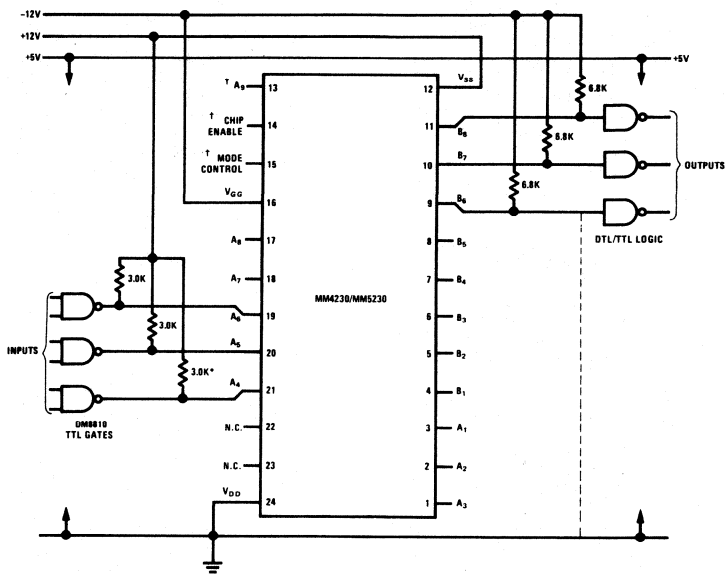




8

typical application

256 x 8 Bit ROM Showing TTL Interface



†See operating mode notes.
*R values can vary from 740Ω to 30 kΩ.

OPERATING MODES

128x8 ROM connection
Mode Control – Logic "0"
A_9 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

The logic levels are in negative voltage logic notation.

National Semiconductor

MM4231/MM5231 2048-Bit (256 x 8 or 512 x 4) ROM

general description

The MM4231/MM5231 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

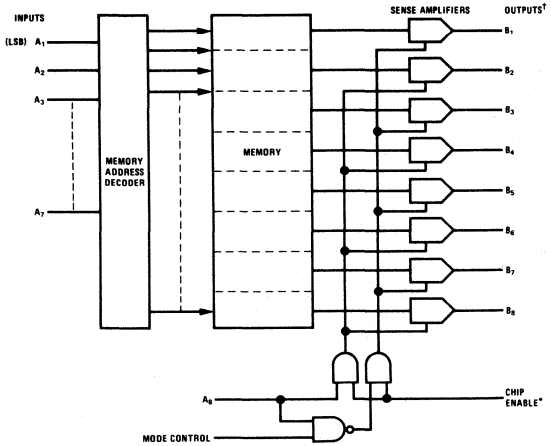
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 640 ns typ.
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control

applications

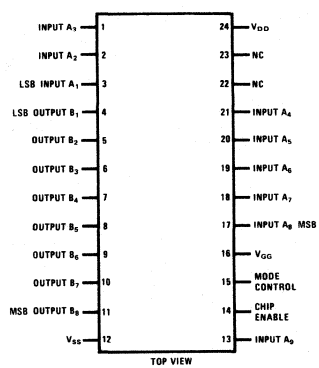
- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



† The outputs are open when Disabled.
* The output is enabled by applying a Logic "1" to the Chip Enable line.

Dual-In-Line Package



Order Number MM4231J or MM5231J
See NS Package J24A

Order Number MM5231N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

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absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{DD} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		–65°C to +150°C
Operating Temperature	MM4231	–55°C to +125°C
	MM5231	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{DD} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		15	30	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD}$ = –12V			1	μA
Input Leakage	V_{IN} = –12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		15		pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C V_{SS} = +5.0V $V_{GG} = V_{DD}$ = –12.0V		640	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{DD} Plus One Standard Series 54/74 Gate			8	

Note 1: These specifications apply for V_{SS} = +5V ±5%, $V_{GG} = V_{DD}$ = –12V, ±5%, and T_A = –55°C to +125°C (MM4231), T_A = –25°C to +70°C (MM5231) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

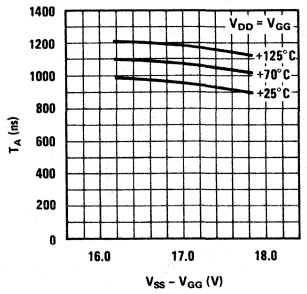
Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns.
Where N = Number of AND connections.

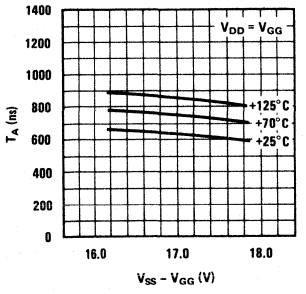
Note 5: Capacitances are measured on a lot sample basis only.

performance characteristics

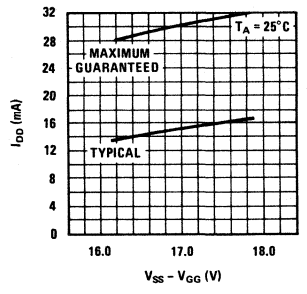
Guaranteed Access Time (T_A) vs Power Supply Voltage



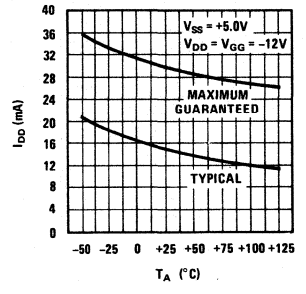
Typical Access Time (T_A) vs Power Supply Voltage



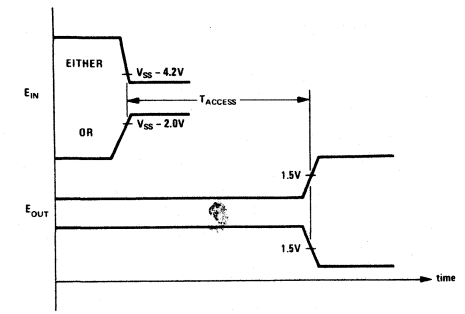
Power Supply Current vs Power Supply Voltage

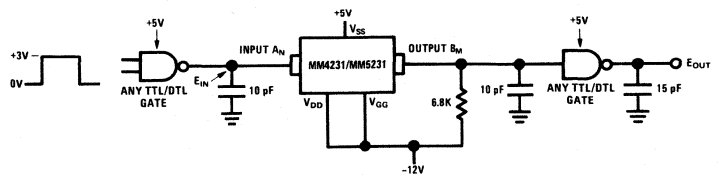


Power Supply Current vs Ambient Temperature



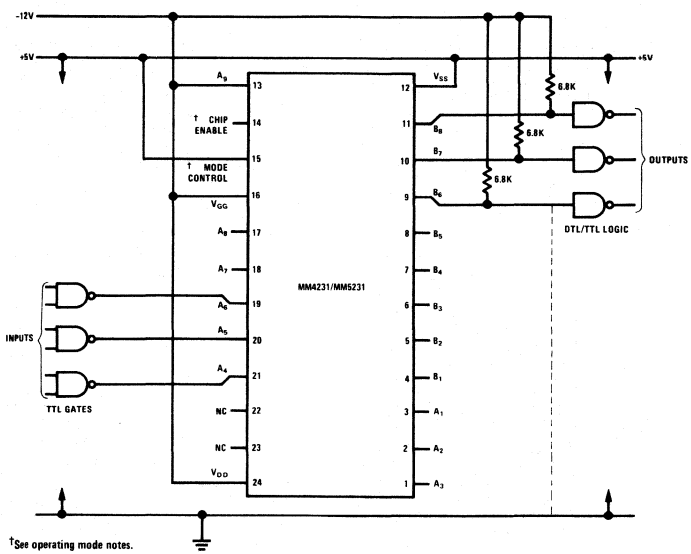
timing diagram/address time





typical application

256 x 8 Bit ROM Showing TTL Interface



Operating Modes

256 x 8 ROM connection (shown)
Mode Control – Logic "0"
A_9 – Logic "1"

512 x 4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "1" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

Logic levels are negative true MOS logic.

Mode Control should be "hard wired" to V_{DD} (Logical "1") or V_{SS} (Logical "0").

The logic levels are in negative voltage logic notation.

National Semiconductor

MM4232/MM5232 4096-Bit (512 × 8 or 1024 × 4) ROM

general description

The MM4232/MM5232 4096-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit or 1024 word x 4-bit memory organization that is controlled by the mode control input. Programmable Chip Enables (CE_1 and CE_2) provide logic control of up to 16K bits without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

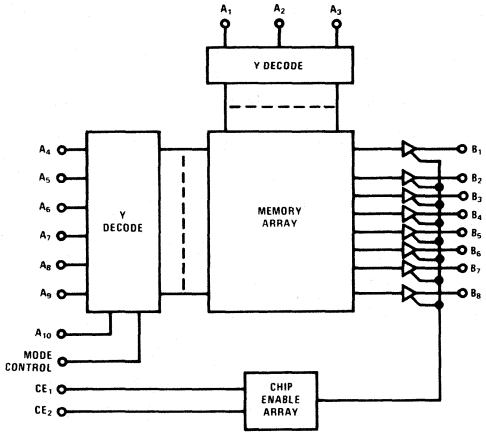
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two-programmable Chip Enable lines

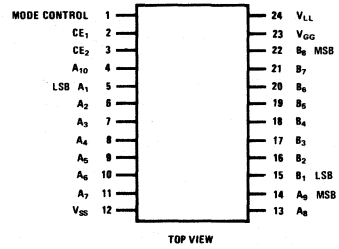
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

block and connection diagrams



Dual-In-Line Package



Order Number MM4232J or MM5232J
See NS Package J24A

Order Number MM5232N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{LL} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	MM4232	−55°C to +125°C
	MM5232	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics POSITIVE LOGIC

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{LL}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "0", V_{OL}	I_L = 1.6 mA Sink			.4	V
Logical "1", V_{OH}	I_L = 100 μA Source	2.4			V
Input Voltage Levels					
Logical "0", V_{IL}		V_{GG}		V_{SS} – 4.0	V
Logical "1", V_{IH}		V_{SS} – 2.0		V_{SS} + 0.3	V
Power Supply Current					
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −12, T_A = 25°C		23	37	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2)	T_A = 25°C, V_{SS} = 5	150		1000	ns
T_{ACCESS}	$V_{GG} = V_{LL}$ = −12V				
Output AND Connections (Note 3)				20	

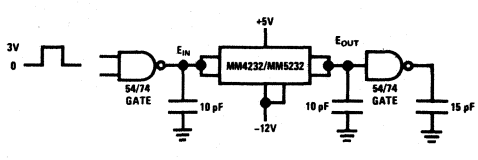
Note 1: Capacitances are measured periodically only.

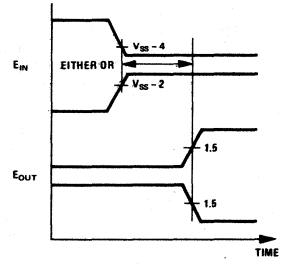
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

Note 3: The address time follows the following equation: T_{ACCESS} = the specified limit + (N − 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

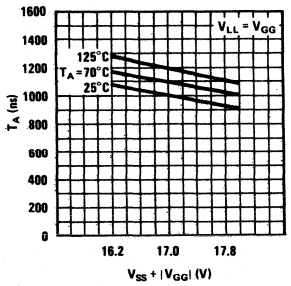
timing diagram/address time



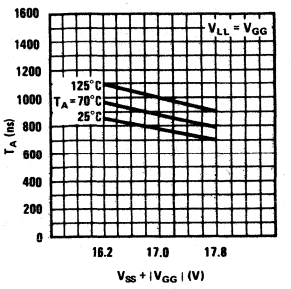


performance characteristics

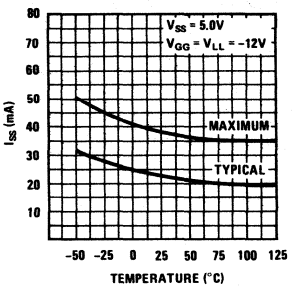
Guaranteed Access Time vs Supply Voltage



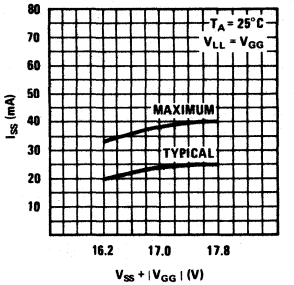
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature

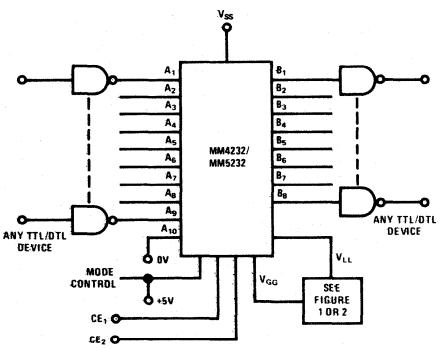


Power Supply Current vs Voltage



typical applications

TTL/MOS Interface



512 x 8 ROM connection
Mode Control = V_{IH}
$A_{10} = V_{IL}$

FIGURE 1. Power Saver for Small Memory Arrays

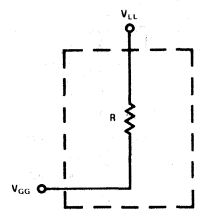
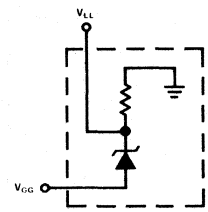


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME $|V_{LL}|_{MIN} = |-3V|$
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

Operating Modes

1024 x 4 ROM connection
Mode Control = V_{IL}
$A_{10} = V_{IL}$ enables the odd ($B_1 \ldots B_7$) outputs
V_{IH} enables the even ($B_2 \ldots B_8$) outputs

Note: Both chip enables may be programmed to provide any of four combinations. Example if $CE_1 = 1$ and $CE_2 = 1$ outputs (Positive Logic) would be enabled only when device pins 2 and 3 are Logic "1". The outputs will be in the third state when disabled.

National Semiconductor

MM4233/MM5233 4096-Bit (512 × 8) ROM

general description

The MM4233/MM5233 4096-bit static read only memory is a monolithic MOS integrated circuit utilizing P-channel ion-implanted enhancement mode low threshold technology to achieve bipolar compatibility. The ROM is organized in a 512 word x 8-bit format.

Four programmable chip selects provide logic control of the TRI-STATE® outputs, allowing wire OR capability of up to 16 ROM's without loading common data lines or reducing systems access times. A separate output supply lead V_{DD} is provided to reduce internal power dissipation in the output stages.

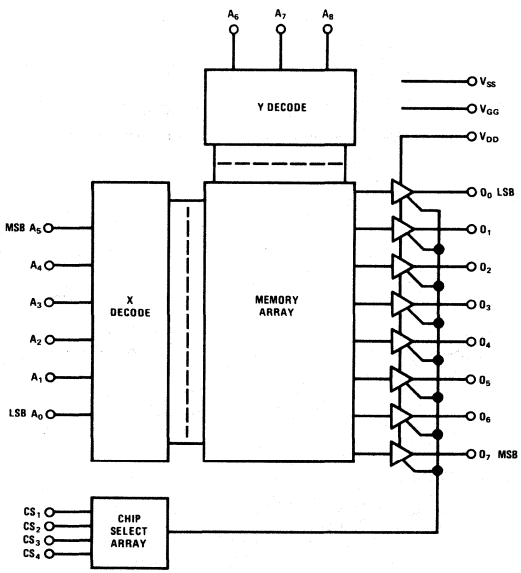
features

- Pin for pin compatible with the Fairchild 3514
- Bipolar compatible — No external components required
- Standard supplies — +5.0V, −12V
- TRI-STATE outputs — Bus ORable outputs
- Static operation — No clocks required
- Multiple ROM control — Four programmable chip select lines

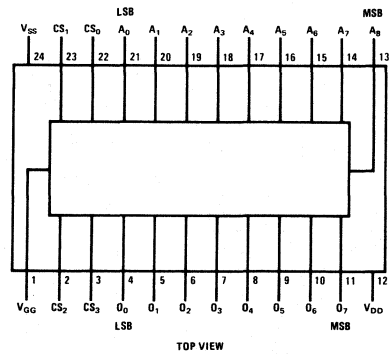
applications

- Code conversion
- Microprogramming
- Control logic
- Table look-up

block and connection diagrams



Dual-In-Line Package



Order Number MM4233J or MM5233J
See NS Package J24A

Order Number MM5233N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.5V to V_{SS} − 20 V
Power Dissipation at 25°C Ambient	0.8W
Operating Temperature	
MM4233	−55°C to +125°C
MM5233	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

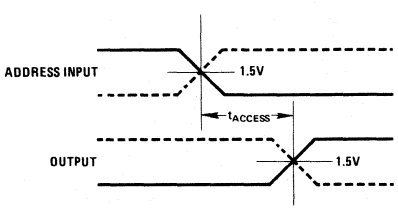
electrical characteristics

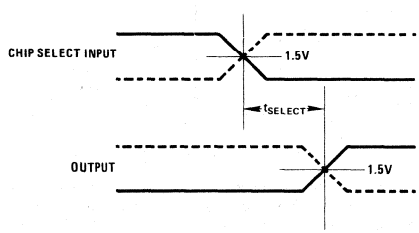
V_{SS} = +5.0V ±5%, V_{DD} = 0V, V_{GG} = −12V ±5%, T_A = −55°C to +125°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical Low	I_L = 2.4 mA Sink			0.4	V
Logical High	I_L = 0.5 mA Source	2.4			V
Input Voltage Levels					
Logical Low				V_{SS} − 4.0	V
Logical High		V_{SS} − 1.0			V
Power Supply Current	T_A = 25°C				
I_{SS}	(Note 1)		21	30	mA
I_{DD}				1.0	mA
I_{GG}			21	30	mA
Input Leakage	V_{IN} = V_{SS} −10V			1.0	μA
Input Capacitance (Note 2)	f = 1 MHz, V_{IN} = V_{SS}			5.0	pF
Output Capacitance (Note 2)	f = 1 MHz, V_{OUT} = V_{SS}			9.0	pF
Address Time	T_A = 25°C				
T_{ACCESS}	(Note 3 and Note 4)			1000	ns
Select Time	T_A = 25°C				
T_{SELECT}	(Note 3 and Note 4)			800	ns

Note 1: Outputs open.
Note 2: Capacitances are measured periodically only.
Note 3: See timing diagram.
Note 4: 1.5 TTL load, C_L = 20 pF.

switching time waveforms





National Semiconductor

MM4241/MM5241 3072-Bit (64 × 6 × 8) ROM

general description

The MM4241/MM5241 3072-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 6 word by 8-bit memory organization. Programmable Chip Enables (CE_1 and CE_2) provide logic control of multiple packages without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

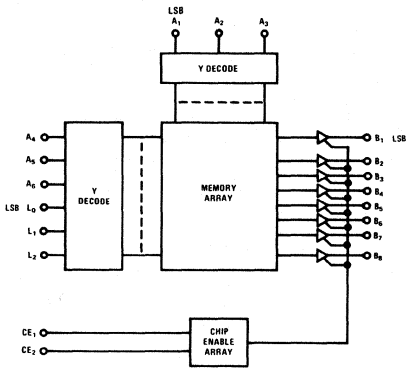
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two programmable Chip Enable lines

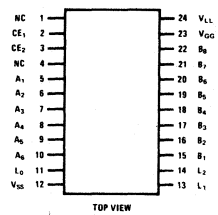
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4241J or MM5241J
See NS Package J24A

Order Number MM5241N
See NS Package N24B

typical applications

TTL/MOS Interface

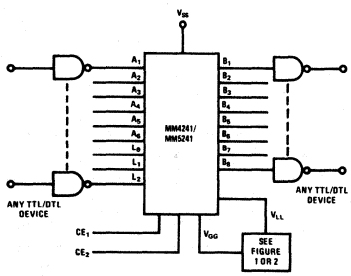


FIGURE 1. Power Saver for Small Memory Arrays

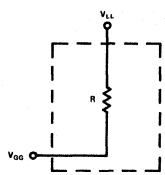
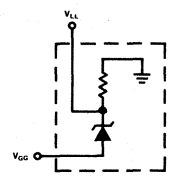


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME |VLL |MIN = |−3V |
VGG − VLL MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

Note: Both chip enables may be programmed to provide any of four combinations. Example: If CE_1 = 1 and CE_2 = 1 outputs (Negative Logic) would be enabled only when device pins 2 and 3 are negative (Logic "1"). The outputs will be in the third state when disabled. L_0, L_1 and L_2 (device pins 11, 13 and 14) are in positive logic (1 = most positive voltage levels = V_S − 2V; 0 = most negative voltage level = V_{SS} − 4V).

Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{LL} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	MM4241	−55°C to +125°C
	MM5241	−25°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics NEGATIVE LOGIC (Note 5)

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{LL}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "1"	I_L = 1.6 mA sink			.4	V
Logical "0"	I_L = 100 μA source	2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} – 4.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current					
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −12, T_A = 25°C		23	37	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2)	T_A = 25°C, V_{SS} = 5	150	700	900	ns
T_{ACCESS}	$V_{GG} = V_{LL}$ = −12V				
Output AND Connections (Note 3)				20	

Note 1: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 2: Capacitances are measured periodically only.

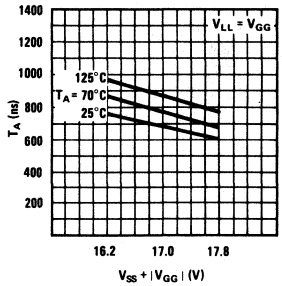
Note 3:. The address time follows the following equation: T_{ACCESS} = the specified limit + (N – 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

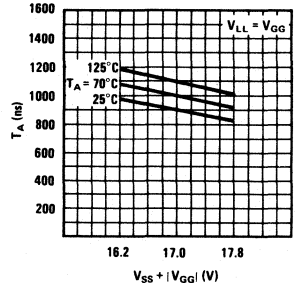
Note 5: All addresses and outputs are in negative true logic with the exception of L_0, L_1, and L_2 which are in positive logic.

performance characteristics

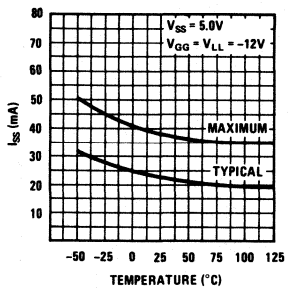
Typical Access Time vs Supply Voltage



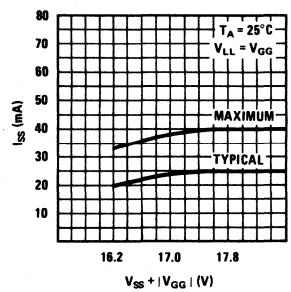
Guaranteed Access Time vs Supply Voltage



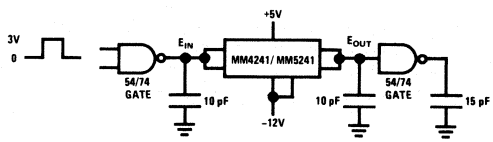
Power Supply Current vs Temperature

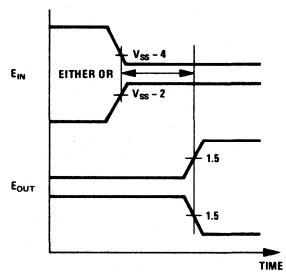


Power Supply Current vs Voltage



timing diagram/address time





National Semiconductor

MM4243/MM5243 2048-Bit (256 x 8 or 512 x 4) ROM

general description

The MM4243/MM5243 is a 2048-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 256 8-bit words or 512 4-bit words. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. Although a PROM die is used, factory programming is required. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

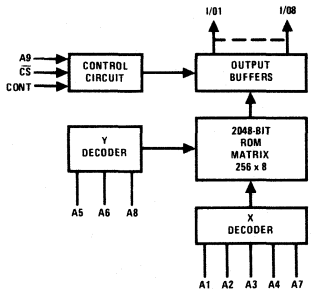
features

- Electrically programmed for fast turn-around
- Bipolar compatibility — +5V, −12V operation
- High speed operation — 1μs max access time
- Pin compatible with MM5203Q, EPROM and the MM5213 masked ROM
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- Chip select output control
- 256 x 8 or 512 x 4 organization

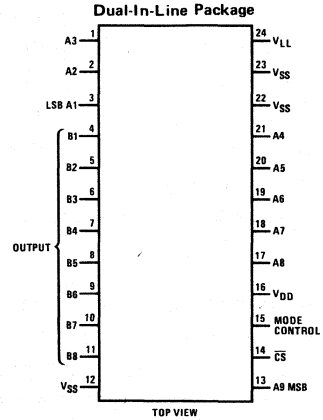
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

block and connection diagrams



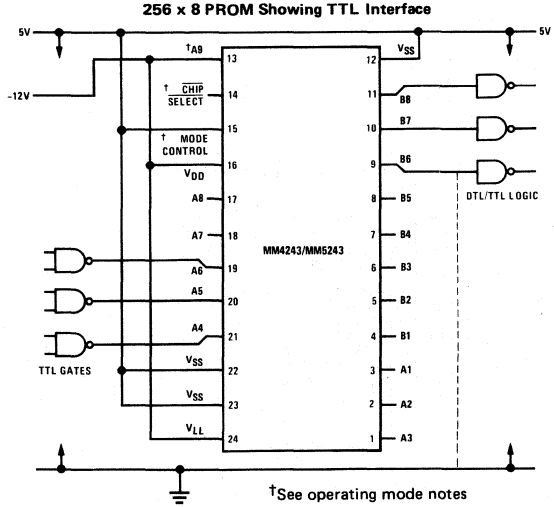
Dual-In-Line Package



Order Number MM4243J or MM5243J
See NS Package J24A

typical application

256 x 8 PROM Showing TTL Interface



†See operating mode notes

Operating Modes

256 x 8 ROM connection (shown)
Mode Control — HIGH (V_{SS})
A9 — LOW

512 x 4 ROM connections
Mode Control — LOW (GND or V_{DD})
A9 — Logic HIGH enables the odd (B1, B3. . .B7) outputs
A9 — Logic LOW enables the even (B2, B4. . .B8) outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

Note: For programming information see Memory Applications Handbook, page 4-6.

absolute maximum ratings

All Input or Output Voltages with Respect to V_{SS}	0.3V to −20V
Power Dissipation	1W
Operating Temperature Range	
MM4243	−55°C to +85°C
MM5243	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

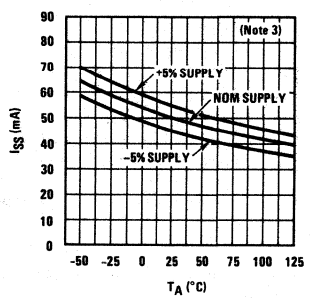
T_A within operating temperature range, V_{SS} = 5V ±5%, $V_{DD} = V_{LL}$ = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0V			1	μA
I_{LO}	Output Leakage	V_{OUT} = 0V, $\overline{CS} = V_{SS} - 2$			1	μA
I_{SS}	Power Supply Current	$\overline{CS} = V_{SS} - 2$, T_A = 25°C		35	55	mA
V_{IL}	Input LOW Voltage		V_{SS}−10		V_{SS}−4	V
V_{IH}	Input HIGH Voltage		V_{SS}−2		V_{SS}+0.3	V
V_{OL}	Output LOW Voltage	1.6 mA sink, $-12.6V < V_{LL} < -3V$			0.4	V
I_{CF}	Output Clamp Current	V_{OUT} = −1V, T_A = 0°C, (Note 4)				
		V_{LL} = −3V		3.5	6	mA
		V_{LL} = −12.6V		8	15	mA
V_{OH}	Output HIGH Voltage	0.8 mA source	2.4			V
T_{OH}	Data Hold Time	(Min Access Time), *(Figures 1 and 2)*			100	ns
T_{ACC}	Access Time	T_A = 25°C, (Note 2), *(Figures 1 and 2)*		0.7	1	μs
T_{CO}	Chip Select Time	*(Figures 1 and 3)*			500	ns
T_{OD}	Chip Deselect Time	*(Figures 1 and 3)*			500	ns
t_{CS}	Allowable Chip Select Delay	*(Figures 1 and 2)* Allowable delay in selecting chip after change of address without affecting access time			100	ns
C_{IN}	Input Capacitance	$V_{IN} = V_{SS}$, f = 1 MHz, (Note 1)		8	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = V_{SS}$, $\overline{CS} = V_{SS} - 2$, f = 1 MHz, (Note 1)		8	15	pF

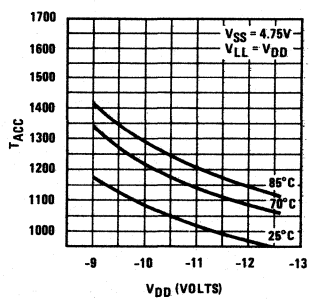
Note 1: Capacitances are not tested on a production basis but are periodically sampled.
Note 2: T_{ACC} = 1000 ns + 25(N−1) where N is the number of chips wired-OR together.
Note 3: Measured under continuous operation.
Note 4: I_{CF} flows out the V_{LL} pin, it does not flow out the V_{DD} pin.

typical performance characteristics

Maximum Supply Current I_{SS} as a Function of Temperature



Maximum Access Time (T_{ACC}) as a Function of V_{DD} Supply Voltage



access time diagrams

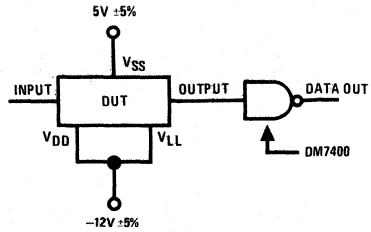


FIGURE 1. AC Test Circuit

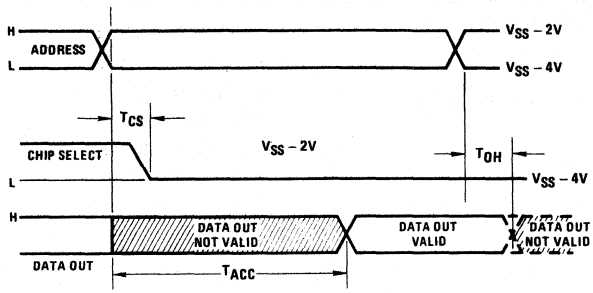


FIGURE 2. Access Time From Address

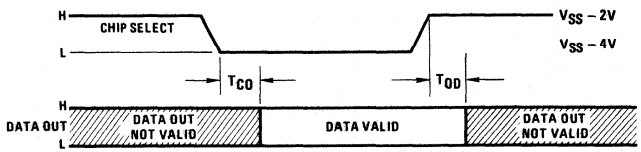


FIGURE 3. Access Time From Chip Select

National Semiconductor

MM4244/MM5244 4096-Bit (512 × 8) ROM

general description

The MM4244/MM5244 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. Although a PROM die is used, factory programming is required. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

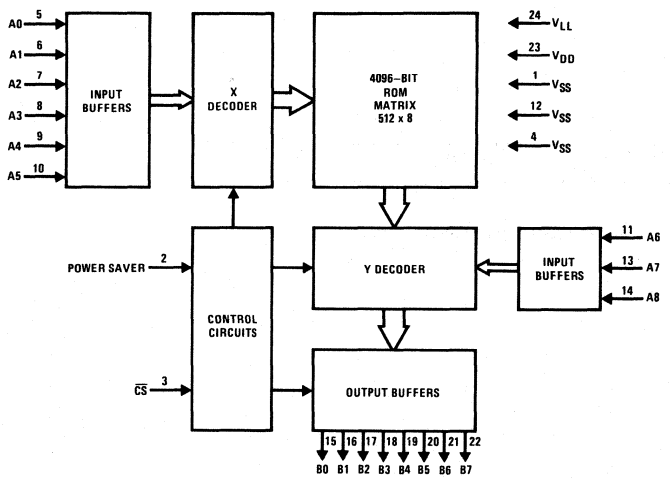
features

- Electrically programmed for fast turn-around
- Fast access time
  - MM4244 1.25μs
  - MM5244 1μs
- DTL/TTL compatibility
- Pin compatible with the MM5204 and the MM5214
- Standard power supplies 5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- Low power dissipation
- "Power Saver" control for low power applications

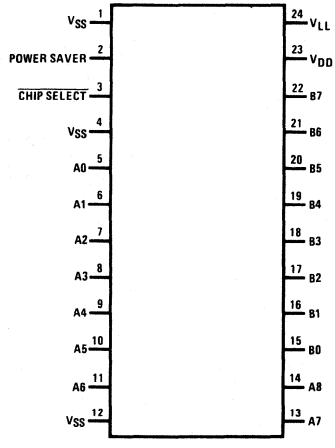
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4244J or MM5244J
See NS Package J24A

absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to V_{SS}	0.3V to −20V	Operating Temperature Range MM5244	0°C to +70°C
Power Dissipation	750 mW	MM4244	−55°C to +85°C
Lead Temperature (Soldering, 10 seconds)	300°C	Storage Temperature Range	−65°C to +125°C

dc electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, MM4244: V_{SS} = 5V ±10%, V_{DD} = −12V ±10%, MM5244: V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP (Note 5)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{DD}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1	μA
I_{DD}	Power Supply Current	T_A = 0°C, $\overline{CS}$ = V_{IH}				
	MM5244	Power Saver = V_{IL}		28	40	mA
	MM4244	Power Saver = V_{IL}			50	mA
	MM5244	Power Saver = V_{IH}		6	8	mA
	MM4244	Power Saver = V_{IH}			10	mA
I_{SS}	MM5244	Power Saver = V_{IL}			42	mA
	MM4244	Power Saver = V_{IL}			52	mA
	MM5244	Power Saver = V_{IH}			10	mA
	MM4244	Power Saver = V_{IH}			12	mA

ac electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, MM4244: V_{SS} = 5V ±10%, V_{DD} = −12V ±10%, MM5244: V_{SS} = 5V ±5V, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP (Note 5)	MAX	UNITS
t_{ACC}	Access Time	*(Figure 1)*, (Note 4)				
	MM5244	T_A = 70°C		0.75	1	μs
	MM4244	T_A = 85°C			1.25	μs
t_{PO}	Power Saver Set-Up Time	*(Figure 1)*				
	MM5244				1.8	μs
	MM4244				2	μs
t_{CO}	Chip Select Delay	*(Figure 1)*				
	MM5244				500	ns
	MM4244				600	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time	*(Figure 1)*				
	MM5244		30	300	500	ns
	MM4244		30	300	600	ns
t_{ODP}	Power Saver Deselect Time	*(Figure 1)*				
	MM5244		30	300	500	ns
	MM4244		30	300	600	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1 MHz, (Note 2)		5	8	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, CS = V_{IH}, f = 1 MHz, (Note 2)		8	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

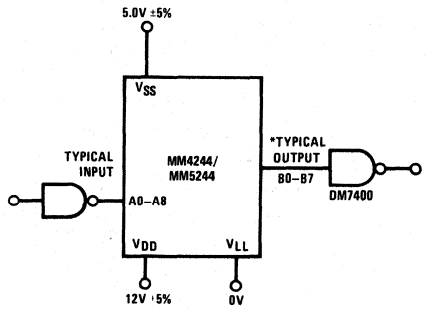
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 1000 ns + 25 (N-1) where N is the number of devices wire−OR'd together.

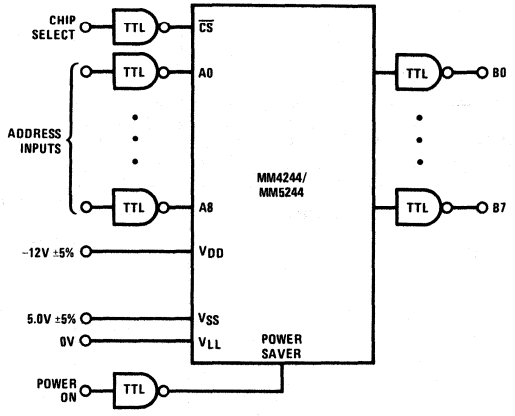
Note 5. Typical values are for nominal voltages and T_A = 25°C,unless otherwise specified.

ac test circuit

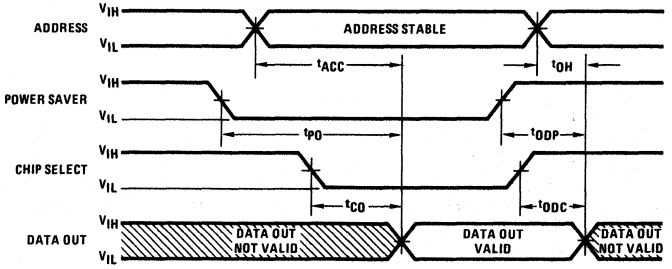


*t_{ACC}, t_{OH}, t_{CO} and t_{OD} measured at output of MM4244/MM5244

typical application



switching time waveforms

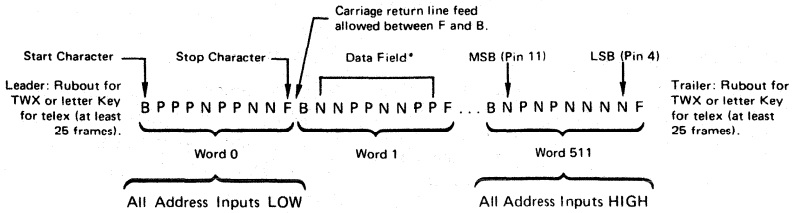


Note: All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns.

FIGURE 1. Read Operation

preferred format MM4243/MM5243, MM4244/MM5244

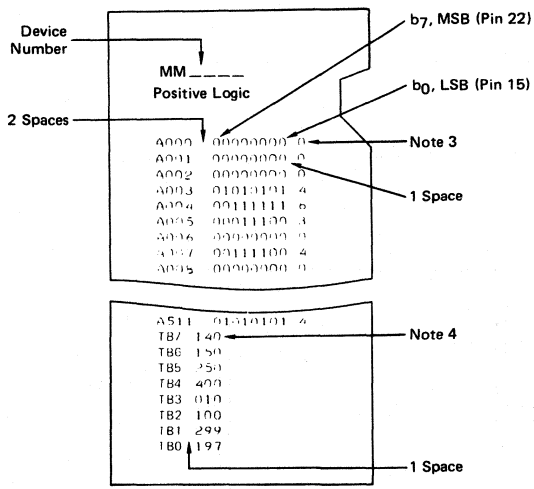
The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape, the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 256 or 512 words must be entered beginning with word 0.

alternate format MM4243/MM5243, MM4244/MM5244

[Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

National Semiconductor

MM52116, INS8316(MM2316E) 16,384-Bit (2048 × 8) ROM

General Description

The INS8316 is a static MOS 16,384-bit read-only memory organized in an 2048-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

Three programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

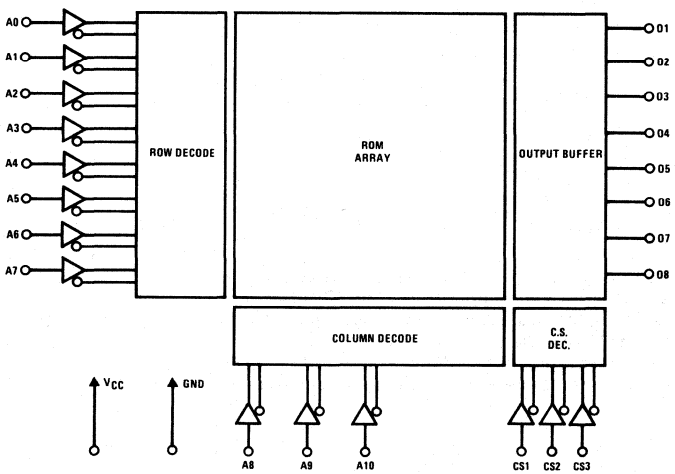
Features

- Fully decoded
- Single 5V power supply ±10% tolerance
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048-word-by-8-bit organization
- Maximum access time — 450 ns
- Industry standard pin outs (MM2316E)

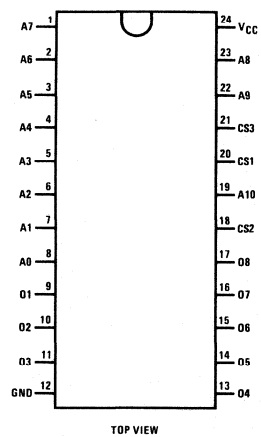
Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number INS8316D
See NS Package D24C

Order Number INS8316N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 2)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−20	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		70	100	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{AC}	Chip Select Access Time	See AC Test Circuit. All Times (Except t_{OFF})			120	ns
t_{OFF}	Output Turn OFF Delay	Measured to 1.5V Level with t_r and t_f of			100	ns
t_A	Address Access Time	Input < 20 ns, *(Figures 1 and 2)*, t_{OFF} TRI-STATE Output Level Measured to Less than ±20 μA Output Current			450	ns

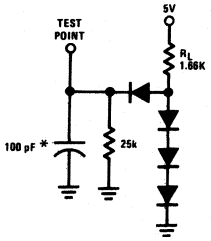
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



*Includes jig capacitance

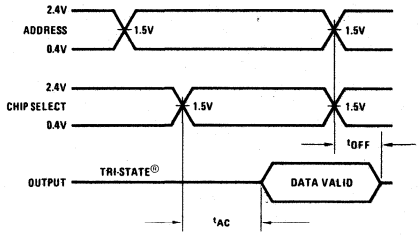


FIGURE 1. Address Preceeds Chip Select

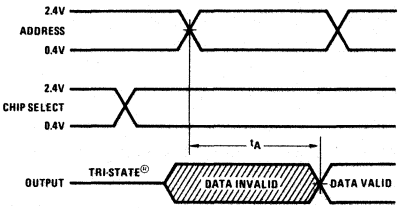


FIGURE 2. Address Follows Chip Select

Custom ROM Programming

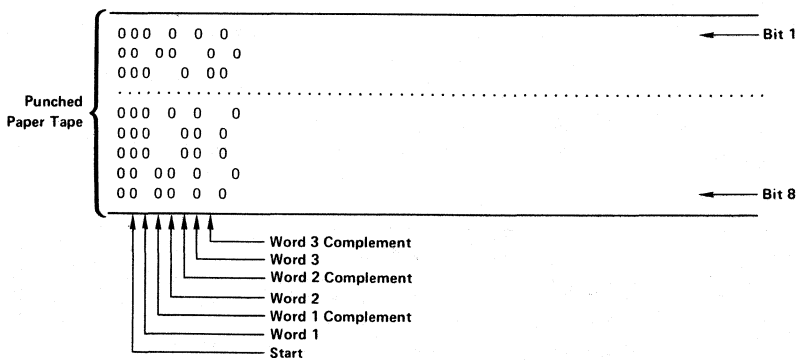
INFORMATION NEEDED

So that National can better serve its customers, the following information *must* be submitted with each ROM order.

National Semiconductor Corporation 2900 Semiconductor Dr., Santa Clara, CA. 95051 Phone (408) 737-5000 TWX 910-339-9240			NATIONAL PART NUMBER
			ROM LETTER CODE (NATIONAL USE ONLY)
NAME			DATE
ADDRESS			CUSTOMER PRINT OR ID NO.
CITY		STATE ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE	DATE
CHIP SELECT INFORMATION		LOGIC ☐ POS ☐ NEG	
CS1	CS2	CS3	

Tape Entry Format

A. Binary Complement Format



POSITIVE Logic: A punch is a "1" or most positive voltage. Omission of a punch is a "0" or the more negative voltage.

Pre-Programmed PROM

B. Hex Format (Intel Standard Hex)

- 2708
- 2716
- Or combinations of the above to make 16k, 32k or 64k bits.

National Semiconductor

MM52132, INS8332 32,768-Bit (4096 × 8) MAXI-ROM™

General Description

The INS8332 is a static MOS 32,768-bit read-only memory organized in a 4096-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

Two programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

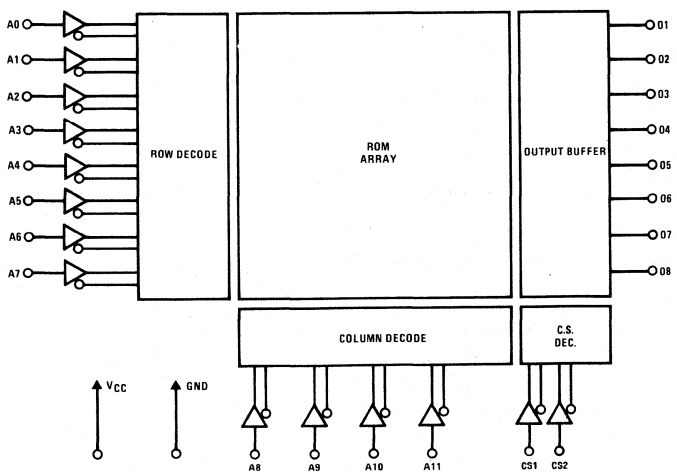
Features

- Fully decoded
- Single 5V power supply ±10% tolerance
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 4096-word-by-8-bit organization
- Maximum access time — 450 ns
- Industry standard pin outs

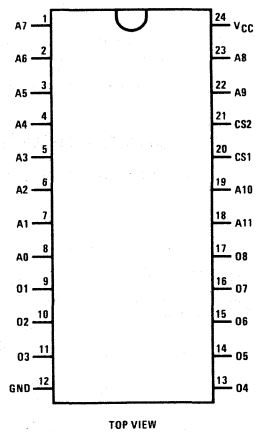
Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number INS8332D
See NS Package D24C

Order Number INS8332N
See NS Package N24B

8

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 2)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−20	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		100	130	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{AC}	Chip Select Access Time	See AC Test Circuit. All Times (Except t_{OFF})			120	ns
t_{OFF}	Output Turn OFF Delay	Measured to 1.5V Level with t_r and t_f of			100	ns
t_A	Address Access Time	Input < 20 ns, *(Figures 1 and 2)*, t_{OFF} TRI-STATE Output Level Measured to Less than ±20 μA Output Current			450	ns

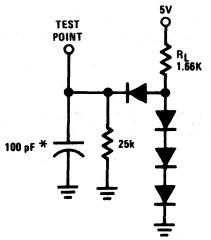
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



*Includes jig capacitance

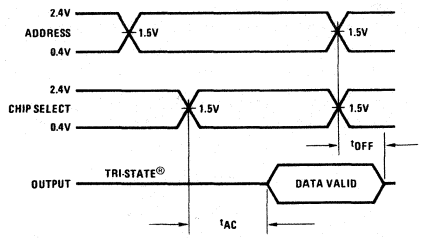


FIGURE 1. Address Preceeds Chip Select

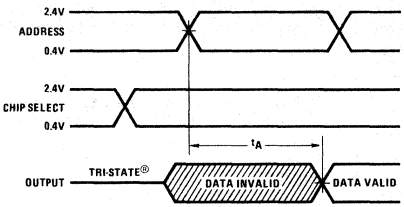


FIGURE 2. Address Follows Chip Select

Custom ROM Programming

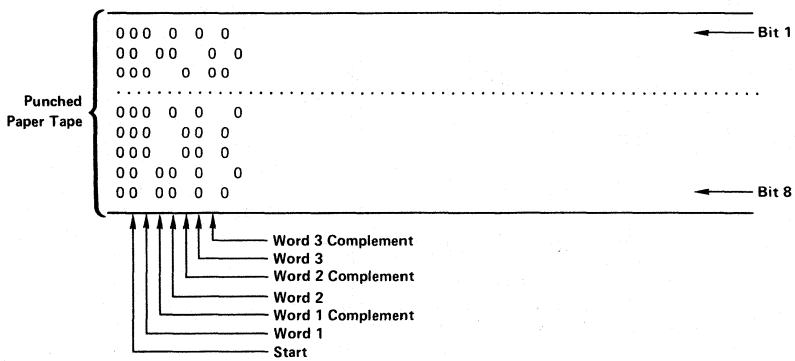
INFORMATION NEEDED

So that National can better serve its customers, the following information *must* be submitted with each ROM order.

National Semiconductor Corporation 2900 Semiconductor Dr., Santa Clara, CA. 95051 Phone (408) 737-5000 TWX 910-339-9240			NATIONAL PART NUMBER ROM LETTER CODE (NATIONAL USE ONLY)
NAME			DATE
ADDRESS			CUSTOMER PRINT OR ID NO.
CITY		STATE ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE	DATE
CHIP SELECT INFORMATION		LOGIC ☐ POS ☐ NEG	
CS1	CS2		CS3

Tape Entry Format

A. Binary Complement Format



POSITIVE Logic: A punch is a "1" or most positive voltage. Omission of a punch is a "0" or the more negative voltage.

Pre-Programmed PROM

B. Hex Format (Intel Standard Hex)

- 2708
- 2716
- Or combinations of the above to make 16k, 32k or 64k bits.

National Semiconductor

MM52164, INS8364 65,536-Bit (8192 × 8) MAXI-ROM™

General Description

The INS8364 is a static MOS 65,536-bit read-only memory organized in an 8192-word by 8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

One programmable chip select controlling the TRI-STATE® outputs allow for memory expansions.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

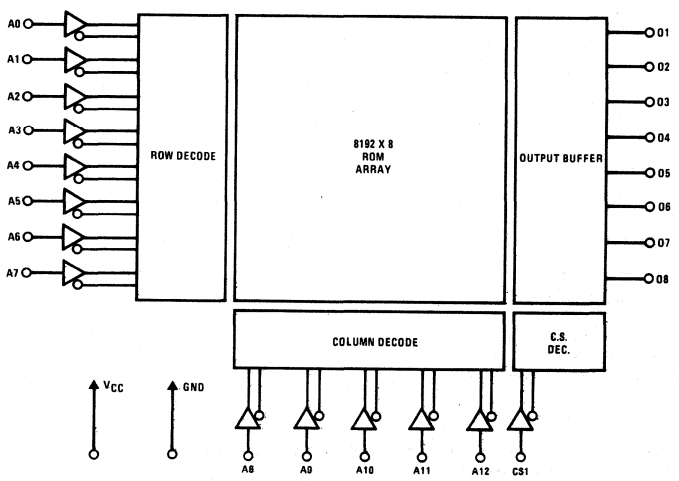
Features

- Fully decoded
- Single 5V power supply ±10% tolerance
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip select
- 8192-word-by-8-bit organization
- Maximum access time — 450 ns
- Industry standard pin outs

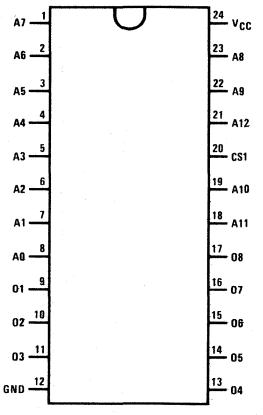
Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number INS8364D
See NS Package D24C

Order Number INS8364N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 2)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2.2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.6	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−20	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		100	130	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
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AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{AC}	Chip Select Access Time	See AC Test Circuit. All Times (Except t_{OFF})			120	ns
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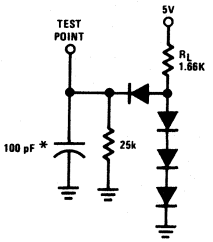
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



*Includes jig capacitance

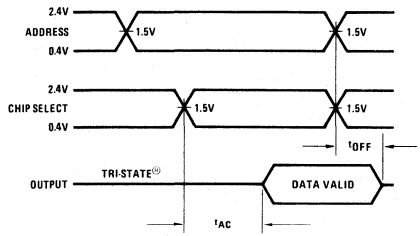


FIGURE 1. Address Preceeds Chip Select

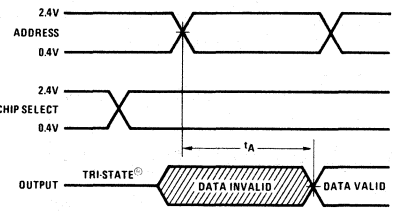


FIGURE 2. Address Follows Chip Select

Custom ROM Programming

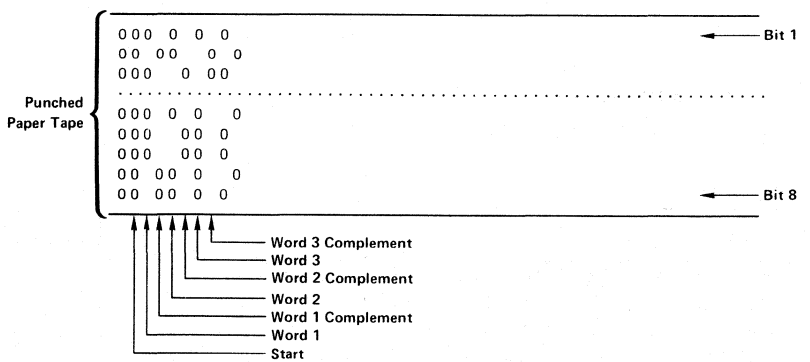
INFORMATION NEEDED

So that National can better serve its customers, the following information *must* be submitted with each ROM order.

National Semiconductor Corporation 2900 Semiconductor Dr., Santa Clara, CA. 95051 Phone (408) 737-5000 TWX 910-339-9240			NATIONAL PART NUMBER ROM LETTER CODE (NATIONAL USE ONLY)
NAME			DATE
ADDRESS			CUSTOMER PRINT OR ID NO.
CITY		STATE ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE	DATE
CHIP SELECT INFORMATION		LOGIC ☐ POS ☐ NEG	
CS1	CS2	CS3	

Tape Entry Format

A. Binary Complement Format



POSITIVE Logic: A punch is a "1" or most positive voltage. Omission of a punch is a "0" or the more negative voltage.

Pre-Programmed PROM

B. Hex Format (Intel Standard Hex)

- 2708
- 2716
- Or combinations of the above to make 16k, 32k or 64k bits.

Section 9

Character Generators

9

The Character Generators included in this section represent very cost effective solutions to problems arising in the design and implementation of CRT display subsystems. National's innovations in these devices in conjunction with the DP8350 series of CRT Controllers have assisted in the growth of this very important marketplace. Contact your local National representative for costs and other assistance.

National Semiconductor

Character Generators

MM4220DF/MM5220DF "Quick Brown Fox" Generator

general description

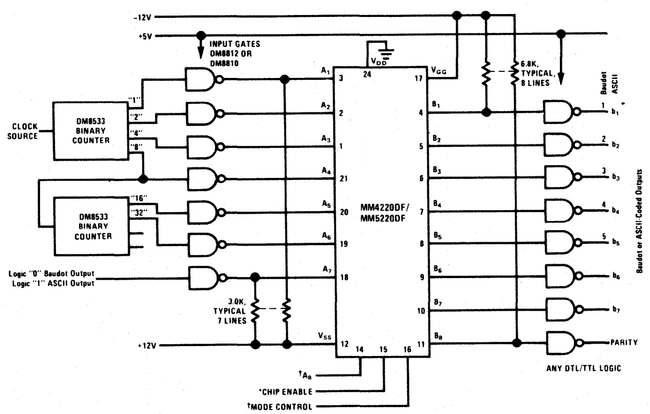
The MM4220DF/MM5220DF is designed for exercising and rapid testing of ASCII and Baudot-coded keyboards, typing mechanisms, and data communications links by generating the internationally accepted "Quick Brown Fox" message.

The input is a 7-bit binary sequential count. The output of a 6 stage up-counter can be used; a seventh bit selects the desired code. The message is generated in the 5-bit Baudot Communications Set code with a binary count input of 0 to 63. The message is generated in the 7-bit American Standard Code for Information Interchange (ASCII) along with an even parity bit for a binary count input of 64 to 127.

device characteristics

The message generator is fully contained on a monolithic MOS integrated circuit chip utilizing low threshold voltage technology for increased DTL/TTL compatibility. For complete electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical applications



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

Outputs for circuit shown
Baudot: Logic "0" = "punch"
ASCII: Logic inversion

A typical application showing the ASCII-coded test message as received at a computer terminal.

```
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
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THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
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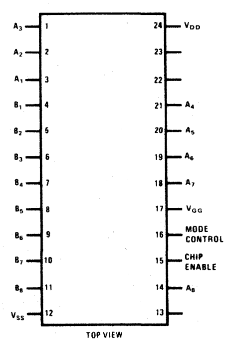
connection diagram

Dual-In-Line Package



Order Number MM4220DF/J or MM5220DF/J
See NS Package J24A

Order Number MM5220DF/N
See NS Package N24B

code conversion table

ADDRESS	OUTPUT CHARACTER	OUTPUT CODE (Baudot) –	–	–	5	4	3	2	1	ADDRESS	OUTPUT CHARACTER	OUTPUT CODE (ASCII) PARITY	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	CR	1	1	1	1	0	1	1	1	64	NULL	0	0	0	0	0	0	0	0
1	CR	1	1	1	1	0	1	1	1	65	CR	0	1	1	1	0	0	1	0
2	LF	1	1	1	1	1	1	0	1	66	CR	0	1	1	1	0	0	1	0
3	Ltr.	1	1	1	0	0	0	0	0	67	LF	1	1	1	1	0	1	0	1
4	T	1	1	1	0	1	1	1	1	68	T	0	0	1	0	1	0	1	1
5	H	1	1	1	0	1	0	1	1	69	H	1	0	1	1	0	1	1	1
6	E	1	1	1	1	1	1	1	0	70	E	0	0	1	1	1	0	1	0
7	SP	1	1	1	1	1	0	1	1	71	SP	0	1	0	1	1	1	1	1
8	Q	1	1	1	0	1	0	0	0	72	Q	0	0	1	0	1	1	1	0
9	U	1	1	1	1	1	0	0	0	73	U	1	0	1	0	1	0	1	0
10	I	1	1	1	1	1	0	0	1	74	I	0	0	1	1	0	1	1	0
11	C	1	1	1	1	0	0	0	1	75	C	0	0	1	1	1	1	0	0
12	K	1	1	1	1	0	0	0	0	76	K	1	0	1	1	0	1	0	0
13	SP	1	1	1	1	1	0	1	1	77	SP	0	1	0	1	1	1	1	1
14	B	1	1	1	0	0	1	1	0	78	B	1	0	1	1	1	1	0	1
15	R	1	1	1	1	0	1	0	1	79	R	0	0	1	0	1	1	0	1
16	O	1	1	1	0	0	1	1	1	80	O	0	0	1	1	0	0	0	0
17	W	1	1	1	0	1	1	0	0	81	W	0	0	1	0	1	0	0	0
18	N	1	1	1	1	0	0	1	1	82	N	1	0	1	1	0	0	0	1
19	SP	1	1	1	1	1	0	1	1	83	SP	0	1	0	1	1	1	1	1
20	F	1	1	1	1	0	0	1	0	84	F	0	0	1	1	1	0	0	1
21	O	1	1	1	0	0	1	1	1	85	O	0	0	1	1	0	0	0	0
22	X	1	1	1	0	0	0	1	0	86	X	0	0	1	0	0	1	1	1
23	SP	1	1	1	1	1	0	1	1	87	SP	0	1	0	1	1	1	1	1
24	J	1	1	1	1	0	1	0	0	88	J	0	0	1	1	0	1	0	1
25	U	1	1	1	1	1	0	0	0	89	U	1	0	1	0	1	0	1	0
26	M	1	1	1	0	0	0	1	1	90	M	1	0	1	1	0	0	1	0
27	P	1	1	1	0	1	0	0	1	91	P	1	0	1	0	1	1	1	1
28	S	1	1	1	1	1	0	1	0	92	S	1	0	1	0	1	1	0	0
29	SP	1	1	1	1	1	0	1	1	93	SP	0	1	0	1	1	1	1	1
30	O	1	1	1	0	0	1	1	1	94	O	0	0	1	1	0	0	0	0
31	V	1	1	1	0	0	0	0	1	95	V	1	0	1	0	1	0	0	1
32	E	1	1	1	1	1	1	1	0	96	E	0	0	1	1	1	0	1	0
33	R	1	1	1	1	0	1	0	1	97	R	0	0	1	0	1	1	0	1
34	SP	1	1	1	1	1	0	1	1	98	SP	0	1	0	1	1	1	1	1
35	T	1	1	1	0	1	1	1	1	99	T	0	0	1	0	1	0	1	1
36	H	1	1	1	0	1	0	1	1	100	H	1	0	1	1	0	1	1	1
37	E	1	1	1	1	1	1	1	0	101	E	0	0	1	1	1	0	1	0
38	SP	1	1	1	1	1	0	1	1	102	SP	0	1	0	1	1	1	1	1
39	L	1	1	1	0	1	1	0	1	103	L	0	0	1	1	0	0	1	1
40	A	1	1	1	1	1	1	0	0	104	A	1	0	1	1	1	1	1	0
41	Z	1	1	1	0	1	1	1	0	105	Z	1	0	1	0	0	1	0	1
42	Y	1	1	1	0	1	0	1	0	106	Y	1	0	1	0	0	1	1	0
43	SP	1	1	1	1	1	0	1	1	107	SP	0	1	0	1	1	1	1	1
44	D	1	1	1	1	0	1	1	0	108	D	1	0	1	1	1	0	1	1
45	O	1	1	1	0	0	1	1	1	109	O	0	0	1	1	0	0	0	0
46	G	1	1	1	0	0	1	0	1	110	G	1	0	1	1	1	0	0	0
47	SP	1	1	1	1	1	0	1	1	111	SP	0	1	0	1	1	1	1	1
48	Fig.	1	1	1	0	0	1	0	0	112	1	0	1	0	0	1	1	1	0
49	1	1	1	1	0	1	0	0	0	113	2	0	1	0	0	1	1	0	1
50	2	1	1	1	0	1	1	0	0	114	3	1	1	0	0	1	1	0	0
51	3	1	1	1	1	1	1	1	0	115	4	0	1	0	0	1	0	1	1
52	4	1	1	1	1	0	1	0	1	116	5	1	1	0	0	1	0	1	0
53	5	1	1	1	0	1	1	1	1	117	6	1	1	0	0	1	0	0	1
54	6	1	1	1	0	1	0	1	0	118	7	0	1	0	0	1	0	0	0
55	7	1	1	1	1	1	0	0	0	119	8	0	1	0	0	0	1	1	1
56	8	1	1	1	1	1	0	0	1	120	9	1	1	0	0	0	1	1	0
57	9	1	1	1	0	0	1	1	1	121	0	1	1	0	0	1	1	1	1
58	0	1	1	1	0	1	0	0	1	122	SP	0	1	0	1	1	1	1	1
59	SP	1	1	1	1	1	0	1	1	123	D	1	0	1	1	1	0	1	1
60	Ltr.	1	1	1	0	0	0	0	0	124	E	0	0	1	1	1	0	1	0
61	D	1	1	1	1	0	1	1	0	125	SP	0	1	0	1	1	1	1	1
62	E	1	1	1	1	1	1	1	0	126	DEL	0	0	0	0	0	0	0	0
63	SP	1	1	1	1	1	0	1	1	127	DEL	0	0	0	0	0	0	0	0
		B8	B7	B6	B5	B4	B3	B2	B1			B8	B7	B6	B5	B4	B3	B2	B1
		Baudot: Logic "0" = "punch"										ASCII: Logic inversion							

SP = Space

Note: When chip enable input is at a logical 0, all outputs are at a logical 1.

National Semiconductor

MM4240/MM5240
2560-Bit Static Chararacter Generator

general description

The MM4240/MM5240 2560-bit static character generator is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology. Six character address and three row address input lines provide access to 64-8 x 5 characters. Customer-generated single or multiple package character fonts are easily programmed by completing a pattern selection form. A standard 7 x 5 raster scan font is available by ordering the MM4240AA/MM5240AA.

The MM4240/MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

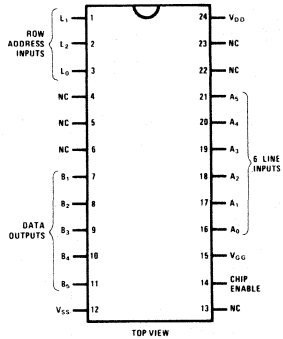
features

- Bipolar compatibility
- High speed operation—500 ns max
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

applications

- Character generation
- Random logic synthesis
- Micro-programming
- Table look-up

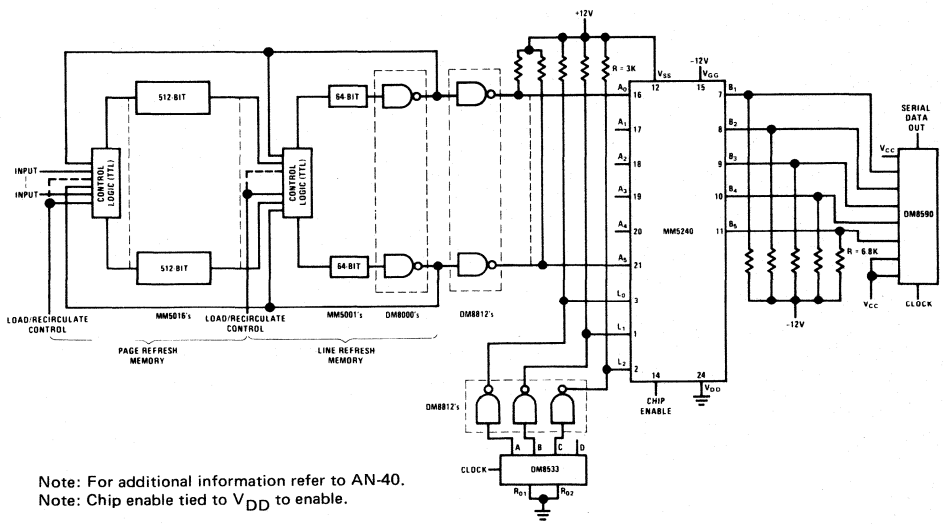
connection diagram



Order Number MM4240J or MM5240J
See NS Package J24A

Order Number MM5240N
See NS Package N24B

typical application



Note: For additional information refer to AN-40.
Note: Chip enable tied to V_{DD} to enable.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 30V
V_{DD} Supply Voltage		V_{SS} – 15V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		–65°C to +150°C
Operating Temperature	MM4240	–55°C to +125°C
	MM5240	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1MΩ to GND			V_{SS} – 9.0	V
Logical "0"		V_{SS} – 1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.5			V
Output Current Capability					
Logical "0"	$V_{OUT} = V_{SS} - 6.0V$	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 8.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	$T_A = 25°C$				
I_{DD}	MOS Load		25	40	mA
I_{GG} (Note 2)				1	μA
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, $V_{IN} = 0V$		5	8	pF
V_{GG} Capacitance (Note 5)	f = 1.0 MHz, $V_{IN} = 0V$		25	40	pF
Address Time (Note 3)	See Timing Diagram				
T_{ACCESS}	$T_A = 25°C$	150	425	500	ns
Output AND Connection	MOS Load			4	
(Note 4)	TTL Load			10	

Note 1: These specifications apply for $V_{SS} = +12V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, and $T_A = -55°C$ to +125°C (MM4240) $T_A = 0°C$ to +70°C (MM5240) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns

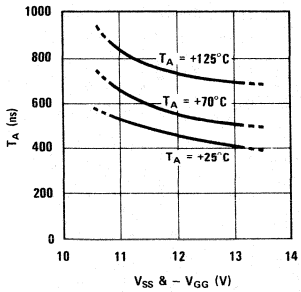
Where N = Number of AND connections.

The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

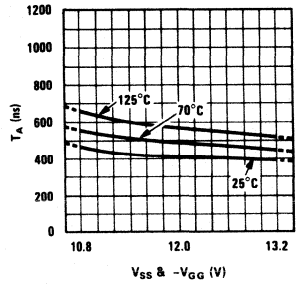
Note 5: Guaranteed by design.

performance characteristics

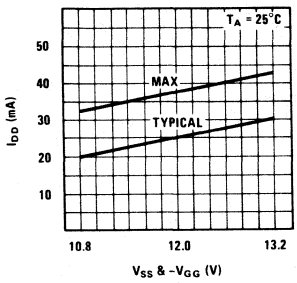
Guaranteed Access Time (T_A) vs Supply Voltage



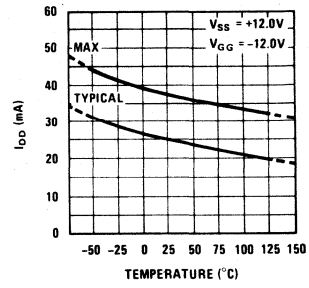
Typical Access Time (T_A) vs Supply Voltage



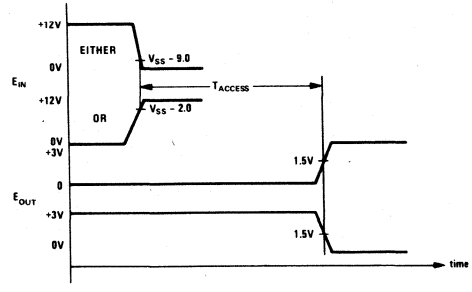
Power Supply Current vs Voltage

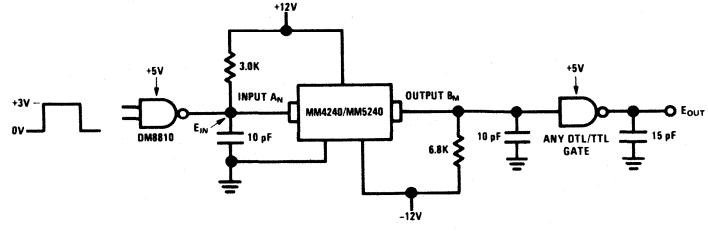


V_{DD} Power Supply Current vs Temperature

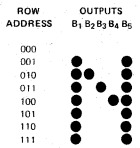


timing diagram/address time





MM4240AA/MM5240AA character font



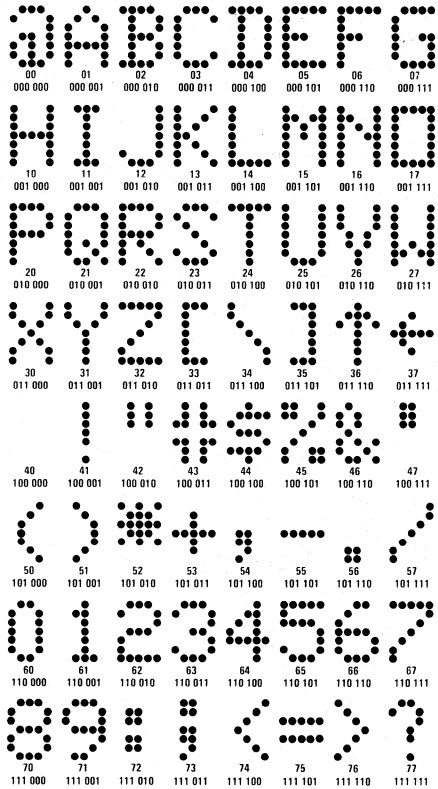


FIGURE 4

Note: Negative logic assumed.

MM4240/MM5240AA, AE, ABU, ABZ, ACA
MM4241/MM5241ABL, ABU, ABW, ABX, ABY
American and European Character Fonts

Ten popular American and European 64-character subsets for displays and printers are now available from National as single-chip, standard character generators. These parts, listed in Table 1, are sold off-the-shelf without a ROM masking charge.

The ROMs are static, bipolar-compatible types, operating without clocks on standard power supplies. Row and column access times are typically 450 and 700 ns respectively. An MM4240/MM5240 2560-bit ROM is used for the 5 x 7 horizontal-scan fonts and an MM4241/MM5241 3072-bit ROM for the 7 x 5 vertical-scan fonts. The MM4240 and MM4241 operate at −55°C to +125°C and the MM5240 and MM5241 at −25°C to +70°C.

Input-output configurations and character formats for the ROMs are shown in Figures 1 and 2. Application Note *AN-40 The Systems Approach to Character Generators* gives examples of line and column address-control logic, and CRT and printer operating techniques. Refer to the MM4240/MM5240 in this section and MM4241/MM5241 in section 8 for electrical specifications and ordering information.

TYPE NUMBER	CODE	64-CHARACTER SUBSET	FIGURE		
Horizontal Scan (5 x 7)				CE	
MM4240AA/MM5240AA	ASCII	Upper-case alphanumeric	3	1	
MM4240AE/MM5240AE	ASCII	Lower-case alpha and symbols	4	1	
MM4240ABU/MM5240ABU	Hollerith	Upper-case alphanumeric	5	1	
MM4240ABZ/MM5240ABZ	EBCDIC-8	Upper-case alphanumeric	6	1	
MM4240ACA/MM5240ACA	EBCDIC	Upper-case alphanumeric (IBM)	7	1	
Vertical Scan (7 x 5)				CE1	CE2
MM4241ABL/MM5241ABL	ASCII	Upper-case alphanumeric	8	1	1
MM4241ABV/MM5241ABV	ECMA	Upper-case A/N, Scandinavian	9	1	1
MM4241ABW/MM5241ABW	ECMA	Upper-case A/N, German	10	1	1
MM4241ABX/MM5241ABX	ECMA	Upper-case A/N, general European (French, British, Italian)	11	1	1
MM4241ABY/MM5241ABY	ECMA	Upper-case A/N, Spanish	12	1	1

TABLE 1. Single Chip, Standard Horizontal-Scan and Vertical-Scan Character Generators

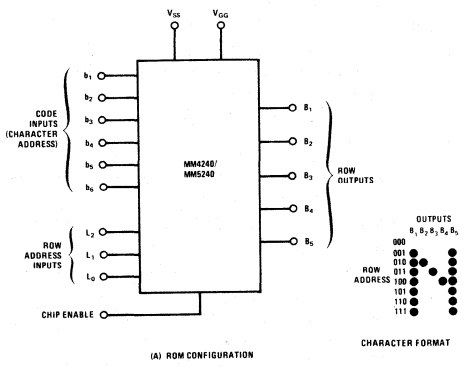


FIGURE 1. Horizontal-Scan Character Generator ROM

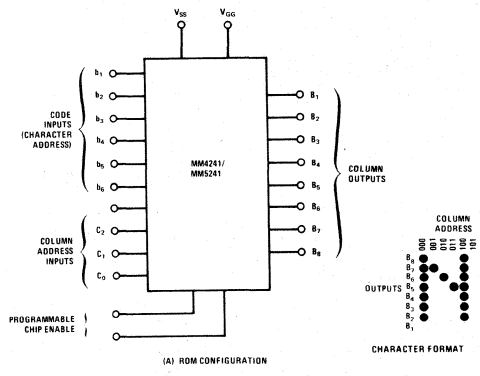


FIGURE 2. Vertical-Scan Character Generator ROM

Note that each ROM has a chip-enable input to permit multi-ROM operation with common control logic. For instance, two horizontal-scan ASCII character generators may be operated in tandem to obtain upper and lower-case characters. In this case, chip-enable would be controlled with bit b_6 of the normal 7-bit ASCII code, and its complement, $\overline{b_6}$.

HORIZONTAL SCAN FONTS

The subsets of 64 5 x 7 characters in the horizontal-scan fonts are the ones most commonly used in low-cost TV and CRT raster-scan displays and dot-matrix line printers.

MM4240AA/MM5240AA contains the ASCII-6 preferred graphic subset, formed from ASCII-7 by ignoring bit b_6. The remaining six bits form two octal address characters. One is formed by the three more significant bits, b_7, b_5 and b_4, and the second by b_3, b_2 and b_1.

Also, characters 36 and 37 in ASCII (x3.4 1968)* are respectively a carat (or circumflex), and an underscore. These are awkward in a video display, so they are replaced by the more useful arrows. (The arrows are related to characters in an older teletypewriter set.) This font is shown in Figure 3. The MM4240/MM5240 data sheet should be referred to for operating characteristics of all the horizontal-scan character generators.

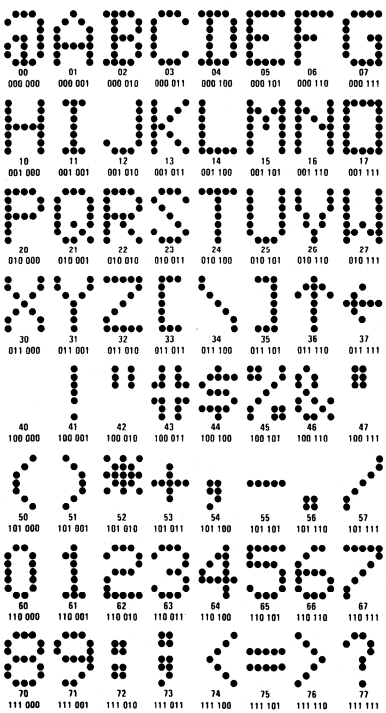


FIGURE 3. MM4240AA/MM5240AA Horizontal-Scan ASCII-7 Graphic Subset

MM4240AE/MM5240AE generates unique symbols describing the ASCII-7 control codes, as well as lower-case letters (Figure 4). The designer may not wish to display or dot-print the symbols. Since the symbols are generated only when the most significant address bit is logic "0", this bit line may be used to disable the chip, and blank the screen when control signals are transmitted. If not, the system designer can use the symbols as he likes.

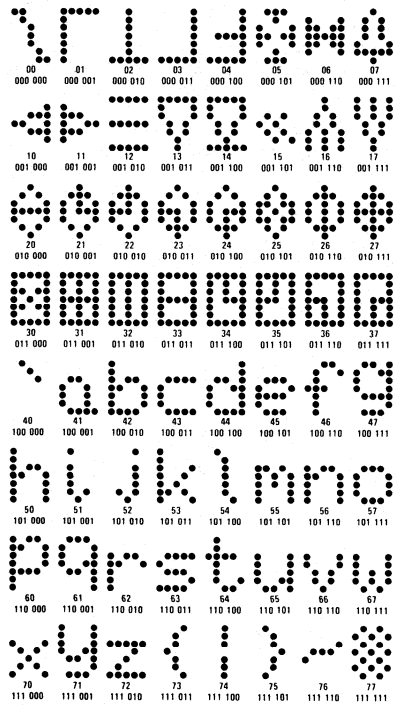


FIGURE 4. MM4240AE/MM5240AE Horizontal-Scan ASCII-7 Lower-Case Graphic and Control Symbol Subset

The Hollerith character subset in Figure 5b is formed by using six gates to compress the 12-line Hollerith code to the 6-bit address for 64 characters, as shown in Figure 5a.

As shown in Figure 6, an ASCII-compatible subset is provided by the EBCDIC-8 character generator (MM4240ABZ/MM5240ABZ) by simply ignoring the two most significant bits, b_0 and b_1, in the EBCDIC-8 code. The ABZ version follows the ANSI standard, while the ACA version follows the IBM style. A cent sign, and IBM's logical OR and logic NOT signs are given by the ACA subset (characters 12, 17, and 37). And a plus or minus sign is provided, as character 52. (See Figure 7.)

*American National Standards Institute (ANSI)

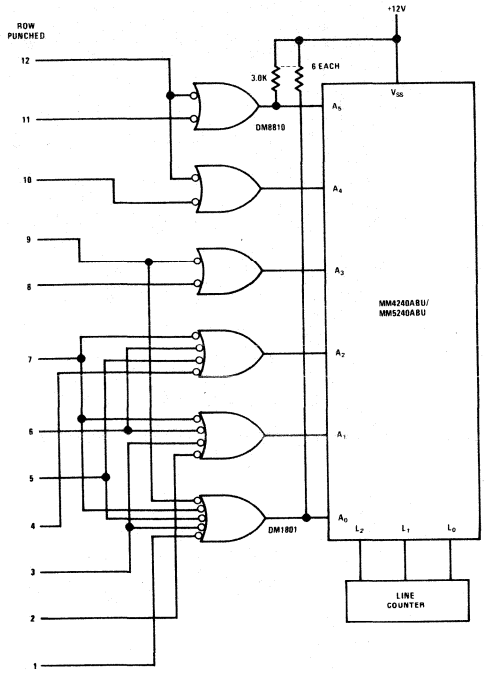


FIGURE 5a. MM4240ABU/MM5240ABU Typical Address Inputs

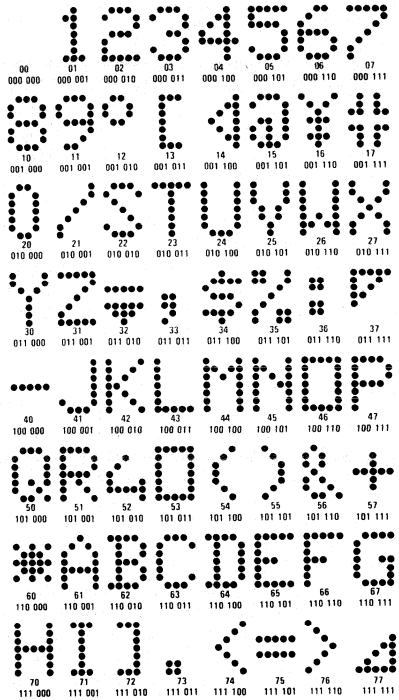


FIGURE 5b. MM4240ABU/MM5240ABU Horizontal Scan Hollerith Graphics Subset

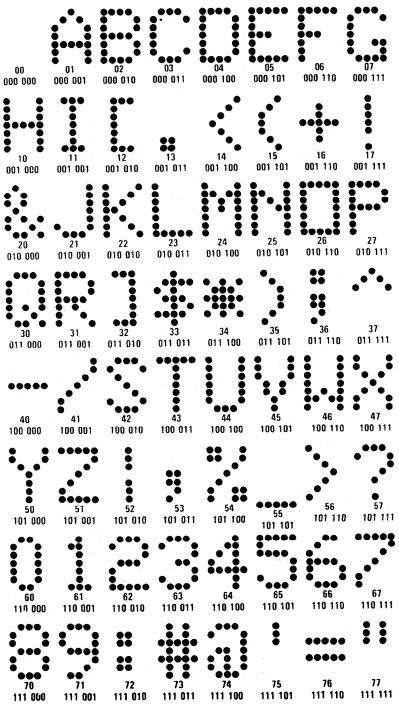


FIGURE 6. MM4240BABZ/MM5240BABZ Horizontal-Scan EBCDIC-8 Graphic Subset

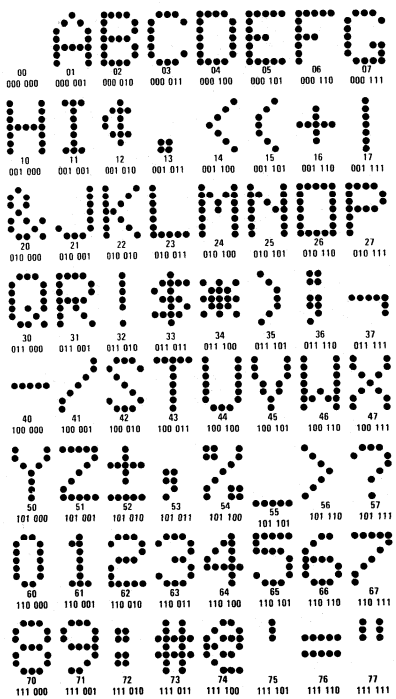


FIGURE 7. MM4240ACA/MM5240ACA Horizontal-Scan IBM EBCDIC Graphic Subset

VERTICAL SCAN FONTS

All five of the standard vertical-scan subsets in Figures 8 through 12 are generated with 6-bit codes derived from code recommendations R646 of the International Organization for Standardization. These recommendations cover ASCII-7, European ECMA-7 and CCITT alphabet number 5.

The ASCII subset for American use, in Figure 8, is practically identical to the horizontal-scan subset. Those in Figures 9 through 12 follow preferred character styles in the countries indicated. The underscore (character 37) is dropped below the line so that it may be used as a cursor.

Vertical-scan character generators are generally used in dot-matrix tape printers, ink-dot spray printers and high-definition sawtooth or pedestal-scan CRT displays. They may also be used to control raster-scan TV tubes or CRTs if the tube is turned on its side so that the raster scan is made vertically to provide a page-like format.

With standard programming, the bits in the column outputs are sequenced for a sawtooth scan with dot columns running in the same direction, as illustrated in Figure 13a. For a pedestal scan, Figure 13b, alternate columns can be reversed by putting an 8-bit shift left/shift right TTL shift register (DM74198) on the output as illustrated in Figure 14.

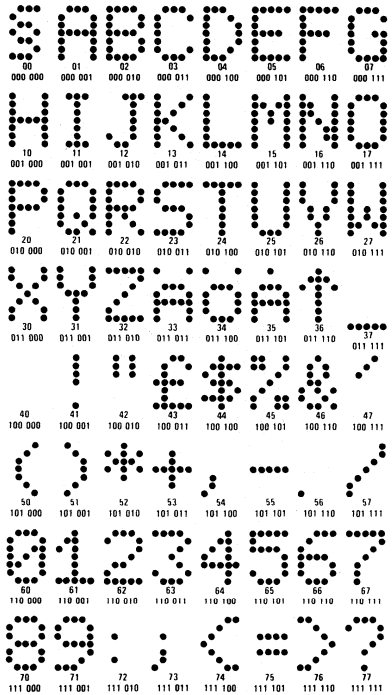


FIGURE 9. MM4241ABV/MM5241ABV Vertical Scan ECMA-7 Font for Scandinavian Use

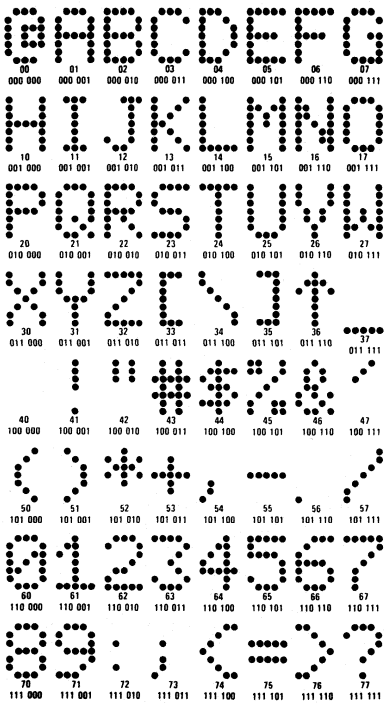


FIGURE 8. MM4241ABL/MM5241ABL Vertical-Scan ASCII-7 Graphic Subset

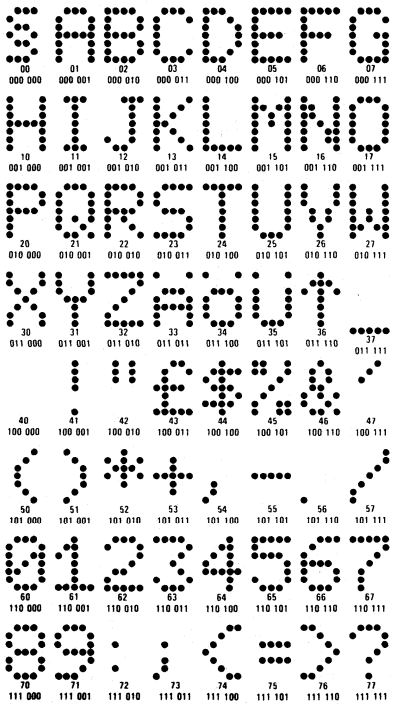


FIGURE 10. MM4241ABW/MM5241ABW Vertical-Scan ECMA-7 Font for German Use

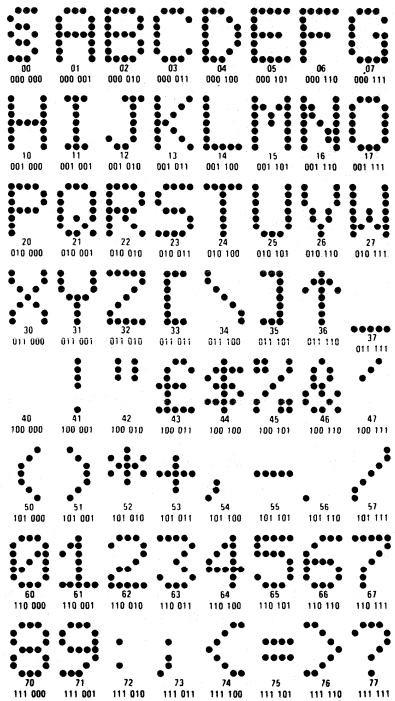


FIGURE 11. MM4241ABX/MM5241ABX Vertical-Scan ECMA-7 Font for General European Use (French, British, Italian)

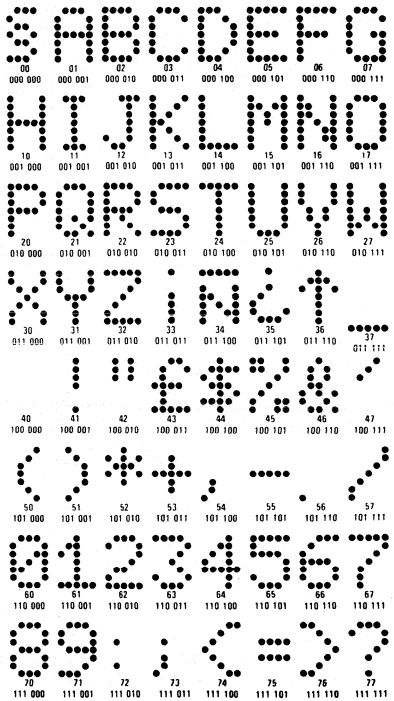


FIGURE 12. MM4241ABY/MM5241ABY Vertical-Scan ECMA-7 Font for Spanish Use

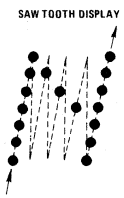


FIGURE 13a. Sawtooth Vertical Scan

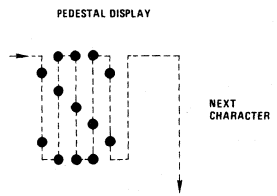


FIGURE 13b. Pedestal Vertical Scan

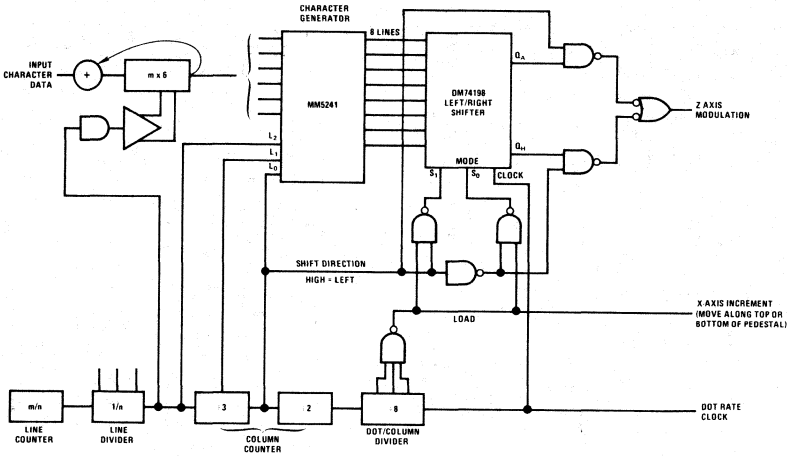


FIGURE 14. Conversion of Sawtooth Output to Pedestal Scan

CUSTOM FONTS

The two ROMs can also be custom-programmed to provide special characters, or fonts larger than 5 x 7. The MM4240/MM5240 actually stores 64 5 x 8 characters or character segments and the MM4241/MM5241 stores 64 8 x 6 characters or segments. They are not limited to 5 x 7 and 7 x 5. For example, the extra height may be used in an otherwise 5 x 7 font to drop the tails of commas, semicolons and lower-case letters below the bottom line of the capital letters. Fonts as large as 16 x 12 are entirely practical without additional control logic, using the chip-enable feature of four MM5241s. Large-font organizations are discussed in AN-40.

National Semiconductor

MM52116FDW, MM52116FDX Character Generators

General Description

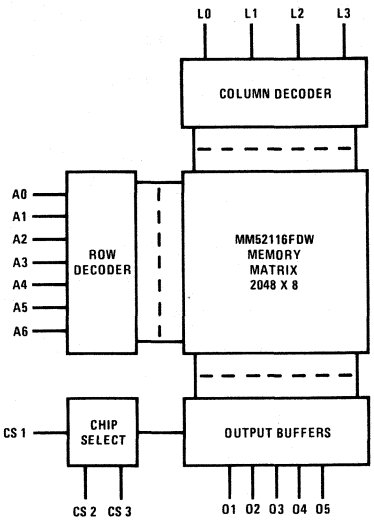
The MM52116FDW, MM52116FDX are 128-character, N-channel, silicon-gate character generators designed primarily for CRT display applications. The MM52116FDW/MM52116FDX provide 5x7 and 7x9 row scan character fonts, respectively. They provide complete DTL/TTL compatibility with single 5V power supply operation.

Features

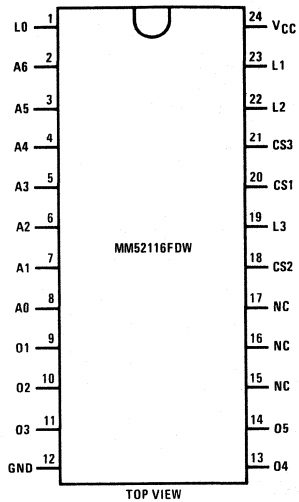
- 128-character row scan
- 5x7 or 7x9 font
- Maximum access time — 450 ns
- TRI-STATE® outputs for bus interface
- Programmable chip selects
- Single 5V power supply
- Inputs and outputs TTL compatible
- MM2316E and MM2716 pin compatible

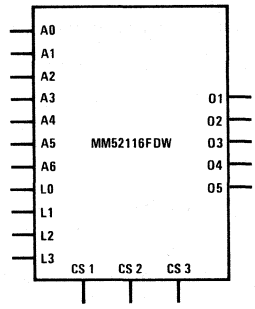
Block Diagrams, Connection Diagrams and Logic Symbols

Chip Select Enable Pattern CS1 = 0, CS2 = 0, CS3 = 1



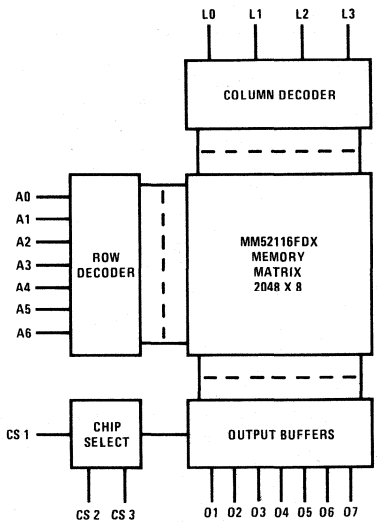
Dual-In-Line Package



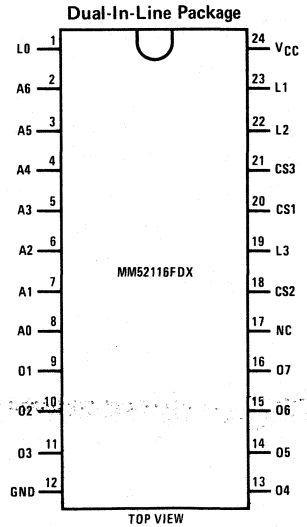


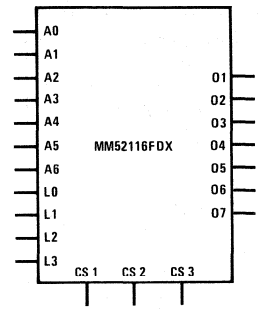
Order Number MM52116FDW-J
See NS Package J24A

Order Number MM52116FDW-N
See NS Package N24B



Dual-In-Line Package





Order Number MM52116FDX-J
See NS Package J24A

Order Number MM52116FDX-N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise noted).

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Current (I_{LI})	V_{IN} = 0 to V_{CC}			10	μA
Logical "1" Input Voltage (V_{IH})		2.0		V_{CC}+1.0	V
Logical "0" Input Voltage (V_{IL})		−0.5		0.8	V
Logical "1" Output Voltage (V_{OH})	I_{OH} = −100 μA	2.2			V
Logical "0" Output Voltage (V_{OL})	I_{OL} = 2 mA			0.45	V
Output Leakage Current (I_{LOH})	V_{OUT} = 4V, CS = 2.2V			10	μA
Output Leakage Current (I_{LOL})	V_{OUT} = 0.45V, CS = 2.2V			−20	μA
Power Supply Current (I_{CC1})	All Inputs = 5.25V, Data Output Open		40	98	mA

Capacitance

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Capacitance (All Inputs) (C_{IN})	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
Output Capacitance (C_{OUT})	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise specified).
See ac test circuit and switching time waveforms.

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{ACCESS}	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 1)*			450	ns
t_{SELECT}	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 2)*			300	ns
$t_{DESELECT}$	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 2)*			300	ns

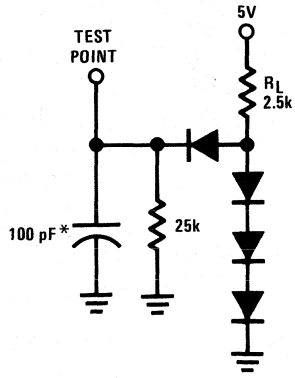
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



*Includes jig capacitance

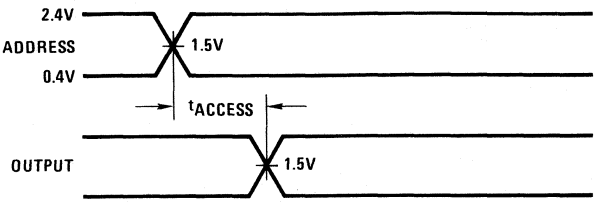


FIGURE 1. Access Time

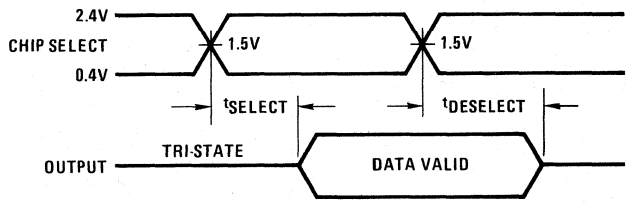


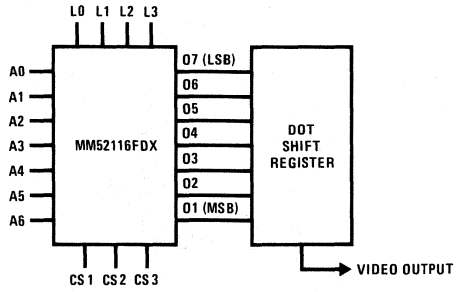
FIGURE 2. Output Enable and Disable

Functional Description

The chip is selected by applying the proper logic levels to the 3-chip select pins. A 7-bit binary word must be present at the character address inputs, A0–A6 to select a character. The dot matrix of selected characters is generated by cycling the line count address inputs L0–L3 through the line counts necessary to generate the characters. A dot is generated when an output is a "1" (at V_{OH}).

Figure 3 shows an example of the conditions required at the address and line count pins to generate the dot matrix of the character A. *Figures 5 and 6* show the character fonts of the MM52116FDW and MM52116FDX.

Functional Description (Continued)



CHIP SELECT			CHARACTER ADDRESS							LINE COUNT				DOT MATRIX							
CS 1	CS 2	CS 3	A6	—	—	A4	A3	—	—	—	A0	L3	L2	L1	L0	O1	—	—	—	—	—	—	O7
1	0	1	1	0	0	0	0	0	0	1		0	0	0	0	0	0	1	1	1	0	0
												0	0	0	1	0	1	0	0	0	1	0
												0	0	1	0	1	0	0	0	0	0	1
												0	0	1	1	1	0	0	0	0	0	1
												0	1	0	0	1	0	0	0	0	0	1
												0	1	0	1	1	1	1	1	1	1	1
												0	1	1	0	1	0	0	0	0	0	1
												0	1	1	1	1	0	0	0	0	0	1
												1	0	0	0	1	0	0	0	0	0	1

Note. A "1" = V_{IH} for address, line count and chip select inputs and a "1" = V_{OH} for outputs.

FIGURE 3. Example of Generating the Character A

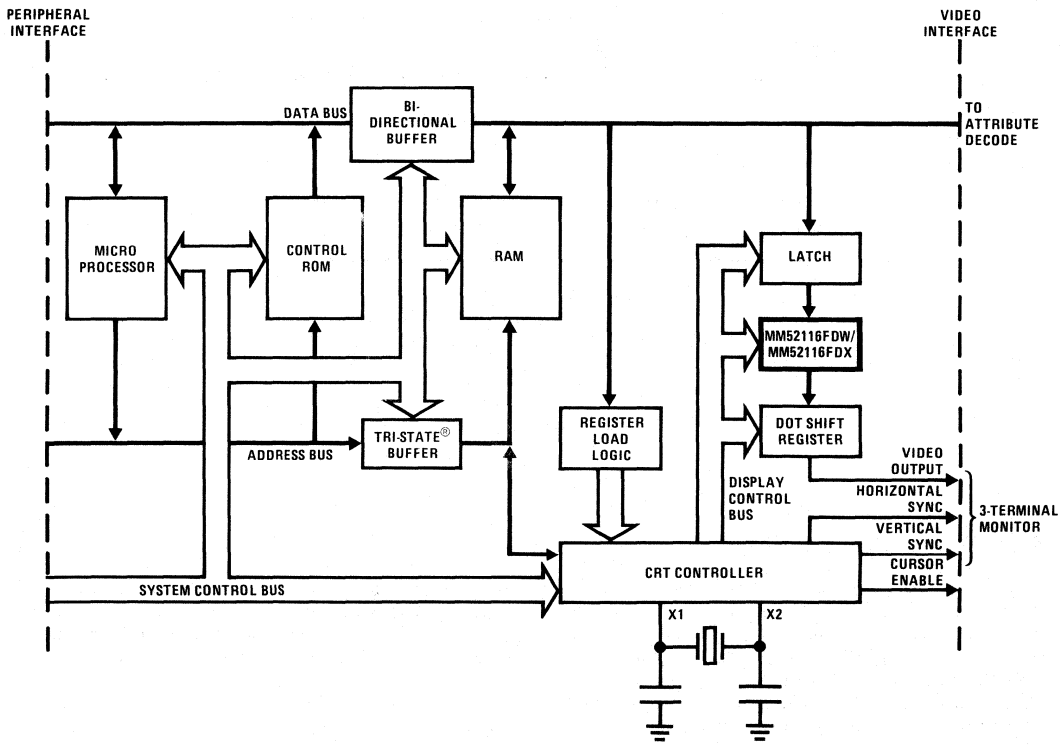


FIGURE 4. Typical MM52116FDW and MM52116FDX Application

Functional Description (Continued)

A6	A5 A4 A3 \ A2 A1 A0	000	001	010	011	100	101	110	111
0	000								
0	001								
0	010								
0	011								
0	100								
0	101								
0	110								
0	111								
1	000								
1	001								
1	010								
1	011								
1	100								
1	101								
1	110								
1	111								

FIGURE 5. MM52116FDW

Functional Description (Continued)

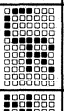
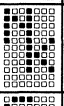
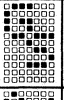
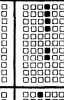
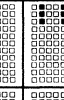
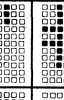
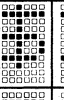
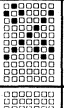
A6	A5 A4 A3 \ A2 A1 A0	000	001	010	011	100	101	110	111
0	000								
0	001								
0	010								
0	011								
0	100								
0	101								
0	110								
0	111								
1	000								
1	001								
1	010								
1	011								
1	100								
1	101								
1	110								
1	111								

FIGURE 6. MM52116FDX

Functional Description (Continued)

MM52116FDX ASCII CHARACTER SET IN HEXADECIMAL REPRESENTATION

Character	7-Bit Hexadecimal Number	Character	7-Bit Hexadecimal Number	Character	7-Bit Hexadecimal Number	Character	7-Bit Hexadecimal Number
NUL	00	SP	20	@	40	\	60
SOH	01	!	21	A	41	a	61
STX	02	"	22	B	42	b	62
ETX	03	#	23	C	43	c	63
EOT	04	$	24	D	44	d	64
ENQ	05	%	25	E	45	e	65
ACK	06	&	26	F	46	f	66
BEL	07	'	27	G	47	g	67
BS	08	(	28	H	48	h	68
HT	09	)	29	I	49	i	69
LF	0A	*	2A	J	4A	j	6A
VT	0B	+	2B	K	4B	k	6B
FF	0C	,	2C	L	4C	l	6C
CR	0D	-	2D	M	4D	m	6D
SO	0E	.	2E	N	4E	n	6E
SI	0F	/	2F	O	4F	o	6F
DLE	10	0	30	P	50	p	70
DC1	11	1	31	Q	51	q	71
DC2	12	2	32	R	52	r	72
DC3	13	3	33	S	53	s	73
DC4	14	4	34	T	54	t	74
NAK	15	5	35	U	55	u	75
SYN	16	6	36	V	56	v	76
ETB	17	7	37	W	57	w	77
CAN	18	8	38	X	58	x	78
EM	19	9	39	Y	59	y	79
SUB	1A	:	3A	Z	5A	z	7A
ESC	1B	;	3B	[	5B		7B
FS	1C	<	3C	\	5C		7C
GS	1D	=	3D	]	5D	ALT	7D
RS	1E	>	3E	↑	5E	ESC	7E
US	1F	?	3F	←	5F	DEL,RUBOUT	7F

Custom Character Font Ordering Information

General

The basic part used for the MM52116FDW and MM52116FDX has the capability of a full 8x16 font for 128 characters. The user can also implement 256 characters with an 8x8 font for unique graphic displays.

Custom character fonts are submitted to National in 3 formats: punched cards, paper tape or truth table, with punched cards being the preferred. These programs are converted into machine language and outputted on a magnetic tape. This magnetic tape is used to make the programmable mask and the test tape. The wafers are tested at the wafer level. The wafer is then scribed and the good dice assembled. After assembly, the units are tested using the custom test tape to assure the correct output pattern for every address.

Definitions

A logical "1" = V_{IH} = 2.0V min and a logical "0" = V_{IL} = 0.8V max for chip selects, line count, and character address inputs.

A logical "1" = V_{OH} = 2.2V min and a logical "0" = V_{OL} = 0.45V max for the outputs.

A0 is the least significant character address bit and L0 is the least significant line count bit.

O7 is the last bit serialized by the DOT SHIFT REGISTER *(Figure 3)*.

Information Needed

So that National can better serve its customers, the following information *must* be submitted with each custom order.

National Semiconductor Corporation 2900 Semiconductor Dr., Santa Clara, CA 95051 Phone (408) 737-5000 TWX 910-339-9240				NATIONAL PART NUMBER
				ALPHA CODE (NATIONAL USE ONLY)
NAME				DATE
ADDRESS				CUSTOMER PRINT OR I.D. NO.
CITY		STATE	ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE		DATE
CHIP SELECT ENABLING CODE (USE 1, 0 PATTERN) CS1 _____ CS2 _____ CS3 _____				

Standard Data Format

The following format is to be used with punched cards, paper tape, or truth table data entry. Punched cards are preferred and each line entry of the standard format represents a card with the blocks of data separated horizontally by one space. When paper tape is used it is punched in the "card image", with each line entry separated by a "carriage return", "line feed", and a single space separating blocks of data as with cards. A truth table would simply list the data in the format shown.

The decimal notation used for the character address and line count simplifies the format. The example in *Figure 3* indicates that binary is used for the character addressing and line count.

Custom Character Font Ordering Information (Continued)

M M 5 2 1 1 6 F D X (Note 1)			
P O S (Note 2)			
C S 1 0	(Note 3)		
C S 2 0			
C S 3 1		O1 (Bit 1) … O7 (Bit 7)	(Note 4)
C 0 0 0	L 0 0	1 0 0 0 1 0 0	2
C 0 0 0	L 0 1	1 1 0 0 1 0 0	3
C 0 0 0	L 0 2	1 0 1 0 1 0 0	3
C 0 0 0	L 0 3	1 0 0 1 1 0 0	3
C 0 0 0	L 0 4	1 0 1 0 1 0 1	4
C 0 0 0	L 0 5	0 0 1 0 0 0 1	2
C 0 0 0	L 0 6	0 0 1 0 0 0 1	2
C 0 0 0	L 0 7	0 0 1 0 0 0 1	2
C 0 0 0	L 0 8	0 0 0 1 1 1 0	3
C 0 0 0	L 0 9	0 0 0 0 0 0 0	0
C 0 0 0	L 1 0	0 0 0 0 0 0 0	0
C 0 0 1	L 0 0	0 1 1 1 0 0 0	3
C 0 0 1	L 0 1	1 0 0 0 0 0 0	1
C 0 0 1	L 0 2	0 1 1 0 0 0 0	2
C 0 0 1	L 0 3	0 0 0 1 0 0 0	1
C 0 0 1	L 0 4	1 1 1 0 0 0 1	4
C 0 0 1	L 0 5	0 0 1 0 0 0 1	2
C 0 0 1	L 0 6	0 0 1 1 1 1 1	5
C 0 0 1	L 0 7	0 0 1 0 0 0 1	2
C 0 0 1	L 0 8	0 0 1 0 0 0 1	2
C 0 0 1	L 0 9	0 0 0 0 0 0 0	0
C 0 0 1	L 1 0	0 0 0 0 0 0 0	0
(Note 5)	(Note 6)	(Note 7)	
. . .	. . .	. . .	
C 1 2 7	L 0 0	0 1 0 0 1 0 0	2
C 1 2 7	L 0 1	1 0 0 1 0 0 1	3
C 1 2 7	L 0 2	0 0 1 0 0 1 0	2
C 1 2 7	L 0 3	0 1 0 0 1 0 0	2
C 1 2 7	L 0 4	1 0 0 1 0 0 1	3
C 1 2 7	L 0 5	0 0 1 0 0 1 0	2
C 1 2 7	L 0 6	0 1 0 0 1 0 0	2
C 1 2 7	L 0 7	1 0 0 1 0 0 1	3
C 1 2 7	L 0 8	0 0 1 0 0 1 0	2
C 1 2 7	L 0 9	0 0 0 0 0 0 0	0
C 1 2 7	L 1 0	0 0 0 0 0 0 0	0
T B 1	2 5 6	(Note 8)	
T B 2	2 6 9		
T B 3	2 8 3		
T B 4	4 1 8		
T B 5	3 0 3		
T B 6	2 4 7		
T B 7	4 4 8		

Note 1: Specify the product type, MM52116FDX or MM52116FDW.

Note 2: This indicates that positive logic is used as defined in the Definitions section.

Note 3: The one-zero logic pattern that will enable the device. Positive logic is used.

Note 4: The total numbers of Ones in the row (output word).

Note 5: The character address in decimal notation preceded by a "C". Leading zeroes are used.

Note 6: The line count in decimal notation preceded by a "C". Leading zeroes are used. The line count will go from L0 to L8 for the MM52116FDW.

Note 7: The output word representing one row of dots at the specified character address and line count. A One is a dot. There will only be 5 bits (columns) for the MM52116FDW.

Note 8: The total number of Ones in each output position (column). Leading zeroes are used. Only 5 entries (TB1—TB5) are necessary for the MM52116FDW.

National Semiconductor

DM8678 Bipolar Character Generator

general description

The DM8678 is a 64-character bipolar character generator with serial output designed primarily for the CRT display marketplace, and packaged in a standard 16-pin DIP. The DM8678 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM8678 performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing. These system functions have required extra packages in the past.

Shifted characters can be generated by the on-chip subtractor.

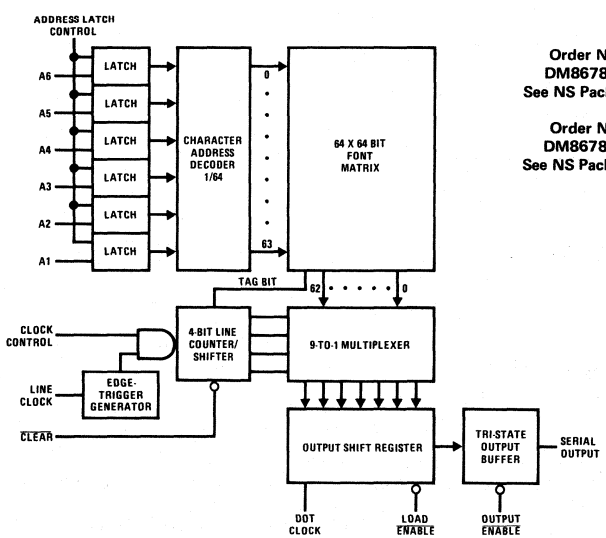
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. Load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "fall through" the latch. And when the address latch control signal goes low, the character addresses are latched.

features

- 64-character—row scan
- 5 x 7 or 7 x 9 font
- Shifted lower case descending characters
- Serial output
- 16-pin package
- 16 MHz min clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- TRI-STATE® output

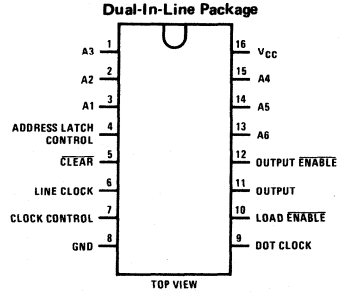
	ROW SCAN	7 x 9	5 x 7	FONT	PACKAGE
DM8678BWF	X	X		Upper Case Block Letters	N, J
DM8678CAE	X	X		Shifted Lower Case Block	N, J
DM8678CAB	X		X	Upper Case Block Letters	N, J
DM8678CAH	X		X	Shifted Lower Case Block	N, J
DM8678CAD	X	X		Kata Kana	N, J
DM8678BTK	X	X		Upper Case Script Letters	N, J
DM8678CAS	X	X		IBM 3741 Selectric	N, J

block diagram



connection diagram

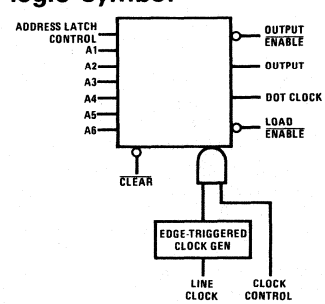
Dual-In-Line Package



Order Number DM8678XXX/J
See NS Package J16A

Order Number DM8678XXX/N
See NS Package N16A

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−0.8	−1.6	mA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−0.8	−1.5	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	145	mA
	TRI-STATE PARAMETERS					
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max	−15		−50	mA
I_{HZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±40	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2		V

ac electrical characteristics (With standard load) (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Access Time					
T_{DO}	Dot Clock to Output			35	55	ns
T_{EA}	Output Enable			20	45	ns
T_{ER}	Output Disable			20	45	ns
	Set-Up Time					
T_{S1}	Load to Dot Clock		40	25		ns
T_{S2}	Address to Load		350	200		ns
T_{S3}	Clear to Load	See Switching Time Waveforms	350			ns
T_{S4}	Control to Line Clock		40			ns
T_{S5}	Line Clock to Load		950			ns
T_{S6}	Address to Address Latch		40			ns
	Hold Time					
T_{H1}	Load from Dot Clock		0			ns
T_{H2}	Address from Load		0			ns
T_{H3}	Control from Line Clock		100			ns
T_{H4}	Address from Address Latch		40			ns

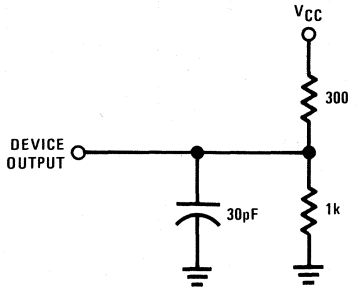
ac electrical characteristics (Continued) (With standard load) (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Pulse Width					
T_{W1}	Line Clock		40			ns
T_{W2}	Clear		40			ns
T_{W3}	Dot Clock	See Switching Time Waveforms	30			ns
T_{W4}	Load		40			ns
T_{W5}	Address Latch		40			ns
f_{MAX}	Maximum Clock Frequency		16	20		MHz

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

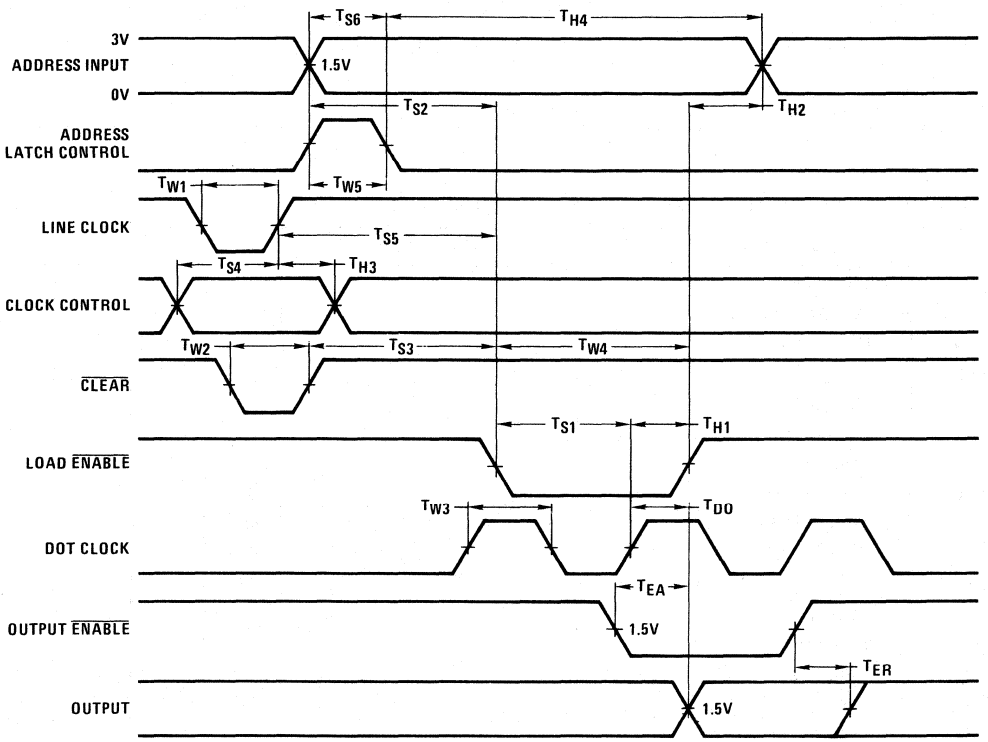
Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

standard test load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, $t_r < 5$ ns and $t_f < 5$ ns (between 1.0V and 2.0V).
- T_{DO} is measured with output enable at a steady low level.

switching time waveforms



truth tables

a) Address Latch

ADDRESS LATCH CONTROL	FUNCTION PERFORMED
0	Latched
1	Fall Through

b) Output

OUTPUT $\overline{\text{ENABLE}}$	STATE OF THE OUTPUT
1	Output Hi-Z
0	Data Out

c) 4-Bit Line Counter

CLOCK CONTROL	LINE CLOCK	$\overline{\text{CLEAR}}$	LINE COUNTER
H	⌐	H	Increment line counter
X	X	L	Asynchronous clear resets counter
L	X	H	Clock inhibited
H	¬	H	No change on high-to-low clock edge

X = Don't care

definitions

A1–A6: Character address. A 6-bit code which selects 1 of the 64 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if load $\overline{\text{enable}}$ is low or shifts data if load $\overline{\text{enable}}$ is high.

Output $\overline{\text{Enable}}$: An active low output enable. When high the output is in the Hi-Z state.

Output: A TTL TRI-STATE output buffer.

functional description

To select a character, a 6-bit binary word must be present at the address inputs A1–A6 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the $\overline{\text{clear}}$ input receives a low pulse, the counter is reset to zero. The shift register can be loaded (T_{S2} ns) after the character is addressed. Data, representing one horizontal line of the addressed character, is available at the output when the load $\overline{\text{enable}}$ input is brought low. As shown in *Figure 1*, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out one line of the character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the $\overline{\text{clear}}$ input low. Detailed system application infomation is contained in application note AN-167 available from National.

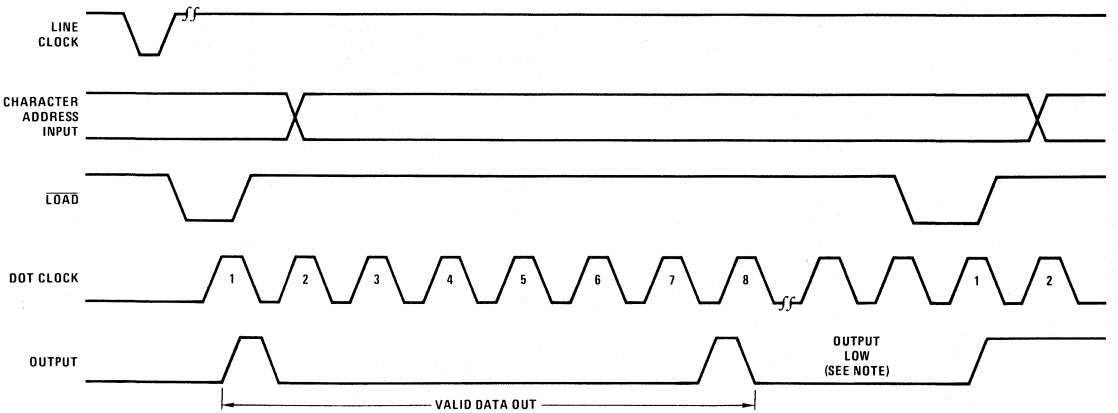
A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4.*

A chip select input is provided for expansion of the character font. The various standard fonts are shown in *Figures 5, 6, 7, 8, 9 and 10.*

functional description (Continued)

Character Cycle – ROM data corresponding to one line of characters is loaded into the shift register T_{S2} after the ROM is addressed. When load $\overline{\text{enable}}$ goes low, ROM data is allowed to be present at the D input of the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load $\overline{\text{enable}}$ goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

Line Cycle – The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the $\overline{\text{clear}}$ input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until Load $\overline{\text{enable}}$ is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle

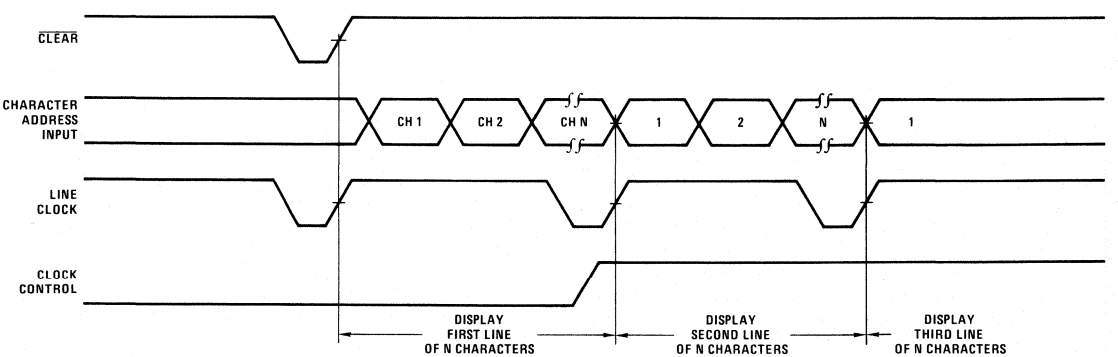


FIGURE 2. Line Cycle

functional description (Continued)

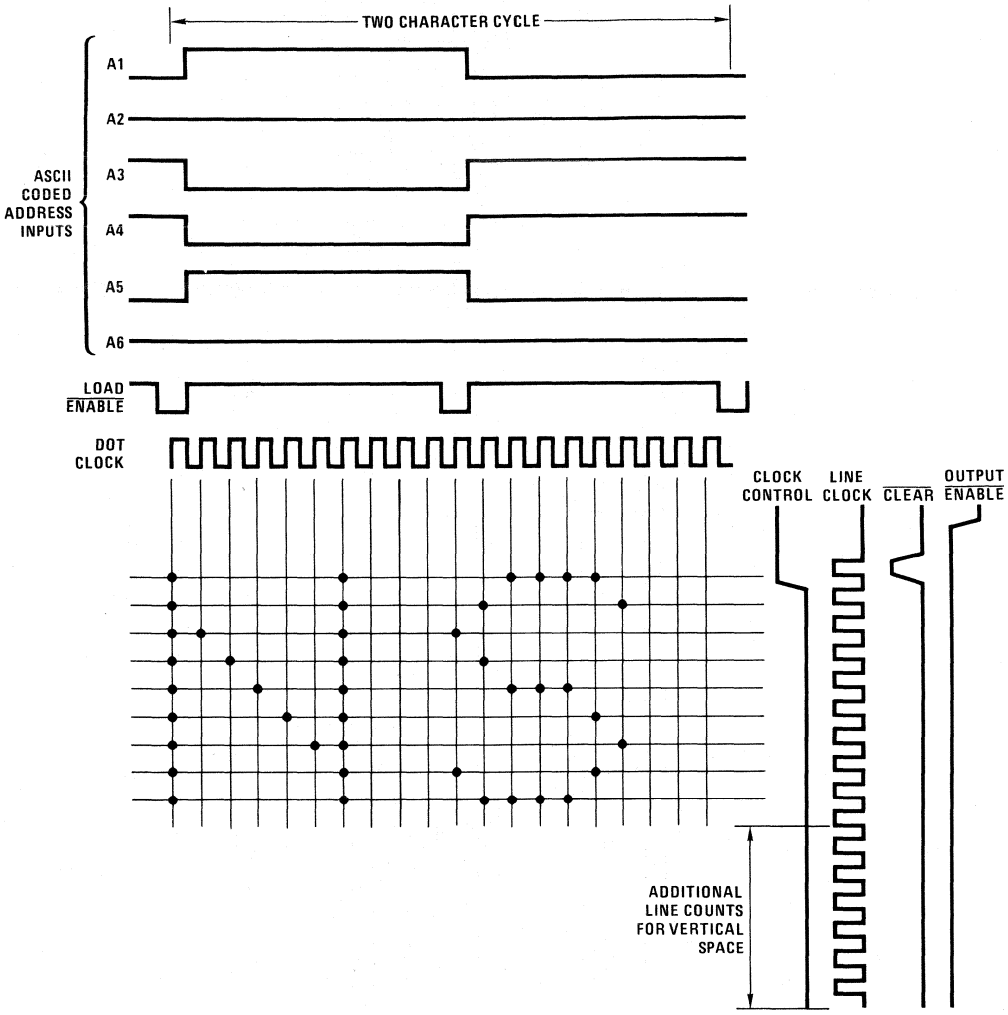
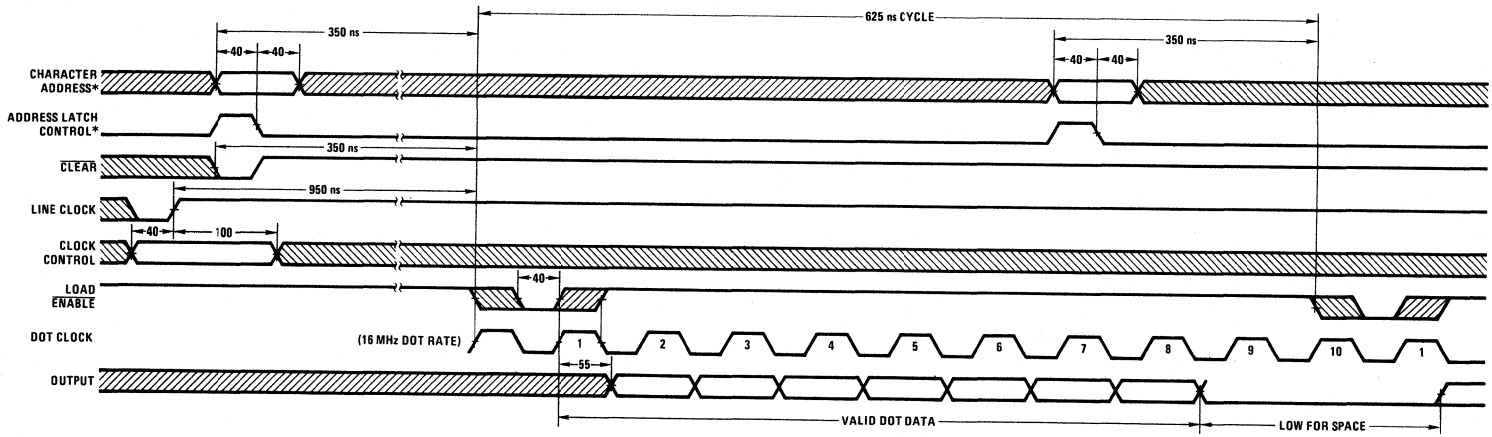


FIGURE 3. Example of Two Characters Display Timing



*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 350 ns before the high-to-low transition of Load $\overline{\text{enable}}$.

FIGURE 4. Typical System Timing Waveform

functional description (Continued)

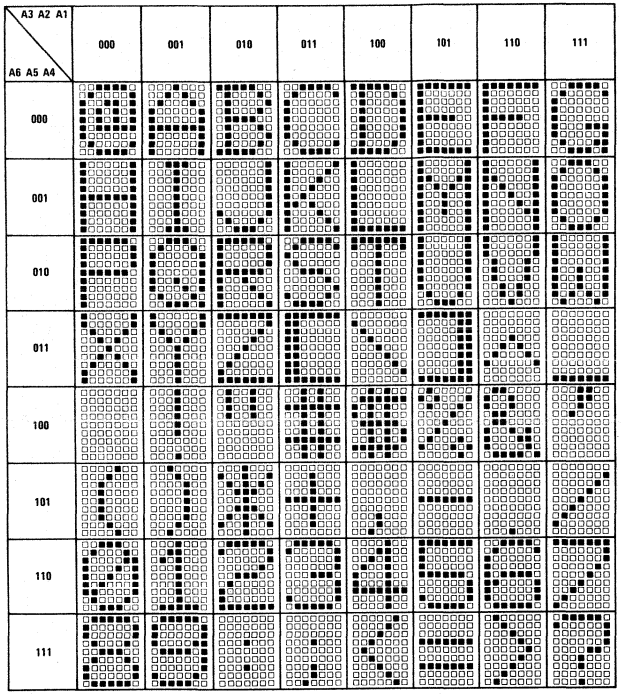
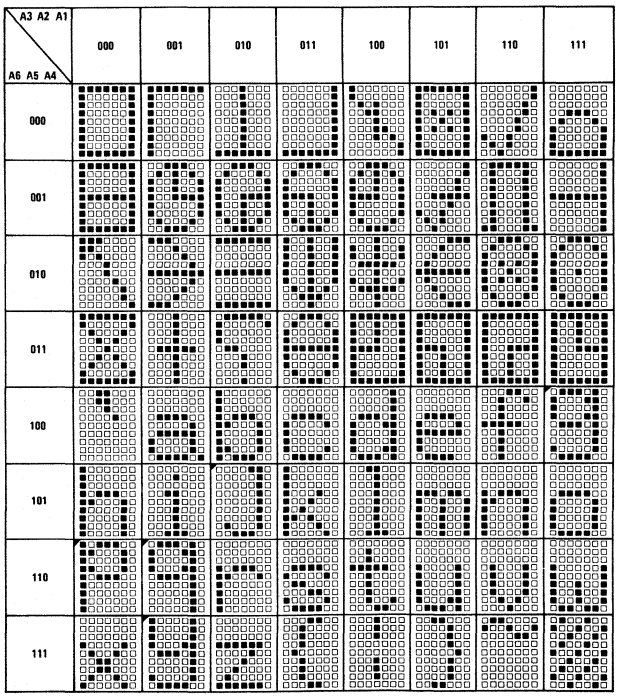


FIGURE 5. DM8678BWF



◤ Shifted characters (see *Figure 12*)

FIGURE 6. DM8678CAE

Note. A "filled in" dot represents a high memory output.

functional description (Continued)

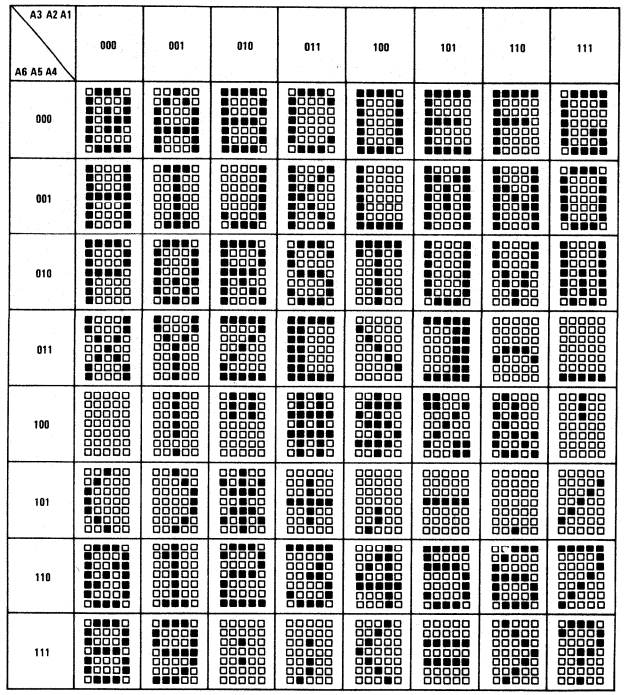
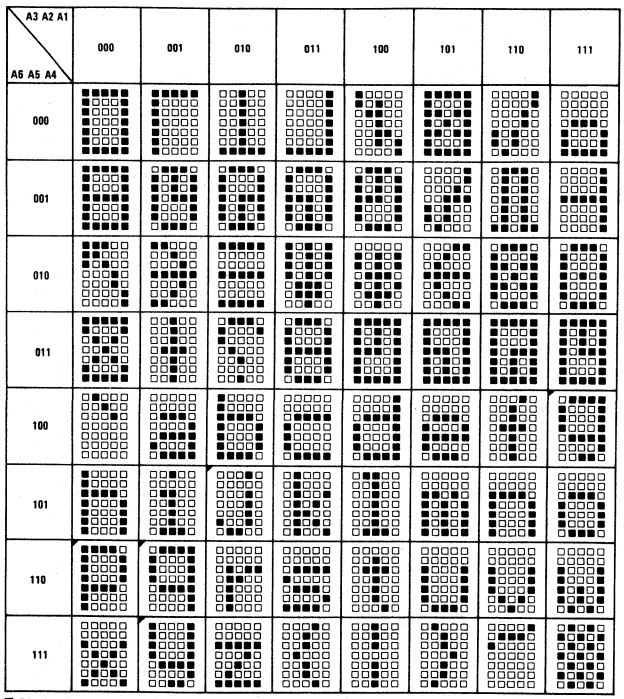


FIGURE 7. DM8767CAB



◤ Shifted characters (see *Figure 13*)

FIGURE 8. DM8678CAH

functional description (Continued)

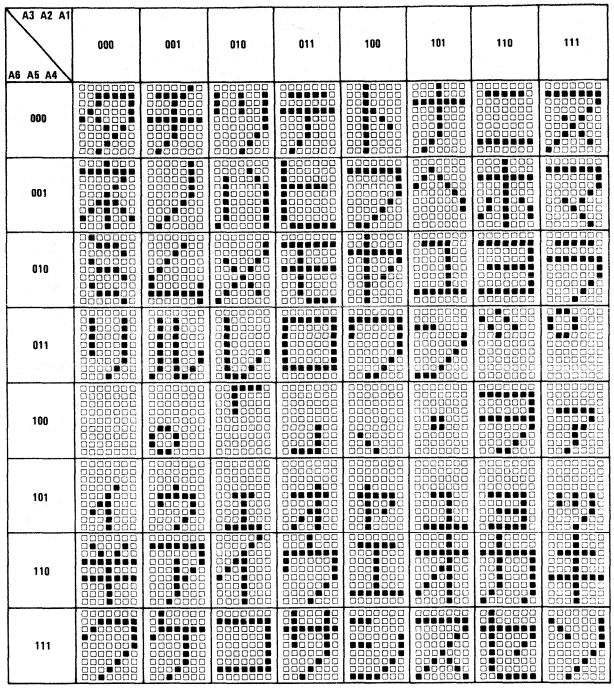


FIGURE 9. DM8678CAD

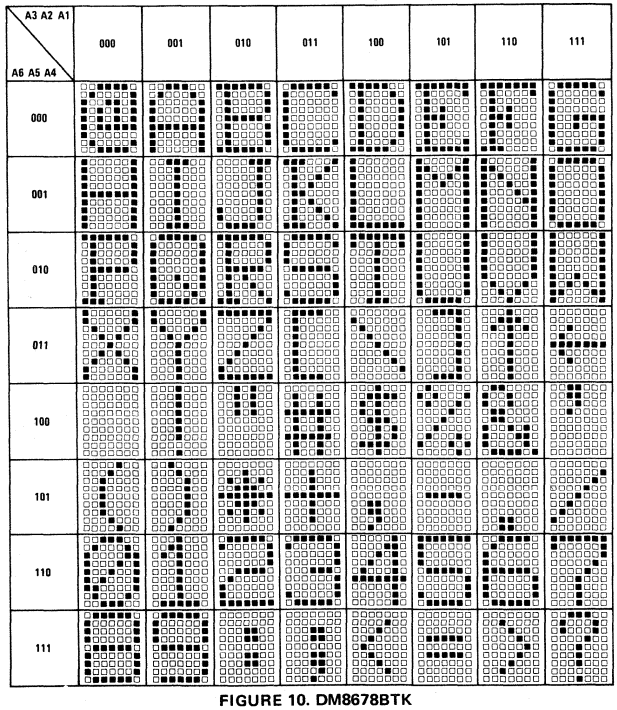


FIGURE 10. DM8678BTK

functional description (Continued)

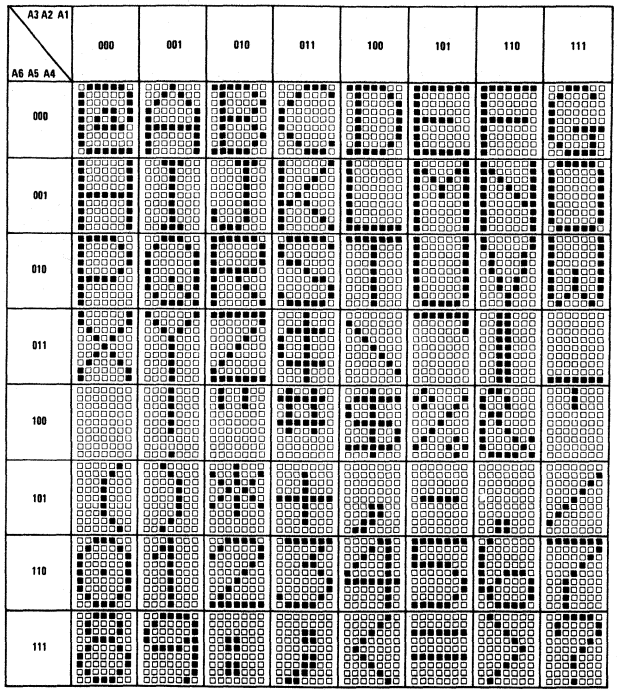


FIGURE 11. DM8678CAS

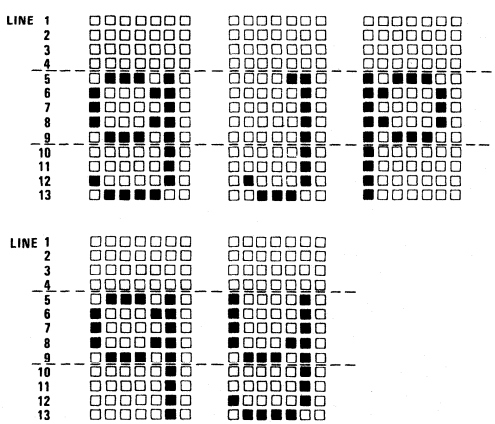
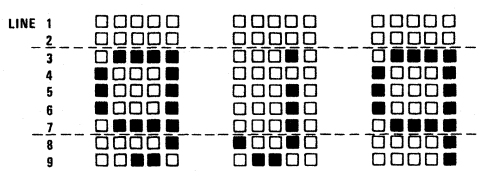


FIGURE 12. Shifted Characters for CAE



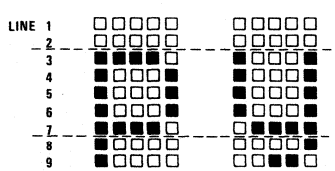


FIGURE 13. Shifted Characters for CAH

ordering information (For special character font for device DM8678).

CUSTOMER CARD INPUT FORMAT

Column 1–3
2-digit character address, from 0–63 preceded by a letter "C".

Column 4
Blank

Column 5–6
1-digit line address, from 0–8, preceded by a letter "L".

Column 7
Blank

Column 8–14
Row data which represents one horizontal row of dots at the specified line address and character address, with first dot at Column 8 and seventh dot at Column 14. Character for TTL high level is 1, for low level is 0.

Column 15
Blank

Column 16
Tag bit–0 for normal character and 1 for shifted character only.

Column 17
Blank

Column 18
Row SUM–Total number of "1's" presents in row data and tag bit expressed in decimal.

"TB" CARD FORMAT (total of eight cards)

Immediately following the data cards, there should be "TB" cards to indicate the column sum.

Column 1–2
The character "TB".

Column 3
1-digit corresponding to Dot number. Use number 8 for tag bit.

Column 4
Blank

Column 5–7
Column SUM–Total number of "1's" in column expressed in decimal.

truth table input format

CHARACTER ADDRESS	LINE ADDRESS	DOT DATA D1, D2, D3, D4, D5, D6, D7	TAG BIT	SUM
0	0			
0	1			
0	2			
0	3			
0	4			
0	5			
0	6			
0	7			
0	8			
1	0			
1	1			
1	2			
1	3			
1	4			
1	5			
1	6			
1	7			
1	8			
2	0			
2	1			
2	2			
2	3			
2	4			
2	5			
2	6			
2	7			
2	8			
.	.			
.	.			
.	.			
.	.			
TB				

Section 10

Code Converters

10

The problem of code conversion is frequently encountered in digital data processing and control equipment design. National's product line includes the converter circuits described in this section. The user should note that converters not included here may be implemented in any one of several ways: custom mask variations of ROMs, specially programmed PROMs or EPROMs, and mask variations of one or more devices in this section. Your National field applications engineer or representative can provide additional assistance.

National Semiconductor

INS8295 NIBL BASIC Interpreter for INS8060

General Description

The INS8295, National's Industrial Basic Language (NIBL) Interpreter, operates with the INS8060 microprocessor (SC/MP family) system to provide a high level, easy to use language for performing control and computation functions in the user's system.

Designed for use in control applications, the NIBL Interpreter enables the user to write and debug programs on-line. The interpreter executes source code directly, thus avoiding the need to translate the source code into machine language. The advantage of this approach is easier source code manipulation (because the source is always available), and instant revision of the program when errors are detected.

The NIBL Interpreter (resident in the INS8295 ROM) executes the user's NIBL source programs from read/write memory or ROM/PROM. The program statements are interpreted and executed line-by-line.

The INS8295 is a programmed version of the INS8332, a 32k mask-programmable ROM organized into 4,096 8-bit words. It provides complete TTL compatibility and uses a single 5V power supply. Two chip selects controlling TRI-STATE™* outputs allow memory expansion.

*A trademark of National Semiconductor Corporation.

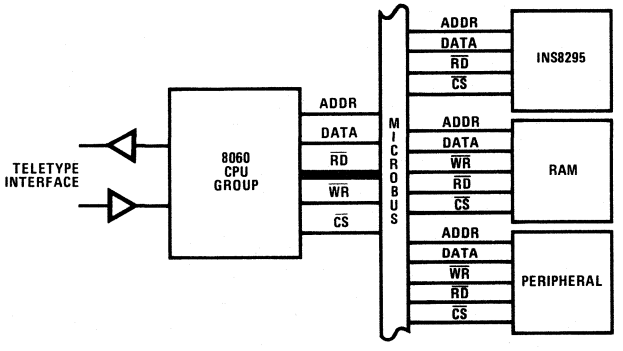
Features

- Reduces software effort in microcomputer applications
- Provides easy source code manipulation and instant program revision
- Allows immediate mode execution of program statements to assist program checkout
- Provides quick sketches of control algorithms
- Facilitates user hardware checkout (faster than assembly language)
- Maximum access time 450 ns
- Industry standard pinouts (2316E)

Applications

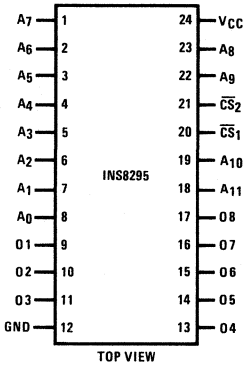
- Instrument Control
- Relay logic replacement
- Testers
- Games

Simple System Diagram



Connection Diagram

Dual In-Line Package



TOP VIEW

Order Number INS8295D
See NS Package D24C

Order Number INS8295N
See NS Package N24B

System Description

The NIBL Basic Interpreter accepts both program statements and control commands. Program statements describe (to the NIBL Interpreter) operations to be performed on program data. A program statement preceded by a line number is inserted into the program for later execution at a spot determined by the line number. If no line number precedes the statement, it is executed immediately and then discarded. This latter mode, known as "immediate" or "direct," is especially valuable during program checkout.

Control commands specify actions that alter the status of the user's program; for example, they direct the execution, saving, and retrieval of programs. Program statements and control commands are summarized in table 1. Table 2 gives the error messages for the Interpreter.

The NIBL Interpreter is located in ROM from X'0 through X'FFF. NIBL assumes that its RAM starts at location X'1000. The memory map is shown in table 3. All Teletype I/O routines used by the INS8295 are located in the top 285 bytes of the ROM address space so that a simple address decoding circuit can allow the substitution of a special user-supplied I/O package, if necessary.

NIBL initializes in a logically clear state, so the first requirement is to supply a program. This is accomplished by typing in numbered lines, by reading in a previously prepared program through the Paper Tape Reader, or by executing out of preprogrammed PROMs in page 2. Execution of programs in pages 3 through 7 is accomplished by the program in page 2 calling pages 3 through 7.

NIBL has very powerful command expressions and functions composed of variable names, relational, arithmetic, and logic operators. NIBL also has easy to use input/output, assignment and control statements.

The Indirect Operator is a NIBL exclusive, at least in the realm of BASIC. It duplicates the functions of PEEK and POKE in other BASICs, but with a less cumbersome syntax. The indirect operator is a way to access absolute memory locations, although its applications are not limited to just accessing absolute memory. In microprocessors such as the INS8060, where interfacing is commonly carried out via memory addressing, its utility is especially significant.

Hardware Configuration

The minimum hardware configuration required to support the NIBL Interpreter is as follows (refer to figure 2):

a. INS8060 (SC/MP) Central Processing Unit (CPU), crystal, and support logic.

b. 110-Baud ASCII terminal interface (20 mA current loop).

c. 2k-by-8 Read/Write Memory (RAM) (X'1000 - X'17FF) for user memory (allows approximately 60 average NIBL line statements).

d. Teletype (TTY) or similar terminal.

e. Power supply (+5 volts).

Users who do not want to build a system from scratch can obtain items a. through c. above already assembled and tested in the form of the SC/MP Low-Cost Development System (ISP-8P/301N) and the 2k-by-8 RAM Card (ISP-8C/002N).

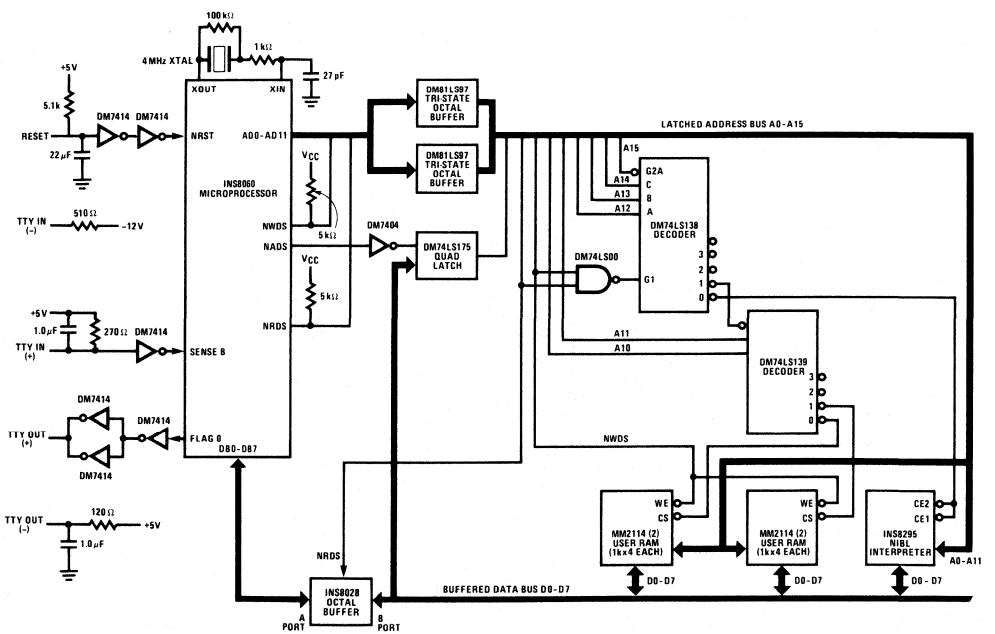


Figure 2. Detailed System Configuration

Table 1. NIBL Statements and Commands

Program Entry

- A line without a number executes immediately.
- A line with a number is inserted in order in the program.
- Line numbers must be from 0 to 32767.
- No blanks in keywords (LET, IF, THEN, GOTO, GOSUB, GO, TO, SUB, RETURN, INPUT, PRINT, LIST, CLEAR, RUN).
- Blanks outside keywords are optional.
- SHIFT/O (Back-arrow) deletes the last character typed.
- CONTROL/H (Backspace) has the same function as SHIFT/O (for use with CRTs).
- CONTROL/U deletes the entire current line.

Program Control

- CLEAR clears all variables (A-Z) and all stacks.
- NEW deletes the program in PAGE 1 (normal page).
- NEW n (n is from 2-7) deletes the program in PAGE n.
- LIST lists the program starting at the lowest line number *or* the line number given.
- RUN starts the program at the lowest line number.

NOTE

Repeated pressing of the BREAK Key interrupts execution and returns the system to programming mode.

Expressions

- All expressions are 16-bit, twos-complement values.
- 26 variable names: A through Z.
- Relational Operators <, >, =, <=, >=, <>.
- Arithmetic Operations +, –, *, /.
- Logical Operators AND, OR, NOT.
- Decimal Constants in the range –32767 to 32767.
- Hexadecimal Constants denoted by '#' followed by hex digits.
- Expressions can be on individual lines or several can be inserted on the same line if they are separated with a colon (i.e., 100 PRINT "HOW MANY";: INPUT X).

Functions

- RND (a, b) returns the random number in the range a through b.
- MOD (a, b) returns the remainder of a/b.
- STAT returns the value of the INS8060 Status Register.
- PAGE returns the number of the current Page.
- TOP returns the highest address of NIBL program in the current Page.

Input/Output Statements

- INPUT X
- INPUT X, Y, Z
- PRINT "A STRING"
- PRINT "F=", M*A
- PRINT "TAKE", X, "PILLS BEFORE";

NOTE

The semicolon suppresses an otherwise automatic carriage return after any PRINT statement.

Assignment Statements

- LET X=7
- E = I * R
- STAT = #70
- PAGE = PAGE + 1
- LET @A = 255
- @ (T+36) = FF
- B = @(TOP+5)

Control Statements

- GO TO 15 or GOTO 15
- GOTO X+5
- GO SUB 100 or GOSUB 100
- RETURN
- IF X+Y>#1A GOTO 15
- IF A=B LET A=B-C
- FOR I = 10 TO 0 STEP –2
- NEXT I
- FOR K = 1 TO 5
- DO: X=X+1: UNTIL (X=10) OR (@X=13)

Indirect Operator

- If the value of V is #2000, then "LET @V = 100" stores 100_{10} at memory location 2000_{16} and "LET W = @V" sets W to the contents of the location specified by V.

NOTE

The values that can be stored at any one specified memory location range from 0 to 255_{10}.

String Handling

- $T = "THIS IS A STRING"
- PRINT $T, $ (TOP+72)
- INPUT $ (U+20)
- $U = $(TOP + 2*36)

Additional Statements

- LINK <address> causes control to be transferred to the SC/MP Machine Language Routine starting at <address>, which is a decimal number.
- REM – this Statement is used to insert comments into NIBL programs.
- END – this statement is useful for inserting breakpoints into a NIBL program while it is being debugged. When NIBL encounters an END statement, it prints a break message and the current line number, and returns to edit mode.

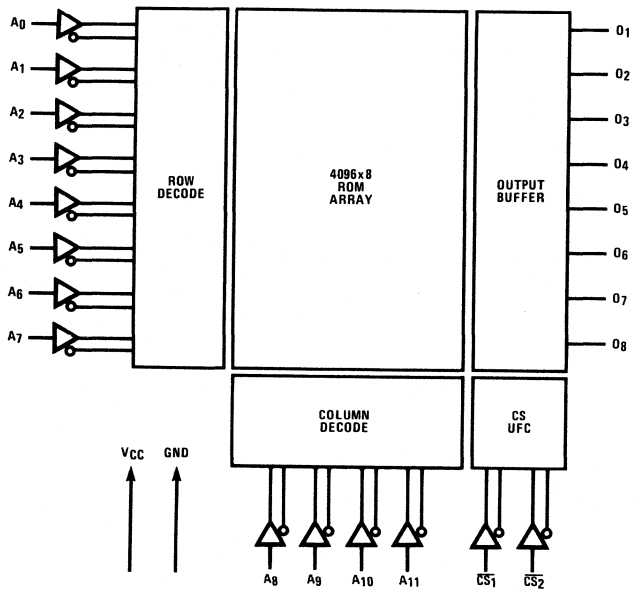
Table 2. NIBL Interpreter Error Messages

Message	Description
CHAR	Character after logical end of statement
DIV0	Division by zero
END"	No ending quote on string
FOR	FOR without NEXT
NEST	Nesting limit exceeded in expression, FORs, GOSUBs, etc.
NEXT	NEXT without FOR
NOGO	No line number corresponding to GOTO or GOSUB
RTRN	RETURN without previous GOSUB
SNTX	Syntax error
STMT	Statement type used improperly
UNTL	UNTIL without DO
VALU	Constant format or value error
AREA	No more room left in current page for program

Table 3. NIBL Memory Map

ROM Address (hex)	Function
0-FFF	NIBL Interpreter
F77-FFF	I/O routines (get character F77) (put character FC2)
2000 upwards	A ROM program stored within this space will be executed upon system initialization.
RAM Address (hex)	**Function**
1000-111D	NIBL RAM scratch area (buffers, variables, etc.)
111E upwards	NIBL user program space

Block Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ± 5%, unless otherwise specified.)

	Parameter (Note 3)	Conditions	Min	Typ (Note 4)	Max	Units
I_I	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2			V
V_{IL}	Logical "0" Input Voltage				0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−20	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Outputs Open		100	130	mA

Capacitance

	Parameter (Note 3)	Conditions	Min	Typ (Note 4)	Max	Units
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ± 5%, unless otherwise specified.) See AC test circuit and switching time waveforms.

	Parameter (Note 3)	Conditions	Min	Typ (Note 4)	Max	Units
t_{AC}	Chip Select Access Time	See AC Load Circuit All Times (except t_{OFF})			150	ns
t_{OFF}	Output Turn OFF Delay	Measured to 1.5V Level with t_r and t_f of Input < 20 ns (figures 3 and 4)			150	ns
t_A	Address Access Time	t_{OFF} TRI-STATE Output Level Measured to Less than ±20μA Output Current			450	ns

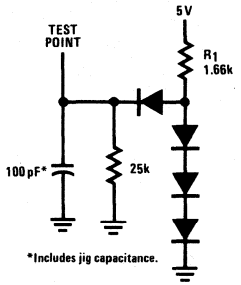
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



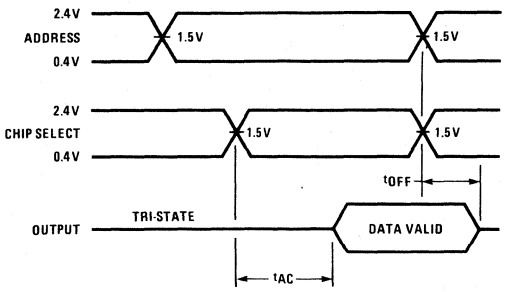


Figure 3. Address Preceeds Chip Select

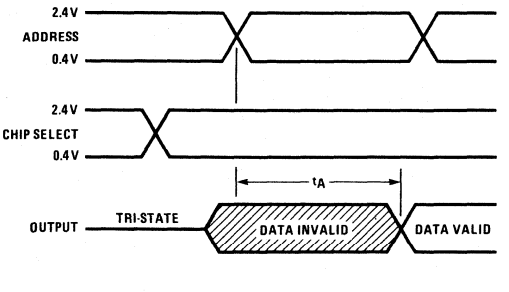


Figure 4. Address Follows Chip Select

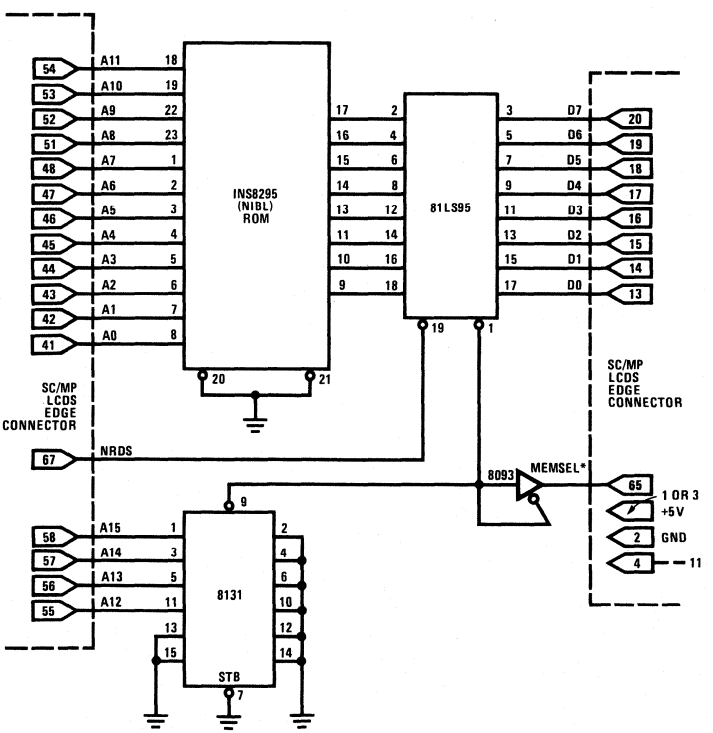


Figure 5. LCDS Interconnect for the INS8295 NIBL ROM (should be used with a RAM card addressed at 1000_{HEX})

Typical Applications

The application example below shows a 6-inch butterfly valve driven under program control in one of two modes: *direct position* or *oscillate*. In the direct-position mode, the operator enters a digit (0 through 10) via a CRT terminal keyboard. The value of the digit corresponds to a particular valve position — the closed position through the wide-open position in 10% increments. The valve is positioned in accordance with the entered value by the INS8060 through a digital-to-analog converter. In the oscillate mode, the operator enters two *limit* values. The valve is driven back and forth continuously between positions represented by the two limits entered until a new command is entered. An example of an interface circuit for valve control is shown in figure 6.

Figure 7 shows the NIBL program listing for this example. Since there is no position feedback in this example, the program has a delay loop that allows time for the valve to be driven between the limits entered.

One INS8060 could easily control a dozen of these valves in an actual application that included valve-position and fluid-flow feedback (via a pressure transducer).

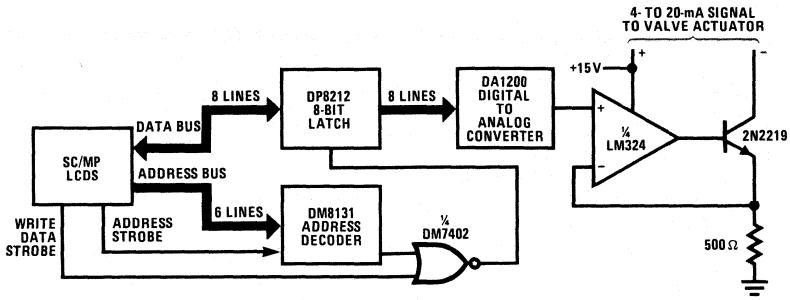


Figure 6. Interface Circuit for Valve Control

```
5 LET V=-32735
10 LET K=28702
15 PRINT "ENTER UPPER LIMIT (1=10%, 2=20%, ETC. . . ). "
20 INPUT U
25 IF U>10 THEN GOTO 300
30 PRINT "ENTER LOWER LIMIT (1=10%, 2=20%, ETC. . . ). "
35 INPUT L
40 IF L>10 THEN GOTO 310
45 IF U<L THEN GOTO 65
50 LET B=U
55 LET U=L
60 LET L=B
65 LET R=(U-L)*13
70 LET U=(((U-9)*(-1))+1)*20
75 LET L=(((L-9)*(-1))+1)*20
80 LET @V=U
85 GOSUB 500
90 IF F=1 THEN GOTO 200
95 LET @V=L
100 GOSUB 500
105 IF F=1 THEN GOTO 200
110 GOTO 80
200 PRINT "WHAT VALUE OF VALVE OPENING DO YOU WANT?"
205 PRINT "0=FULL CLOSE, 1=10%, 2=20%, . . . 9=90%, 10=FULL OPEN. "
210 INPUT S
212 IF S>10 THEN GOTO 320
215 IF S=0 THEN GOTO 280
220 IF S=10 THEN GOTO 290
225 LET S=(((S-9)*(-1))+1)*20
230 LET @V=S
235 PRINT "WAIT FOR VALVE TO REACH DESIRED SETTING. "
240 PRINT "DO YOU WANT ANOTHER SETTING (1=YES, 0=NO)?"
245 INPUT T
250 IF T=0 THEN GOTO 265
255 PRINT "ENTER NEW SETTING. "
260 GOTO 210
265 PRINT "DO YOU WANT NEW LIMITS (1=YES, 0=NO)?"
270 INPUT T
275 IF T=0 THEN GOTO 80
277 GOTO 15
280 LET @V=206
285 GOTO 235
290 LET @V=6
295 GOTO 235
300 PRINT "ERROR"
305 GOTO 15
310 PRINT "ERROR"
315 GOTO 30
320 PRINT "ERROR"
325 GOTO 255
500 LET A=R
505 IF F=1 THEN F=0
510 IF @K <> 240 THEN GOTO 530
515 LET A=A-1
520 IF A>0 THEN GOTO 510
525 RETURN
530 LET F=1
535 RETURN
```

Figure 7. NIBL Program Listing

National Semiconductor

INS8298, INS8298E 8080A LLL BASIC Interpreter

General Description

The INS8298/INS8298E is a 65k MAXI-ROM™*, organized into 8192 8-bit words, that is preprogrammed with the 8080A Lawrence Livermore Laboratory (LLL) BASIC Interpreter. Unprogrammed versions of the INS8298 and INS8298E are the MM5235 (28 pin, 800 ns access) and INS8364E/MM52164 (24 pin, 450 ns access), respectively. Both the INS8298 and INS8298E provide complete TTL compatibility and single 5V power supply. Three chip selects controlling TRI-STATE™* outputs allow for memory expansion.

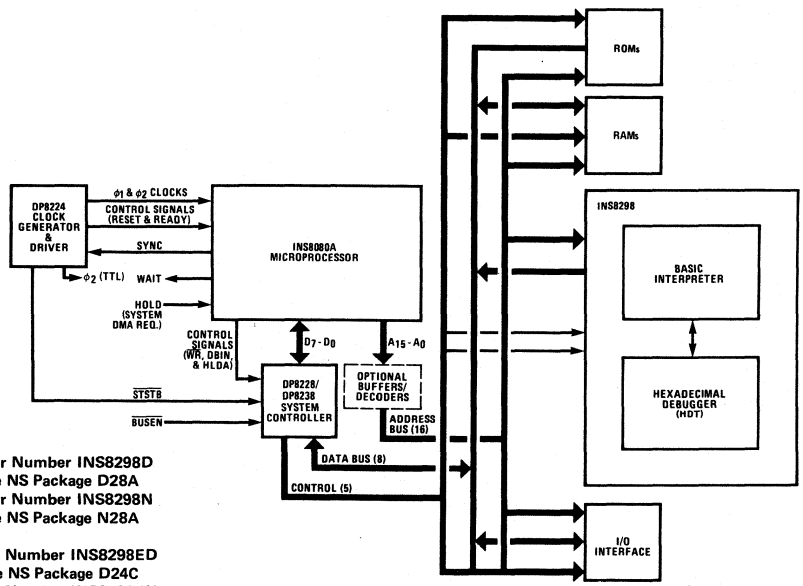
The 8080A LLL BASIC Interpreter operates with the INS8080A microprocessor system to provide a high-level, easy-to-use language for performing both control and computation functions in the INS8080A. Designed for use in data acquisition and control applications, the LLL BASIC Interpreter enables the user to write and debug a program on-line. The interpreter executes source code statements directly, thus avoiding the need to translate into machine language. This approach has the advantage of easier source code manipulation (because the source is always available), and instant revision of the program when errors are detected.

Features

- Reduces software effort in microcomputer applications
- Provides easy source code manipulation and instant program revision
- Allows immediate-mode execution of program statements to assist program checkout
- Includes floating-point arithmetic package to provide full computational capability
- Readily adaptable to user-supplied I/O routines
- Allows calls to high-speed, machine-language subroutines
- Allows use of indestructible hexadecimal debugging package
- Available as INS8298 (28 pin, 800 ns access) and INS8298E (24 pin, 450 ns access)
- MICROBUS™* compatible

*A trademark of National Semiconductor Corporation.

General System Configuration



Order Number INS8298D
See NS Package D28A
Order Number INS8298N
See NS Package N28A

Order Number INS8298ED
See NS Package D24C
Order Number INS8298EN
See NS Package N24A

The LLL BASIC Interpreter is used to translate, debug, and execute user-written ASCII programs in read/write memory (RAM). Each statement is interpreted from its ASCII BASIC format, and then executed line-by-line. An LLL BASIC Compiler, written in FORTRAN, will soon be available in the public domain.* (See figure 1.)

The BASIC Interpreter accepts both program statements and control commands. Program statements describe (to the BASIC Interpreter) operations to be performed on program data. A program statement preceded by a line number is inserted into the program for later execution at a spot determined by the line number. If no line number precedes the statement, it is executed immediately and then discarded. This latter mode, known as "immediate" or "direct," is especially valuable during program checkout. Control commands specify actions that alter the status of the user's program; for example, they direct the execution, saving, and retrieval of programs. Program statements are summarized in table 1; control commands are summarized in table 2.

The BASIC Interpreter is located in ROM from 1000_{16} through $2FFF_{16}$. BASIC assumes that its RAM starts at location $3D00_{16}$. The memory map is shown in table 3. All I/O routines used by the INS8298 are located in the upper 256 bytes of the address space so that a simple address decoding circuit can allow the substitution of a special user-supplied I/O package, if necessary. As an alternative scheme for allowing the user to tailor I/O to his own needs, entry points to the interpreter are provided that allow the page zero initialization program to channel all BASIC I/O through its own routines.

A hexadecimal debugging routine (HDT) is also available on the INS8298 ROM. HDT allows the user to examine internal registers and memory locations and modify their contents. HDT is called from the BASIC Interpreter to help debug user-developed software. Input and output data representation is in hexadecimal format. In addition to the usual debugging capabilities, HDT also has commands to perform the following functions:

- Test a specified range of memory locations
- Load programs in hexadecimal, NSC, and LLL binary formats
- Save the contents of a specified range of memory locations

In addition to the features summarized previously, LLL BASIC has many capabilities found in other standard BASIC systems (see tables 1 and 2). However, LLL BASIC does not include built-in operations as intrinsic functions, e.g., trigonometric or string-manipulation functions. Also, LLL BASIC does not permit arbitrary arithmetic expressions beyond those of the form:

variable op variable

where the first variable in the expression may be preceded by a minus (–); op may be a plus (+), minus (–), asterisk (*) for multiplication, or slash (/) for division; and either variable can be an identifier, function, or number.

*For additional information, contact:

Argonne Code Center
Argonne National Laboratory
9700 South Cass Avenue
Argonne, Illinois 60439

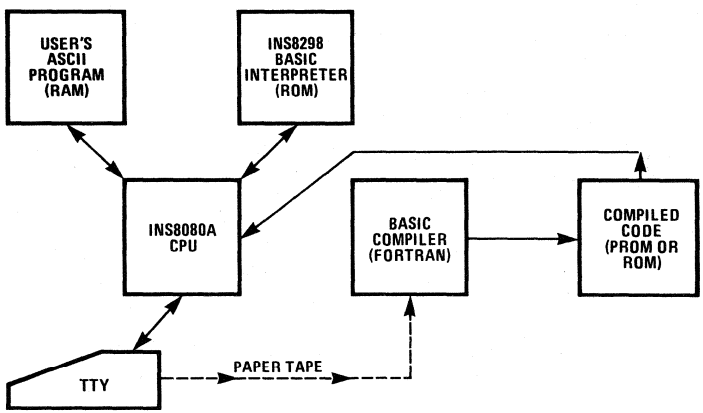


Figure 1. Operation of the LLL BASIC Interpreter and Compiler with the INS8080A

Table 1. BASIC Statements

Statement	Function
CALL	Calls user-written assembly-language routines.
DIM	Declares a one-dimensional array. (Indexing is from zero.)
END	Terminates a program and returns control to BASIC.
FOR	Causes program to iterate through a loop a designated number of times.
GET expression	Reads input data from a specified port.
GOSUB nn	Transfers control to a subroutine beginning at line nn.
GOTO nn	Transfers control to line nn.
IF expression THEN nn	Transfers to line nn if the condition of the expression is met.
INPUT list	Allows the user to supply numeric data to a program directly from the terminal.
LET identifier = expression	Assigns the value of an expression to the identifier on the left side of the equal sign.
NEXT	Signals the end of a loop.
PRINT	Allows numeric data and character strings to be printed on the terminal.
PUT expression	Writes output data to a specified port.
REM	Allows comments to be inserted in the program listing.
RETURN	Returns control to the line after the last GOSUB.
STOP	Suspends program execution and returns.

Table 2. BASIC Commands

Command	Function
CONTROL/H (backspace)	Deletes the previous character typed during input.
CONTROL/S	Interrupts program during execution and returns to immediate mode.
DEBUG	Transfers control to the Hexadecimal Debugger program (HDT).
LIST	Prints out all or part of a program at the terminal.
PACK	Frees memory locations in RAM to allow the user more working space.
PLIST	Punches paper-tape copy of a program.
PTAPE	Reads in paper-tape copy of program using high-speed reader.
RUN	Begins execution of the program currently in memory.
SCR	Erases the program in memory

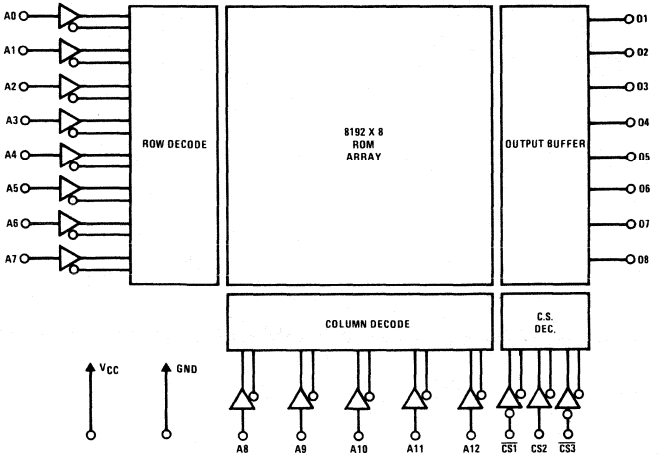
Table 3. Memory Map for BASIC Interpreter

ROM Address (hex)	Function
1000 - 1008	BASIC entry points for initialization.
1009 - 27FF	BASIC Interpreter.
2800 - 2EFF	Hexadecimal Debugger (HDT) and loaders.
2F00 - 2FFF	System I/O routines for INS8251 USART (ports EC and ED).

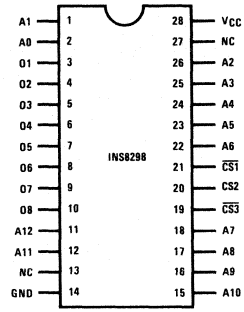
RAM Address (hex)	Function
3D00 - 3DFF	BASIC RAM scratch area (buffers, variables, etc.).
3E00 upward	BASIC user program space.
Top of RAM downward	BASIC stack area.

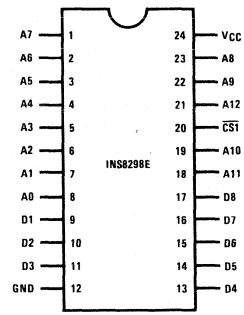
Chip Selects	
$\overline{CS1}$	Active low (0).
CS2	Active high (1).
$\overline{CS3}$	Active low (0).

Block and Connection Diagrams (Dual-In-Line Packages, Top Views)



NOTE: CS2 AND $\overline{CS3}$ NOT AVAILABLE IN INS8298E.





Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1 W
Lead Temperature (Soldering, 10 seconds)	+300°C

Chip Selects

CS No.	Pin No.	Active Level
INS8298		
1	21	0
2	20	1
3	19	0
INS8298E		
1	20	0

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = +5V ± 5%, unless otherwise specified.) See AC test circuit and switching time waveforms.

	Parameter (Note 3)	Conditions	Min.	Typ. (Note 4)	Max.	Units
I_{LI}	Input Current	V_{IN} = 0V to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2.2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		-0.5		0.6	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			-20	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		100	130	mA

Capacitance

Parameter (Note 3)		Conditions	Min.	Typ. (Note 4)	Max.	Units
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = +5V ± 5%, unless otherwise specified.) See AC test circuit and switching time waveforms.

Parameter (Note 3)		Conditions	Limits						Units
			INS8298			INS8298E			
			Min.	Typ. (Note 4)	Max.	Min.	Typ. (Note 4)	Max.	
t_A	Address Access Time	See AC Load Circuit. All times except t_{OFF} measured to 1.5V level with t_r and t_f of input < 20 ns (figures 2 & 3), t_{OFF} TRI-STATE output level measured to less than ±20 μA output current.		450	800			450	ns
t_{AC}	Chip Select Access Time			150	250			150	ns
t_{OFF}	Output Turn OFF Delay			150	250			150	ns
t_C	Cycle Time		800	450					ns
t_{AS}	Address Set-Up Time Referenced to Chip Select		550						ns

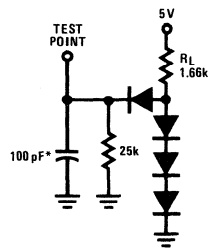
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



*INCLUDES JIG CAPACITANCE.

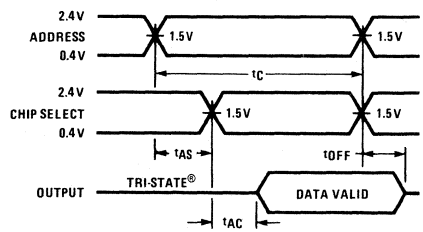


Figure 2. Address Precedes Chip Select

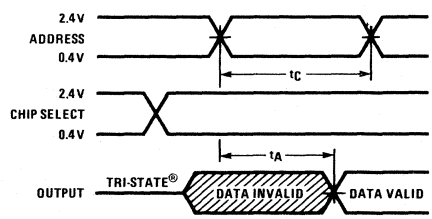


Figure 3. Address Follows Chip Select

National Semiconductor

MM4220AE/MM5220AE
ASCII-7-to-Hollerith Code Converter

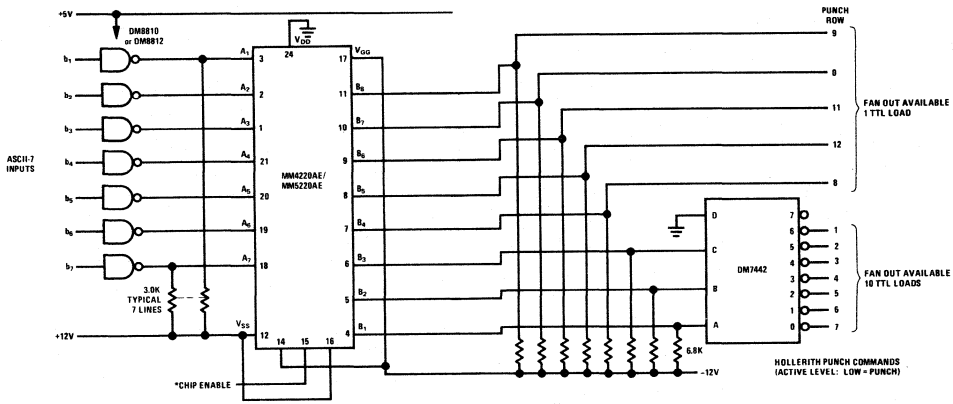
general description

The MM4220AE/MM5220AE 1024-bit read-only memory has been programmed to convert the 128 entries of the American Standard Code for Information Interchange in seven bits (ASCII-7) to Hollerith code (compressed to eight bits). The conversion performed follows the recommendation of American National Standard ANSI x 3.26–1970, Hollerith punched card code.

The typical application shows a recommended circuit for re-expansion of the Hollerith code to twelve lines.

For electrical, environmental and mechanical details, refer to the MM4220/MM5220 data sheet.

typical applications



*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

Order Number MM4220AE/J or MM5220AE/J
See NS Package J24A

Order Number MM5220AE/N
See NS Package N24B

code conversion tables

b_4 b_3 b_2 b_1	ROW \ COL	b_7 0 b_6 0 b_5 0 — 0	0 0 1 — 1	0 1 0 — 2	0 1 1 — 3	1 0 0 — 4	1 0 1 — 5	1 1 0 — 6	1 1 1 — 7
0000	0	NUL 12-0-9-8-1	DLE 12-11-9-8-1	SP NO PCH	0 0	@ 8-4	P 11-7	` 8-1	p 12-11-7
0001	1	SCH 12-9-1	DC1 11-9-1	! ① 12-8-7	1 1	A 12-1	Q 11-8	a 12-0-1	q 12-11-8
0010	2	STX 12-9-2	DC2 11-9-2	" 8-7	2 2	B 12-2	R 11-9	b 12-0-2	r 12-11-9
0011	3	ETX 12-9-3	DC3 11-9-3	# 8-3	3 3	C 12-3	S 0-2	c 12-0-3	s 11-0-2
0100	4	ECT 9-7	DC4 9-8-4	$ 11-8-3	4 4	D 12-4	T 0-3	d 12-0-4	t 11-0-3
0101	5	ENQ 0-9-8-5	NAK 9-8-5	% 0-8-4	5 5	E 12-5	U 0-4	e 12-0-5	u 11-0-4
0110	6	ACK 0-9-8-6	SYN 9-2	& 12	6 6	F 12-6	V 0-5	f 12-0-6	v 11-0-5
0111	7	BEL 0-9-8-7	ETB 0-9-6	' 8-5	7 7	G 12-7	W 0-6	g 12-0-7	w 11-0-6
1000	8	BS 11-9-6	CAN 11-9-8	(12-8-5	8 8	H 12-8	X 0-7	h 12-0-8	x 11-0-7
1001	9	HT 12-9-5	EM 11-9-8-1	) 11-8-5	9 9	I 12-9	Y 0-8	i 12-0-9	y 11-0-8
1010	10	IF 0-9-5	SUB 9-8-7	* 11-8-4	: 8-2	J 11-1	Z 0-9	j 12-11-1	z 11-0-9
1011	11	VT 12-9-8-3	ESC 0-9-7	+ 12-8-6	; 11-8-6	K 11-2	[12-8-2	k 12-11-2	{ 12-0
1100	12	FF 12-9-8-4	FS 11-9-8-4	, 0-8-3	< 12-8-4	L 11-3	\ 0-8-2	l 12-11-3	¦ 12-11
1101	13	CR 12-9-8-5	GS 11-9-8-5	– 11	= 8-6	M 11-4	] 11-8-2	m 12-11-4	} 11-0
1110	14	SO 12-9-8-6	RS 11-9-8-6	. 12-8-3	> 0-8-6	N 11-5	∧ ② 11-8-7	n 12-11-5	~ 11-0-1
1111	15	SI 12-9-8-7	US 11-9-8-7	/ 0-1	? 0-8-7	O 11-6	– 0-8-5	o 12-11-6	DEL 12-9-7

① may be "|"

② may be "¬"

③ The top line in each entry to the table represents an assigned character (Columns 0 to 7).
The bottom line in each entry is the corresponding card hole-pattern.

code conversion tables(con't)

ADDRESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
0	1	1	0	1	1	0	0	1
1	1	0	0	1	0	0	0	1
2	1	0	0	1	0	0	1	0
3	1	0	0	1	0	0	1	1
4	1	0	0	0	0	1	1	1
5	1	1	0	0	1	1	0	1
6	1	1	0	0	1	1	1	0
7	1	1	0	0	1	1	1	1
8	1	0	1	0	0	1	1	0
9	1	0	0	1	0	1	0	1
10	1	1	0	0	0	1	0	1
11	1	0	0	1	1	0	1	1
12	1	0	0	1	1	1	0	0
13	1	0	0	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	1	1	1	1	1
16	1	0	1	1	1	0	0	1
17	1	0	1	0	0	0	0	1
18	1	0	1	0	0	0	1	0
19	1	0	1	0	0	0	1	1
20	1	0	0	0	1	1	0	0
21	1	0	0	0	1	1	0	1
22	1	0	0	0	0	0	1	0
23	1	1	0	0	0	1	1	0
24	1	0	1	0	1	0	0	0
25	1	0	1	0	1	0	0	1
26	1	0	0	0	1	1	1	1
27	1	1	0	0	0	1	1	1
28	1	0	1	0	1	1	0	0
29	1	0	1	0	1	1	0	1
30	1	0	1	0	1	1	1	0
31	1	0	1	0	1	1	1	1
32	0	0	0	0	0	0	0	0
33	0	0	0	1	1	1	1	1
34	0	0	0	0	1	1	1	1
35	0	0	0	0	1	0	1	1
36	0	0	1	0	1	0	1	1
37	0	1	0	0	1	1	0	0
38	0	0	0	1	0	0	0	0
39	0	0	0	0	1	1	0	1
40	0	0	0	1	1	1	0	1
41	0	0	1	0	1	1	0	1
42	0	0	1	0	1	1	0	0
ROW	9	0	11	12	8	4	2	1

ADDRESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
43	0	0	0	1	1	1	1	0
44	0	1	0	0	1	0	1	1
45	0	0	1	0	0	0	0	0
46	0	0	0	1	1	0	1	1
47	0	1	0	0	0	0	0	1
48	0	1	0	0	0	0	0	0
49	0	0	0	0	0	0	0	1
50	0	0	0	0	0	0	1	0
51	0	0	0	0	0	0	1	1
52	0	0	0	0	0	1	0	0
53	0	0	0	0	0	1	0	1
54	0	0	0	0	0	1	1	0
55	0	0	0	0	0	1	1	1
56	0	0	0	0	1	0	0	0
57	1	0	0	0	0	0	0	0
58	0	0	0	0	1	0	1	0
59	0	0	1	0	1	1	1	0
60	0	0	0	1	1	1	0	0
61	0	0	0	0	1	1	1	0
62	0	1	0	0	1	1	1	0
63	0	1	0	0	1	1	1	1
64	0	0	0	0	1	1	0	0
65	0	0	0	1	0	0	0	1
66	0	0	0	1	0	0	1	0
67	0	0	0	1	0	0	1	1
68	0	0	0	1	0	1	0	0
69	0	0	0	1	0	1	0	1
70	0	0	0	1	0	1	1	0
71	0	0	0	1	0	1	1	1
72	0	0	0	1	1	0	0	0
73	1	0	0	1	0	0	0	0
74	0	0	1	0	0	0	0	1
75	0	0	1	0	0	0	1	0
76	0	0	1	0	0	0	1	1
77	0	0	1	0	0	1	0	0
78	0	0	1	0	0	1	0	1
79	0	0	1	0	0	1	1	0
80	0	0	1	0	0	1	1	1
81	0	0	1	0	1	0	0	0
82	1	0	1	0	0	0	0	0
83	0	1	0	0	0	0	1	0
84	0	1	0	0	0	0	1	1
85	0	1	0	0	0	1	0	0
ROW	9	0	11	12	8	4	2	1

ADDRESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
86	0	1	0	0	0	1	0	1
87	0	1	0	0	0	1	1	0
88	0	1	0	0	0	1	1	1
89	0	1	0	0	1	0	0	0
90	1	1	0	0	0	0	0	0
91	0	0	0	1	1	0	1	0
92	0	1	0	0	1	0	1	0
93	0	0	1	0	1	0	1	0
94	0	0	1	0	1	1	1	1
95	0	1	0	0	1	1	0	1
96	0	0	0	0	1	0	0	1
97	0	1	0	1	0	0	0	1
98	0	1	0	1	0	0	1	0
99	0	1	0	1	0	0	1	1
100	0	1	0	1	0	1	0	0
101	0	1	0	1	0	1	0	1
102	0	1	0	1	0	1	1	0
103	0	1	0	1	0	1	1	1
104	0	1	0	1	1	0	0	0
105	1	1	0	1	0	0	0	0
106	0	0	1	1	0	0	0	1
107	0	0	1	1	0	0	1	0
108	0	0	1	1	0	0	1	1
109	0	0	1	1	0	1	0	0
110	0	0	1	1	0	1	0	1
111	0	0	1	1	0	1	1	0
112	0	0	1	1	0	1	1	1
113	0	0	1	1	1	0	0	0
114	1	0	1	1	0	0	0	0
115	0	1	1	0	0	0	1	0
116	0	1	1	0	0	0	1	1
117	0	1	1	0	0	1	0	0
118	0	1	1	0	0	1	0	1
119	0	1	1	0	0	1	1	0
120	0	1	1	0	0	1	1	1
121	0	1	1	0	1	0	0	0
122	1	1	1	0	0	0	0	0
123	0	1	0	1	0	0	0	0
124	0	0	1	1	0	0	0	0
125	0	1	1	0	0	0	0	0
126	0	1	1	0	0	0	0	1
127	1	0	0	1	0	1	1	1
ROW	9	0	11	12	8	4	2	1

National Semiconductor

MM4220AP/MM5220AP BCDIC-to-ASCII Code Converter

general description

The MM4220AP/MM5220AP is used for the conversion of the Binary Coded Decimal Interchange Code(BCDIC) to the American Standard Code for Information Interchange (ASCII).

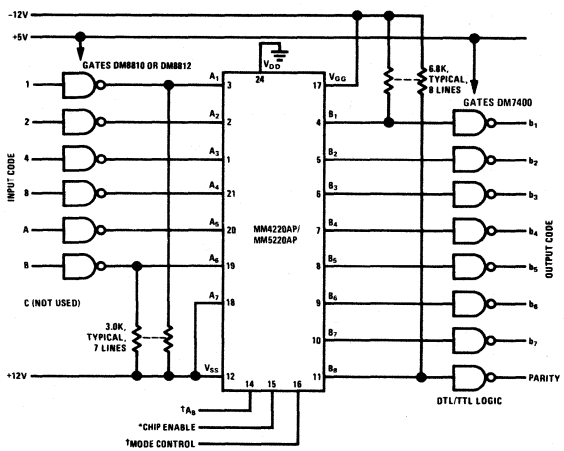
The input is a seven-bit BCDIC code with the exception of the parity (check) bit (pin 18) which is returned to +12V dc. The alternate set of input symbols is also shown in the Conversion Table for reference.

The output is a seven-bit ASCII code, with an eighth bit generated for even parity.

device characteristics

For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

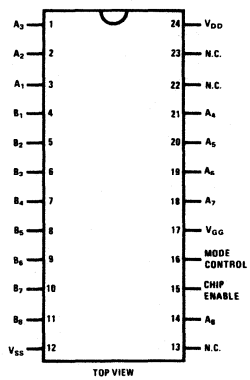
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4220AP/J or MM5220AP/J
See NS Package J24A

Order Number MM5220AP/N
See NS Package N24B

code conversion table

ROM ADDRESS	FUNCTION INPUT BCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT CODE	BCDIC B	A	8	4	2	1	CODE OUTPUT EP	ASCII b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	Space	Space	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1
2	2	2	0	0	0	0	0	1	0	1	0	1	1	0	0	1	0
3	3	3	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
4	4	4	0	0	0	0	1	0	0	1	0	1	1	0	1	0	0
5	5	5	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1
6	6	6	0	0	0	0	1	1	0	0	0	1	1	0	1	1	0
7	7	7	0	0	0	0	1	1	1	1	0	1	1	0	1	1	1
8	8	8	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
9	9	9	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1
10	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	0
11	≠ or =	≠	0	0	0	1	0	1	1	1	0	1	0	0	0	1	1
12	@ or '	@	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0
13	:	:	0	0	0	1	1	0	1	0	0	1	1	1	0	1	0
14	>	>	0	0	0	1	1	1	0	1	0	1	1	1	1	1	0
15	√	?	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1
16	Blank	¦	0	0	1	0	0	0	0	1	1	0	1	1	0	1	1
17	/	/	0	0	1	0	0	0	1	1	0	1	0	1	1	1	1
18	S	S	0	0	1	0	0	1	0	0	1	0	1	0	0	1	1
19	T	T	0	0	1	0	0	1	1	1	1	0	1	0	1	0	0
20	U	U	0	0	1	0	1	0	0	0	1	0	1	0	1	0	1
21	V	V	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0
22	W	W	0	0	1	0	1	1	0	1	1	0	1	0	1	1	1
23	X	X	0	0	1	0	1	1	1	1	1	0	1	1	0	0	0
24	Y	Y	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1
25	Z	Z	0	0	1	1	0	0	1	0	1	0	1	1	0	1	0
26	‡	LF	0	0	1	1	0	1	0	0	0	0	0	1	0	1	0
27	.	.	0	0	1	1	0	1	1	1	0	1	0	1	1	0	0
28	% or (	%	0	0	1	1	1	0	0	1	0	1	0	0	1	0	1
29	∨	HT	0	0	1	1	1	0	1	0	0	0	0	1	0	0	1
30	\	'	0	0	1	1	1	1	0	0	0	1	0	0	1	1	1
31	⌗	"	0	0	1	1	1	1	1	0	0	1	0	0	0	1	0
32	–	–	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1
33	J	J	0	1	0	0	0	0	1	1	1	0	0	1	0	1	0
34	K	K	0	1	0	0	0	1	0	0	1	0	0	1	0	1	1
35	L	L	0	1	0	0	0	1	1	1	1	0	0	1	1	0	0
36	M	M	0	1	0	0	1	0	0	0	1	0	0	1	1	0	1
37	N	N	0	1	0	0	1	0	1	0	1	0	0	1	1	1	0
38	O	O	0	1	0	0	1	1	0	1	1	0	0	1	1	1	1
39	P	P	0	1	0	0	1	1	1	0	1	0	1	0	0	0	0
40	Q	Q	0	1	0	1	0	0	0	1	1	0	1	0	0	0	1
41	R	R	0	1	0	1	0	0	1	1	1	0	1	0	0	1	0
42	!	!	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1
43	$	$	0	1	0	1	0	1	1	0	0	1	0	0	1	0	0
44	*	*	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
45	]	)	0	1	0	1	1	0	1	1	0	1	0	1	0	0	1
46	;	;	0	1	0	1	1	1	0	1	0	1	1	1	0	1	1
47	Δ	[	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1
48	& or +	&	0	1	1	0	0	0	0	1	0	1	0	0	1	1	0
49	A	A	0	1	1	0	0	0	1	0	1	0	0	0	0	0	1
50	B	B	0	1	1	0	0	1	0	0	1	0	0	0	0	1	0
51	C	C	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
52	D	D	0	1	1	0	1	0	0	0	1	0	0	0	1	0	0
53	E	E	0	1	1	0	1	0	1	1	1	0	0	0	1	0	1
54	F	F	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0
55	G	G	0	1	1	0	1	1	1	0	1	0	0	0	1	1	1
56	H	H	0	1	1	1	0	0	0	0	1	0	0	1	0	0	0
57	I	I	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1
58	?	+	0	1	1	1	0	1	0	0	0	1	0	1	0	1	1
59	.	.	0	1	1	1	0	1	1	0	0	1	0	1	1	1	0
60	¤ or)	⌒	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0
61	[	(	0	1	1	1	1	0	1	0	0	1	0	1	0	0	0
62	<	<	0	1	1	1	1	1	0	0	0	1	1	1	1	0	0
63	‡	CR	0	1	1	1	1	1	1	1	0	0	0	1	1	0	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

National Semiconductor

MM4220BL/MM5220BL Baudot-to-ASCII Code Converter

general description

The MM4220BL/MM5220BL is used for conversion of the Communications Set Baudot code to the American Standard Code for Information Interchange (ASCII).

The Baudot and ASCII codes have different formats. ASCII has a unique code combination for each alphabetic, numerical, or control character. The correct interpretation of a five bit Baudot is dependent upon knowing its previous history; whether upper or lower case was *last* selected. In effect a sixth-bit, which can be called the Case Bit, is required to uniquely identify the Baudot input. The latch circuit shown in the typical application can store this information and will generate the Case Bit. If the bit is externally supplied, the feedback and latch circuits can be deleted (as shown with the X's).

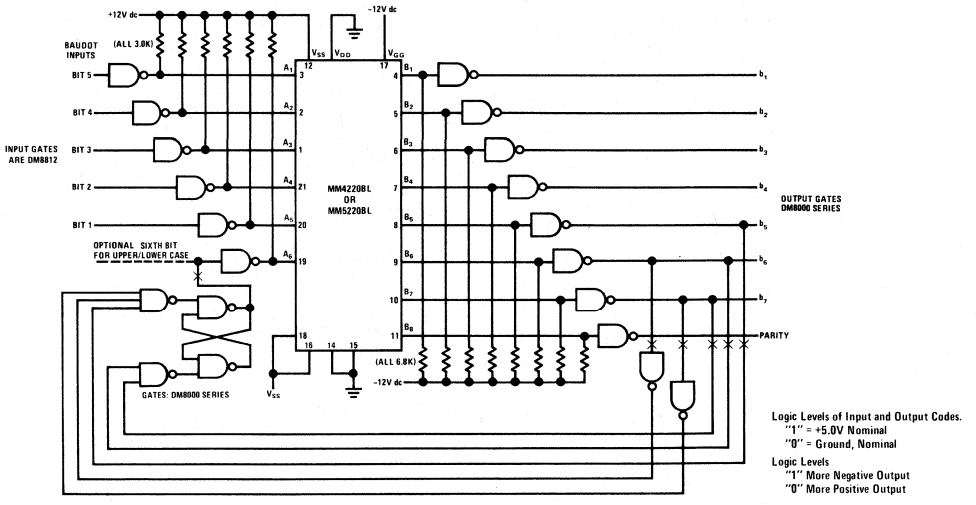
The accompanying table is applicable for the code conversion scheme as shown (or its alternate) rather than for the device itself. The input and output codes are defined at the TTL gates with the logic trues high (Logic "1" = +5 volts, nominal; Logic "0" = Ground, nominal).

device characteristics

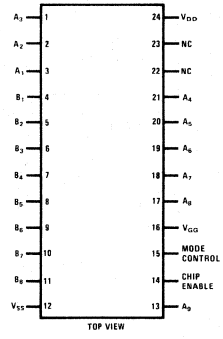
For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical application and connection diagram

Baudot to ASCII



Dual-In-Line Package



Order Number MM4220BL/J or MM5220BL/J
See NS Package J24A

Order Number MM5220BL/N
See NS Package N24B

code conversion tables

ROM ADDRESS	FUNCTION: INPUT BAUDOT SYMBOL	FUNCTION: OUTPUT ASCII SYMBOL	CODE: INPUT CASE	BAUDOT 1	2	3	4	5	OUTPUT ASCII EP	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	Blank	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	T	T	0	0	0	0	0	1	1	1	0	1	0	1	0	0
2	CR	CR	0	0	0	0	1	0	1	0	0	0	1	1	0	1
3	O	O	0	0	0	0	1	1	1	1	0	0	1	1	1	1
4	Space	Space	0	0	0	1	0	0	1	0	1	0	0	0	0	0
5	H	H	0	0	0	1	0	1	0	1	0	0	1	0	0	0
6	N	N	0	0	0	1	1	0	0	1	0	0	1	1	1	0
7	M	M	0	0	0	1	1	1	0	1	0	0	1	1	0	1
8	LF	LF	0	0	1	0	0	0	0	0	0	0	1	0	1	0
9	L	L	0	0	1	0	0	1	1	1	0	0	1	1	0	0
10	R	R	0	0	1	0	1	0	1	1	0	1	0	0	1	0
11	G	G	0	0	1	0	1	1	0	1	0	0	0	1	1	1
12	I	I	0	0	1	1	0	0	1	1	0	0	1	0	0	1
13	P	P	0	0	1	1	0	1	0	1	0	1	0	0	0	0
14	C	C	0	0	1	1	1	0	1	1	0	0	0	0	1	1
15	V	V	0	0	1	1	1	1	0	1	0	1	0	1	1	0
16	E	E	0	1	0	0	0	0	1	1	0	0	0	1	0	1
17	Z	Z	0	1	0	0	0	1	0	1	0	1	1	0	1	0
18	D	D	0	1	0	0	1	0	0	1	0	0	0	1	0	0
19	B	B	0	1	0	0	1	1	0	1	0	0	0	0	1	0
20	S	S	0	1	0	1	0	0	0	1	0	1	0	0	1	1
21	Y	Y	0	1	0	1	0	1	0	1	0	1	1	0	0	1
22	F	F	0	1	0	1	1	0	1	1	0	0	0	1	1	0
23	X	X	0	1	0	1	1	1	1	1	0	1	1	0	0	0
24	A	A	0	1	1	0	0	0	0	1	0	0	0	0	0	1
25	W	W	0	1	1	0	0	1	1	1	0	1	0	1	1	1
26	J	J	0	1	1	0	1	0	1	1	0	0	1	0	1	0
27	Upper	IS1/Can	0	1	1	0	1	1	0	0	0	1	1	0	0	0
28	U	U	0	1	1	1	0	0	0	1	0	1	0	1	0	1
29	Q	Q	0	1	1	1	0	1	1	1	0	1	0	0	0	1
30	K	K	0	1	1	1	1	0	0	1	0	0	1	0	1	1
31	Lower	Delete	0	1	1	1	1	1	1	1	1	1	1	1	1	1
32	Blank	NULL	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33	5	5	1	0	0	0	0	1	0	0	1	1	0	1	0	1
34	CR	CR	1	0	0	0	1	0	1	0	0	0	1	1	0	1
35	9	9	1	0	0	0	1	1	0	0	1	1	1	0	0	1
36	Space	Space	1	0	0	1	0	0	1	0	1	0	0	0	0	0
37	#/£ S/S	BS/FE	1	0	0	1	0	1	1	0	0	0	1	0	0	0
38	,	,	1	0	0	1	1	0	1	0	1	0	1	1	0	0
39	.	.	1	0	0	1	1	1	0	0	1	0	1	1	1	0
40	LF	LF	1	0	1	0	0	0	0	0	0	0	1	0	1	0
41	)	)	1	0	1	0	0	1	1	0	1	0	1	0	0	1
42	4	4	1	0	1	0	1	0	1	0	1	1	0	1	0	0
43	&	&	1	0	1	0	1	1	1	0	1	0	0	1	1	0
44	8	8	1	0	1	1	0	0	1	0	1	1	1	0	0	0
45	0	0	1	0	1	1	0	1	0	0	1	1	0	0	0	0
46	:	:	1	0	1	1	1	0	0	0	1	1	1	0	1	0
47	;	;	1	0	1	1	1	1	1	0	1	1	1	0	1	1
48	3	3	1	1	0	0	0	0	0	0	1	1	0	0	1	1
49	"	"	1	1	0	0	0	1	0	0	1	0	0	0	1	0
50	$	$	1	1	0	0	1	0	0	0	1	0	0	1	0	0
51	?	?	1	1	0	0	1	1	0	0	1	1	1	1	1	1
52	Bell	Bell	1	1	0	1	0	0	1	0	0	0	0	1	1	1
53	6	6	1	1	0	1	0	1	0	0	1	1	0	1	1	0
54	!	!	1	1	0	1	1	0	0	0	1	0	0	0	0	1
55	/	/	1	1	0	1	1	1	1	0	1	0	1	1	1	1
56	–	–	1	1	1	0	0	0	0	0	1	0	1	1	0	1
57	2	2	1	1	1	0	0	1	1	0	1	1	0	0	1	0
58	'	'	1	1	1	0	1	0	0	0	1	0	0	1	1	1
59	Upper	Can	1	1	1	0	1	1	0	0	0	1	1	0	0	0
60	7	7	1	1	1	1	0	0	1	0	1	1	0	1	1	1
61	1	1	1	1	1	1	0	1	1	0	1	1	0	0	0	1
62	(	(	1	1	1	1	1	0	0	0	1	0	1	0	0	0
63	Lower	Delete	1	1	1	1	1	1	1	1	1	1	1	1	1	1

LEGEND:
EP = Even Parity
LF = Line Feed
CR = Carriage Return
Can = Cancel
IS1 = Information Separator #1
S/S = Stop/Start
BS = Back Space

National Semiconductor

MM4220BM/MM5220BM Sine Look-Up Table

general description

The MM4220BM/MM5220BM is a 1024-monolithic MOS read only memory that has been programmed to solve for the sine value x of a known angle θ; i.e., to obtain the solution of the equation $x = \sin \theta$.

Values of θ are defined in the look up table for $0^\circ \leq \theta < 90^\circ$ (quadrant I) which has corresponding solutions of $0 \leq x < 1$. For values of $90^\circ < \theta \leq 180^\circ$ (quadrant II), enter the complement $(180^\circ - \theta)$ to obtain the correct solution. Solutions for quadrants III and IV differ in sign with I and II. This is summarized in Table 1.

This input is divided into 128 parts for θ in each quadrant. Thus, the appropriate input address is $(\theta^1/90^\circ)(128)$ to the nearest whole integer. The actual input code to the ROM is the input address expressed in binary, with A_1 being the least significant bit.

The output is the value of X expressed in binary. The output lines $B_1, B_2, \ldots . B_8$ are binary place values 1/2, 1/4, ... 1/256. The sign for negative values of X is externally generated.

The 8 bit output code has been rounded off from a larger word code, i.e., where A_9 was a binary "1" it carried into the LSB of the eight bit code, where A_9 was a binary "0" it was simply dropped.

EXAMPLE

Find the sine of 45°.

The input address is (45/90) 128 = 64 or 1000000, as expressed in binary. The converter generates the output .10110101 whose decimal equivalent is 0.707131. Thus, sin 45° = 0.707.

Find the sine of 210°.

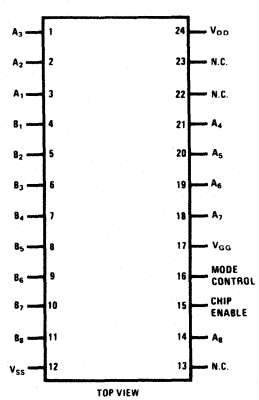
This value is in quadrant III; therefore $\theta^1 = 210^\circ - 180^\circ = 30^\circ$. The input address is then (30/90) $128 \cong 43$ to the nearest whole integer. The binary input to the ROM is then 0101011. The output value is .10000001 or 0.503906. Thus, sin 210° = −0.504, with the sign generated by the external logic. The solution is within 1%; note that address 43 is actually equal to 30.23°.

device characteristics

For full electrical, environmental and mechanical details refer to the MM4220/MM5220 1024-bit read only memory data sheet.

connection diagram

Dual-In-Line Package



Order Number MM4220BM/J or MM5220BM/J
See NS Package J24A

Order Number MM5220BM/N
See NS Package N24B

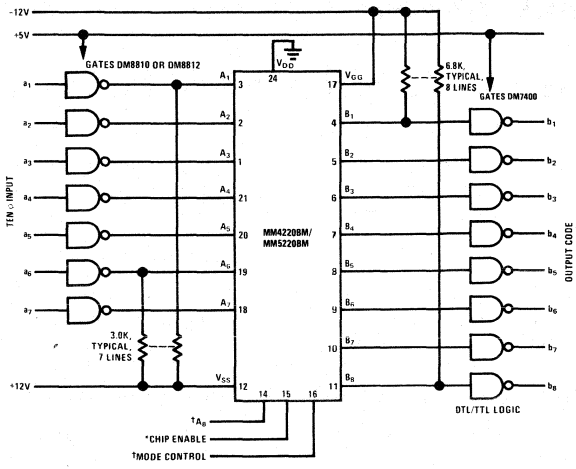
pattern selection form

ADDRESS REFERENCE	FUNCTION INPUT		CODE OUTPUT							
	DEGREES	RADIANS	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
0	.00	.000	0	0	0	0	0	0	0	0
1	.70	.012	1	1	0	0	0	0	0	0
2	1.41	.025	0	1	1	0	0	0	0	0
3	2.11	.037	1	0	0	1	0	0	0	0
4	2.81	.049	0	0	1	1	0	0	0	0
5	3.52	.061	1	1	1	1	0	0	0	0
6	4.22	.074	1	1	0	0	1	0	0	0
7	4.92	.086	0	1	1	0	1	0	0	0
8	5.63	.098	1	0	0	1	1	0	0	0
9	6.33	.110	0	0	1	1	1	0	0	0
10	7.03	.123	1	1	1	1	1	0	0	0
11	7.73	.135	0	1	0	0	0	1	0	0
12	8.44	.147	1	0	1	0	0	1	0	0
13	9.14	.160	0	0	0	1	0	1	0	0
14	9.84	.172	0	0	1	1	0	1	0	0
15	10.55	.184	1	1	1	1	0	1	0	0
16	11.25	.196	0	1	0	0	1	1	0	0
17	11.95	.209	1	0	1	0	1	1	0	0
18	12.66	.221	0	0	0	1	1	1	0	0
19	13.36	.233	1	1	0	1	1	1	0	0
20	14.06	.245	0	1	1	1	1	1	0	0
21	14.77	.258	1	0	0	0	0	0	1	0
22	15.47	.270	0	0	1	0	0	0	1	0
23	16.17	.282	1	1	1	0	0	0	1	0
24	16.88	.295	0	1	0	1	0	0	1	0
25	17.58	.307	1	0	1	1	0	0	1	0
26	18.28	.319	0	0	0	0	1	0	1	0
27	18.98	.331	1	1	0	0	1	0	1	0
28	19.69	.344	0	1	1	0	1	0	1	0
29	20.39	.356	1	0	0	1	1	0	1	0
30	21.09	.368	0	0	1	1	1	0	1	0
31	21.80	.380	1	1	1	1	1	0	1	0
32	22.50	.393	0	1	0	0	0	1	1	0
33	23.20	.405	1	1	1	0	0	1	1	0
34	23.91	.417	1	1	1	0	0	1	1	0
35	24.61	.430	0	1	0	1	0	1	1	0
36	25.31	.442	1	0	1	1	0	1	1	0
37	26.02	.454	0	0	0	0	1	1	1	0
38	26.72	.466	1	1	0	0	1	1	1	0
39	27.42	.479	0	1	1	0	1	1	1	0
40	28.13	.491	0	0	0	1	1	1	1	0
41	28.83	.503	1	1	0	1	1	1	1	0
42	29.53	.515	0	1	1	1	1	1	1	0
43	30.23	.528	0	0	0	0	0	0	0	1
44	30.94	.540	1	1	0	0	0	0	0	1
45	31.64	.552	0	1	1	0	0	0	0	1
46	32.34	.565	1	0	0	1	0	0	0	1
47	33.05	.577	1	1	0	1	0	0	0	1
48	33.75	.589	0	1	1	1	0	0	0	1
49	34.45	.601	1	0	0	0	1	0	0	1
50	35.16	.614	1	1	0	0	1	0	0	1
51	35.86	.626	0	1	1	0	1	0	0	1
52	36.56	.638	0	0	0	1	1	0	0	1
53	37.27	.650	1	1	0	1	1	0	0	1
54	37.97	.663	1	0	1	1	1	0	0	1
55	38.67	.675	0	0	0	0	0	1	0	1
56	39.37	.687	0	1	0	0	0	1	0	1
57	40.08	.699	1	0	1	0	0	1	0	1
58	40.78	.712	1	1	1	0	0	1	0	1
59	41.48	.724	1	0	0	1	0	1	0	1
60	42.19	.736	0	0	1	1	0	1	0	1
61	42.89	.749	0	1	1	1	0	1	0	1
62	43.59	.761	0	0	0	0	1	1	0	1
63	44.30	.773	1	1	0	0	1	1	0	1

pattern selection form(con't)

ADDRESS REFERENCE	FUNCTION INPUT		CODE OUTPUT							
	DEGREES	RADIANS	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
64	45.00	.785	1	0	1	0	1	1	0	1
65	45.70	.798	1	1	1	0	1	1	0	1
66	46.41	.810	1	0	0	1	1	1	0	1
67	47.11	.822	1	1	0	1	1	1	0	1
68	47.81	.834	1	0	1	1	1	1	0	1
69	48.52	.847	0	0	0	0	0	0	1	1
70	49.22	.859	0	1	0	0	0	0	1	1
71	49.92	.871	0	0	1	0	0	0	1	1
72	50.62	.884	0	1	1	0	0	0	1	1
73	51.33	.896	0	0	0	1	0	0	1	1
74	52.03	.908	0	1	0	1	0	0	1	1
75	52.73	.920	1	1	0	1	0	0	1	1
76	53.44	.933	1	0	1	1	0	0	1	1
77	54.14	.945	1	1	1	1	0	0	1	1
78	54.84	.957	1	0	0	0	1	0	1	1
79	55.55	.969	1	1	0	0	1	0	1	1
80	56.25	.982	1	0	1	0	1	0	1	1
81	56.95	.994	0	1	1	0	1	0	1	1
82	57.66	1.006	0	0	0	1	1	0	1	1
83	58.36	1.019	0	1	0	1	1	0	1	1
84	59.06	1.031	1	1	0	1	1	0	1	1
85	59.77	1.043	1	0	1	1	1	0	1	1
86	60.47	1.055	0	1	1	1	1	0	1	1
87	61.17	1.068	0	0	0	0	0	1	1	1
88	61.87	1.080	0	1	0	0	0	1	1	1
89	62.58	1.092	1	1	0	0	0	1	1	1
90	63.28	1.104	0	0	1	0	0	1	1	1
91	63.98	1.117	0	1	1	0	0	1	1	1
92	64.69	1.129	1	1	1	0	0	1	1	1
93	65.39	1.141	0	0	0	1	0	1	1	1
94	66.09	1.154	0	1	0	1	0	1	1	1
95	66.80	1.166	1	1	0	1	0	1	1	1
96	67.50	1.178	0	0	1	1	0	1	1	1
97	68.20	1.190	1	0	1	1	0	1	1	1
98	68.91	1.203	1	1	1	1	0	1	1	1
99	69.61	1.215	0	0	0	0	1	1	1	1
100	70.31	1.227	1	0	0	0	1	1	1	1
101	71.02	1.239	0	1	0	0	1	1	1	1
102	71.72	1.252	1	1	0	0	1	1	1	1
103	72.42	1.264	0	0	1	0	1	1	1	1
104	73.12	1.276	1	0	1	0	1	1	1	1
105	73.83	1.289	0	1	1	0	1	1	1	1
106	74.53	1.301	0	1	1	0	1	1	1	1
107	75.23	1.313	1	1	1	0	1	1	1	1
108	75.94	1.325	0	0	0	1	1	1	1	1
109	76.64	1.338	1	0	0	1	1	1	1	1
110	77.34	1.350	0	1	0	1	1	1	1	1
111	78.05	1.362	0	1	0	1	1	1	1	1
112	78.75	1.374	1	1	0	1	1	1	1	1
113	79.45	1.387	1	1	0	1	1	1	1	1
114	80.16	1.399	0	0	1	1	1	1	1	1
115	80.86	1.411	0	0	1	1	1	1	1	1
116	81.56	1.424	1	0	1	1	1	1	1	1
117	82.27	1.436	1	0	1	1	1	1	1	1
118	82.97	1.448	0	1	1	1	1	1	1	1
119	83.67	1.460	0	1	1	1	1	1	1	1
120	84.38	1.473	1	1	1	1	1	1	1	1
121	85.08	1.485	1	1	1	1	1	1	1	1
122	85.78	1.497	1	1	1	1	1	1	1	1
123	86.48	1.509	1	1	1	1	1	1	1	1
124	87.19	1.522	1	1	1	1	1	1	1	1
125	87.89	1.534	1	1	1	1	1	1	1	1
126	88.59	1.546	1	1	1	1	1	1	1	1
127	89.30	1.559	1	1	1	1	1	1	1	1

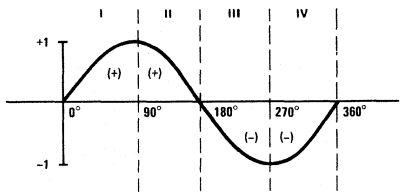
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

Table 1. SINE

	INPUT		OUTPUT	
Quadrant	**Range**	**Entry to ROM (θ^1)**	**Binary Value**	**Sign**
I	$\geq 0^\circ < 90^\circ$	Direct	Direct Reading	+
II	$> 90^\circ \leq 180^\circ$	$180^\circ - X$	Direct Reading	+
III	$\geq 180^\circ < 270^\circ$	$X - 180^\circ$	Direct Reading	–
IV	$> 270^\circ \leq 360^\circ$	$360^\circ - X$	Direct Reading	–



National Semiconductor

MM4220BN/MM5220BN Arctangent Look-Up Table

general description

The MM4220BN/MM5220BN is a 1024-bit monolithic MOS read only memory that has been programmed to solve for the angle θ whose tangent value x is known; i.e., to obtain the solution to the equation: $\theta = \arctan x$.

Values of x are defined in the Look Up table for $0 \leq x < 1$ with angles corresponding from $0^\circ \leq \theta < 45^\circ$. For values $x \geq 1$, the reciprocal of x (i.e., 1/x) must be entered and the output angle must be complemented to obtain the actual value.

The input is divided into 128 equal parts for x. Thus, the appropriate input address is (128)(x) to the nearest whole integer for obtaining the appropriate ROM address. The input code is the ROM address expressed in binary with A_1 being the least significant bit. For input values greater than unity, the decimal reciprocal is to be taken prior to entry of the binary address.

The output has been normalized for 45°. To obtain the true angular reading, the output should be multiplied by 45°, i.e.: $\theta = (\theta_{output}) \times 45^\circ$ where θ_{output} is the decimal equivalent of the output. The output code is the normalized value of the angle θ expressed in binary. The output lines B_1, B_2, ... B_8 are binary place values 1/2, 1/4, ... 1/256. To obtain angles between 45° and 89.6° which occur when input values of x are equal to or greater than unity, either complement the output binary code and add a 1, or complement the resultant angular value (i.e., subtract from 90°).

The 8-bit output code has been rounded off. That is, if another bit of even lower significance had been computed for the given arctangent value was a binary "1", it would have carried over into the LSB of the eight bit code. If it was a binary "0", it would have been dropped.

EXAMPLE

Find the angle whose tangent is 0.258.

The input address is 128 x 0.258, or 33 to the nearest integer. Expressed in binary, this is 0100001, and is the actual input code to the converter. The converter will generate the binary value .01010010, whose decimal equivalent is 0.3203125.

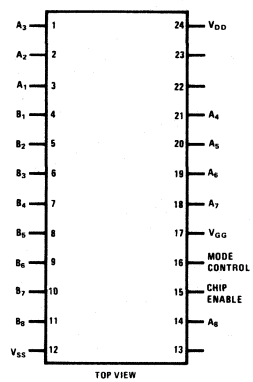
Thus, $\theta = 0.320 \times 45^\circ = 14.4^\circ$

device characteristics

For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

connection diagram

Dual-In-Line Package



Order Number MM4220N/J or MM5220BN/J
See NS Package J24A

Order Number MM5220BN/N
See NS Package N24B

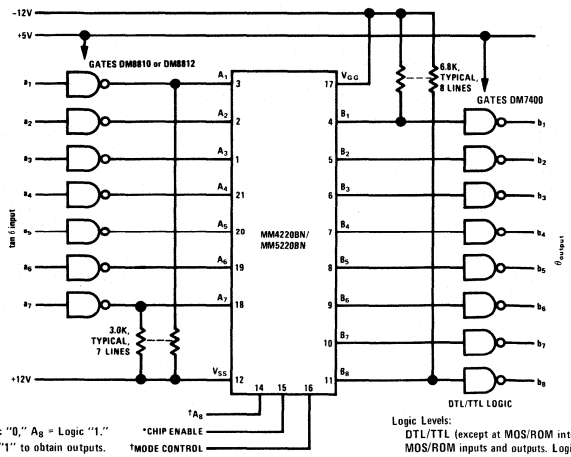
pattern selection form

ADDRESS 128 (x)	OUTPUT CODE (θ_{OUTPUT}) B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
2	1	0	1	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	0	1	0	1	0	0	0	0
5	0	0	1	1	0	0	0	0
6	1	1	1	1	0	0	0	0
7	0	1	0	0	1	0	0	0
8	0	0	1	0	1	0	0	0
9	1	1	1	0	1	0	0	0
10	1	0	0	1	1	0	0	0
11	0	0	1	1	1	0	0	0
12	0	1	1	1	1	0	0	0
13	1	0	0	0	0	1	0	0
14	1	1	0	0	0	1	0	0
15	0	1	1	0	0	1	0	0
16	0	0	0	1	0	1	0	0
17	1	1	0	1	0	1	0	0
18	1	0	1	1	0	1	0	0
19	0	0	0	0	1	1	0	0
20	0	1	0	0	1	1	0	0
21	1	0	1	0	1	1	0	0
22	1	1	1	0	1	1	0	0
23	0	1	0	1	1	1	0	0
24	0	0	1	1	1	1	0	0
25	1	1	1	1	1	1	0	0
26	1	0	0	0	0	0	1	0
27	0	0	1	0	0	0	1	0
28	0	1	1	0	0	0	1	0
29	0	0	0	1	0	0	1	0
30	1	1	0	1	0	0	1	0
31	1	0	1	1	0	0	1	0
32	0	0	0	0	1	0	1	0
33	0	1	0	0	1	0	1	0
34	0	0	1	0	1	0	1	0
35	1	1	1	0	1	0	1	0
36	1	0	0	1	1	0	1	0
37	1	1	0	1	1	0	1	0
38	0	1	1	1	1	0	1	0
39	0	0	0	0	0	1	1	0
40	0	1	0	0	0	1	1	0
41	1	0	1	0	0	1	1	0
42	1	1	1	0	0	1	1	0
43	1	0	0	1	0	1	1	0
44	0	0	1	1	0	1	1	0
45	0	1	1	1	0	1	1	0
46	0	0	0	0	1	1	1	0
47	0	1	0	0	1	1	1	0
48	1	0	1	0	1	1	1	0
49	1	1	1	0	1	1	1	0
50	1	0	0	1	1	1	1	0
51	1	1	0	1	1	1	1	0
52	0	1	1	1	1	1	1	0
53	0	0	0	0	0	0	0	1
54	0	1	0	0	0	0	0	1
55	0	0	1	0	0	0	0	1
56	0	1	1	0	0	0	0	1
57	0	0	0	1	0	0	0	1
58	0	1	0	1	0	0	0	1
59	1	0	1	1	0	0	0	1
60	1	1	1	1	0	0	0	1
61	1	0	0	0	1	0	0	1
62	1	1	0	0	1	0	0	1
63	1	0	1	0	1	0	0	1
64	1	1	1	0	1	0	0	1
65	1	0	0	1	1	0	0	1
66	1	1	0	1	1	0	0	1
67	1	0	1	1	1	0	0	1
68	1	1	1	1	1	0	0	1
69	1	0	0	0	0	1	0	1
70	1	1	0	0	0	1	0	1
71	1	0	1	0	0	1	0	1
72	1	1	1	0	0	1	0	1
73	1	0	0	1	0	1	0	1
74	1	1	0	1	0	1	0	1
75	1	0	1	1	0	1	0	1
76	0	1	1	1	0	1	0	1
77	0	0	0	0	1	1	0	1
78	0	1	0	0	1	1	0	1
79	0	0	1	0	1	1	0	1
80	0	1	1	0	1	1	0	1
81	0	0	0	1	1	1	0	1
82	1	0	0	1	1	1	0	1
83	1	1	0	1	1	1	0	1
84	1	0	1	1	1	1	0	1
85	1	1	1	1	1	1	0	1
86	1	0	0	0	0	0	1	1
87	0	1	0	0	0	0	1	1
88	0	0	1	0	0	0	1	1
89	0	1	1	0	0	0	1	1
90	1	1	1	0	0	0	1	1
91	1	0	0	1	0	0	1	1
92	1	1	0	1	0	0	1	1
93	1	0	1	1	0	0	1	1
94	0	1	1	1	0	0	1	1
95	0	0	0	0	1	0	1	1
96	1	0	0	0	1	0	1	1
97	1	1	0	0	1	0	1	1
98	1	0	1	0	1	0	1	1
99	0	1	1	0	1	0	1	1
100	0	0	0	1	1	0	1	1
101	1	0	0	1	1	0	1	1
102	1	1	0	1	1	0	1	1
103	1	0	1	1	1	0	1	1
104	0	1	1	1	1	0	1	1
105	0	0	0	0	0	1	1	1
106	1	0	0	0	0	1	1	1
107	1	1	0	0	0	1	1	1
108	0	0	1	0	0	1	1	1
109	0	1	1	0	0	1	1	1
110	1	1	1	0	0	1	1	1
111	1	0	0	1	0	1	1	1
112	0	1	0	1	0	1	1	1
113	1	1	0	1	0	1	1	1
114	1	0	1	1	0	1	1	1
115	0	1	1	1	0	1	1	1
116	0	0	0	0	1	1	1	1
117	1	0	0	0	1	1	1	1
118	1	1	0	0	1	1	1	1
119	0	0	1	0	1	1	1	1
120	1	0	1	0	1	1	1	1
121	1	1	1	0	1	1	1	1
122	0	0	0	1	1	1	1	1
123	1	0	0	1	1	1	1	1
124	1	1	0	1	1	1	1	1
125	0	0	1	1	1	1	1	1
126	1	0	1	1	1	1	1	1
127	0	1	1	1	1	1	1	1

MM5220BN

Note: 1 more negative output.
0 more positive output.

typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

National Semiconductor

MM4220EK/MM5220EK BCDIC-to-EBCDIC/ASCII-to-EBCDIC Code Converter

general description

The MM4220EK/MM5220EK is a 1024-bit read only memory that has been programmed to convert both Binary Coded Decimal Interchange Code (BCDIC) and the American Standard Code for Information Interchange (ASCII) to Extended Binary Coded Decimal Interchange Code (EBCDIC).

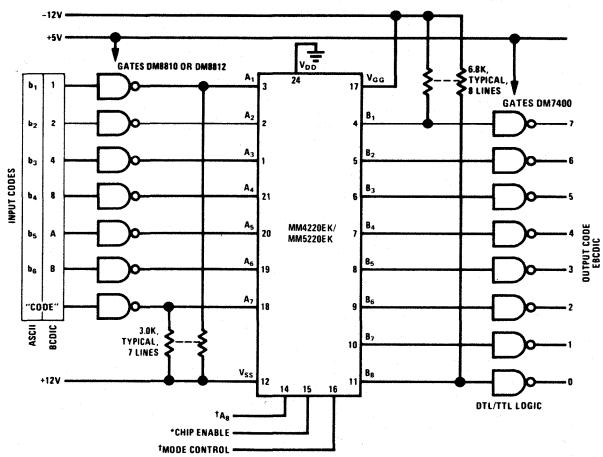
The BCDIC-to-EBCDIC converter is located in the first 64 8-bit bytes of the ROM. The unused parity check bit (the most significant input BCDIC bit) is always a "0".

The ASCII-to-EBCDIC converter is located in the second 64 8-bit bytes of the ROM. Thus, the input ASCII code in addresses 64 through 127 has a "1" in the most significant (A_7) bit which is used with the selection logic. The resulting 6-bit ASCII input is for display–only upper case and numerical codes, since it will not accept the control commands or the lower case characters.

device characteristics

For full electrical, environmental and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

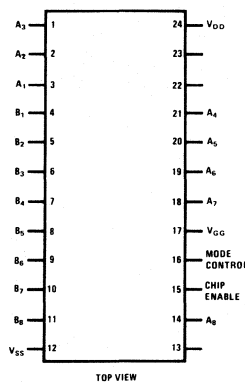
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4220EK/J or MM5220EK/J
See NS Package J24A

Order Number MM5220EK/N
See NS Package N24B

code conversion tables

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT							OUTPUT								
	BCDIC SYMBOL	EBCDIC SYMBOL	CODE	BCDIC B	A	8	4	2	1	EBCDIC 0	1	2	3	4	5	6	7
0	Space	Space	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1
2	2	2	0	0	0	0	0	1	0	1	1	1	1	0	0	1	0
3	3	3	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1
4	4	4	0	0	0	0	1	0	0	1	1	1	1	0	1	0	0
5	5	5	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1
6	6	6	0	0	0	0	1	1	0	1	1	1	1	0	1	1	0
7	7	7	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
8	8	8	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0
9	9	9	0	0	0	1	0	0	1	1	1	1	1	1	0	0	1
10	0	0	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0
11	# or =	#	0	0	0	1	0	1	1	0	1	1	1	1	0	1	1
12	@ or '	@	0	0	0	1	1	0	0	0	1	1	1	1	1	0	0
13	:	:	0	0	0	1	1	0	1	0	1	1	1	1	0	1	0
14	>	>	0	0	0	1	1	1	0	0	1	1	0	1	1	1	0
15	√(TM)	TM	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1
16	Space	Space	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
17	/	/	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1
18	S	S	0	0	1	0	0	1	0	1	1	1	0	0	0	1	0
19	T	T	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1
20	U	U	0	0	1	0	1	0	0	1	1	1	0	0	1	0	0
21	V	V	0	0	1	0	1	0	1	1	1	1	0	0	1	0	1
22	W	W	0	0	1	0	1	1	0	1	1	1	0	0	1	1	0
23	X	X	0	0	1	0	1	1	1	1	1	1	0	0	1	1	1
24	Y	Y	0	0	1	1	0	0	0	1	1	1	0	1	0	0	0
25	Z	Z	0	0	1	1	0	0	1	1	1	1	0	1	0	0	1
26	‡(RM)	RM	0	0	1	1	0	1	0	1	1	1	0	0	0	0	0
27	,	,	0	0	1	1	0	1	1	0	1	1	0	1	0	1	1
28	% or (	%	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0
29	v	+	0	0	1	1	1	0	1	0	1	0	0	1	1	1	0
30	\	¢	0	0	1	1	1	1	0	0	1	0	0	1	0	1	0
31	⌗	=	0	0	1	1	1	1	1	0	1	1	1	1	1	1	0
32	-	-	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0
33	J	J	0	1	0	0	0	0	1	1	1	0	1	0	0	0	1
34	K	K	0	1	0	0	0	1	0	1	1	0	1	0	0	1	0
35	L	L	0	1	0	0	0	1	1	1	1	0	1	0	0	1	1
36	M	M	0	1	0	0	1	0	0	1	1	0	1	0	1	0	0
37	N	N	0	1	0	0	1	0	1	1	1	0	1	0	1	0	1
38	O	O	0	1	0	0	1	1	0	1	1	0	1	0	1	1	0
39	P	P	0	1	0	0	1	1	1	1	1	0	1	0	1	1	1
40	Q	Q	0	1	0	1	0	0	0	1	1	0	1	1	0	0	0
41	R	R	0	1	0	1	0	0	1	1	1	0	1	1	0	0	1
42	!	!	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0
43	$	$	0	1	0	1	0	1	1	0	1	0	1	1	0	1	1
44	*	*	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0
45	]	)	0	1	0	1	1	0	1	0	1	0	1	1	1	0	1
46	;	;	0	1	0	1	1	1	0	0	1	0	1	1	1	1	0
47	△	"	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
48	& or +	&	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0
49	A	A	0	1	1	0	0	0	1	1	1	0	0	0	0	0	1
50	B	B	0	1	1	0	0	1	0	1	1	0	0	0	0	1	0
51	C	C	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
52	D	D	0	1	1	0	1	0	0	1	1	0	0	0	1	0	0
53	E	E	0	1	1	0	1	0	1	1	1	0	0	0	1	0	1
54	F	F	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0
55	G	G	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1
56	H	H	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0
57	I	I	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1
58	?	?	0	1	1	1	0	1	0	0	1	1	0	1	1	1	1
59	.	.	0	1	1	1	0	1	1	0	1	0	0	1	0	1	1
60	¤ or)	¤	0	1	1	1	1	0	0	0	1	1	0	1	0	1	0
61	[	(	0	1	1	1	1	0	1	0	1	0	0	1	1	0	1
62	<	<	0	1	1	1	1	1	0	0	1	0	0	1	1	0	0
63	‡	'	0	1	1	1	1	1	1	0	1	1	1	1	1	0	1

code conversion tables(con't)

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT							OUTPUT								
	ASCII SYMBOL	EBCDIC SYMBOL	CODE	ASCII b_6	b_5	b_4	b_3	b_2	b_1	EBCDIC 0	1	2	3	4	5	6	7
64	@	@	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
65	A	A	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1
66	B	B	1	0	0	0	0	1	0	1	1	0	0	0	0	1	0
67	C	C	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
68	D	D	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0
69	E	E	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1
70	F	F	1	0	0	0	1	1	0	1	1	0	0	0	1	1	0
71	G	G	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
72	H	H	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0
73	I	I	1	0	0	1	0	0	1	1	1	0	0	1	0	0	1
74	J	J	1	0	0	1	0	1	0	1	1	0	1	0	0	0	1
75	K	K	1	0	0	1	0	1	1	1	1	0	1	0	0	1	0
76	L	L	1	0	0	1	1	0	0	1	1	0	1	0	0	1	1
77	M	M	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0
78	N	N	1	0	0	1	1	1	0	1	1	0	1	0	1	0	1
79	O	O	1	0	0	1	1	1	1	1	1	0	1	0	1	1	0
80	P	P	1	0	1	0	0	0	0	1	1	0	1	0	1	1	1
81	Q	Q	1	0	1	0	0	0	1	1	1	0	1	1	0	0	0
82	R	R	1	0	1	0	0	1	0	1	1	0	1	1	0	0	1
83	S	S	1	0	1	0	0	1	1	1	1	1	0	0	0	1	0
84	T	T	1	0	1	0	1	0	0	1	1	1	0	0	0	1	1
85	U	U	1	0	1	0	1	0	1	1	1	1	0	0	1	0	0
86	V	V	1	0	1	0	1	1	0	1	1	1	0	0	1	0	1
87	W	W	1	0	1	0	1	1	1	1	1	1	0	0	1	1	0
88	X	X	1	0	1	1	0	0	0	1	1	1	0	0	1	1	1
89	Y	Y	1	0	1	1	0	0	1	1	1	1	0	1	0	0	0
90	Z	Z	1	0	1	1	0	1	0	1	1	1	0	1	0	0	1
91	[	(	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1
92	\	\	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0
93	]	)	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1
94	⌒ or ^	¬	1	0	1	1	1	1	0	0	1	0	1	1	1	1	1
95	–	–	1	0	1	1	1	1	1	0	1	1	0	1	1	0	1
96	Space	Space	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0
97	!	!	1	1	0	0	0	0	1	0	1	0	1	1	0	1	0
98	"	"	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1
99	#	#	1	1	0	0	0	1	1	0	1	1	1	1	0	1	1
100	$	$	1	1	0	0	1	0	0	0	1	0	1	1	0	1	1
101	%	%	1	1	0	0	1	0	1	0	1	1	0	1	1	0	0
102	&	&	1	1	0	0	1	1	0	0	1	0	1	0	0	0	0
103	'	'	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1
104	(	(	1	1	0	1	0	0	0	0	1	0	0	1	1	0	1
105	)	)	1	1	0	1	0	0	1	0	1	0	1	1	1	0	1
106	*	*	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0
107	+	+	1	1	0	1	0	1	1	0	1	0	0	1	1	1	0
108	,	,	1	1	0	1	1	0	0	0	1	1	0	1	0	1	1
109	-	-	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0
110	.	.	1	1	0	1	1	1	0	0	1	0	0	1	0	1	1
111	/	/	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1
112	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
113	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1
114	2	2	1	1	1	0	0	1	0	1	1	1	1	0	0	1	0
115	3	3	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1
116	4	4	1	1	1	0	1	0	0	1	1	1	1	0	1	0	0
117	5	5	1	1	1	0	1	0	1	1	1	1	1	0	1	0	1
118	6	6	1	1	1	0	1	1	0	1	1	1	1	0	1	1	0
119	7	7	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
120	8	8	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0
121	9	9	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1
122	:	:	1	1	1	1	0	1	0	0	1	1	1	1	0	1	0
123	;	;	1	1	1	1	0	1	1	0	1	0	1	1	1	1	0
124	<	<	1	1	1	1	1	0	0	0	1	0	0	1	1	0	0
125	=	=	1	1	1	1	1	0	1	0	1	1	1	1	1	1	0
126	>	>	1	1	1	1	1	1	0	0	1	1	0	1	1	1	0
127	?	?	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1

National Semiconductor

MM4220LR/MM5220LR BCDIC-to-ASCII-7/ASCII-7-to-BCDIC Code Converter

general description

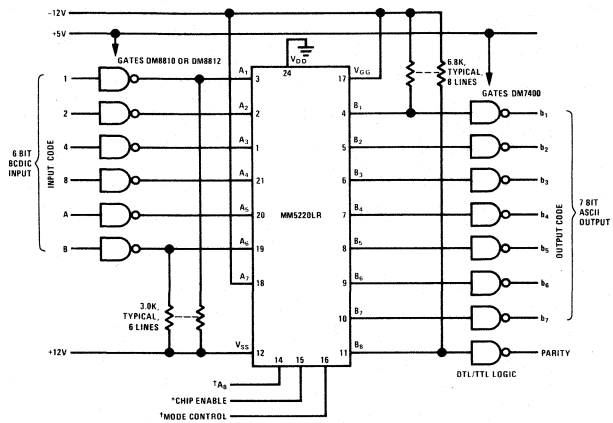
The MM4220LR/MM5220LR is a 128 x 8 read only memory which has been programmed to convert the 64 characters of the Binary Coded Decimal Interchange Code (BCDIC) to the American Standard code for Information Interchange in seven bits (ASCII-7).

The first half of the ROM, from address 0 to address 63, converts the 64 character ASCII graphic subset to BCDIC. The tables show the character assignments and their binary equivalents.

For electrical, environmental and mechanical details, refer to the MM4220/MM5220 data sheet.

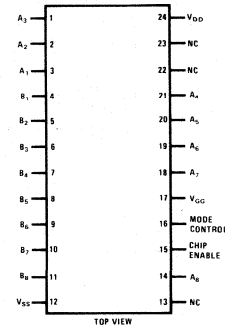
typical applications and connection diagram

BCDIC to ASCII



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

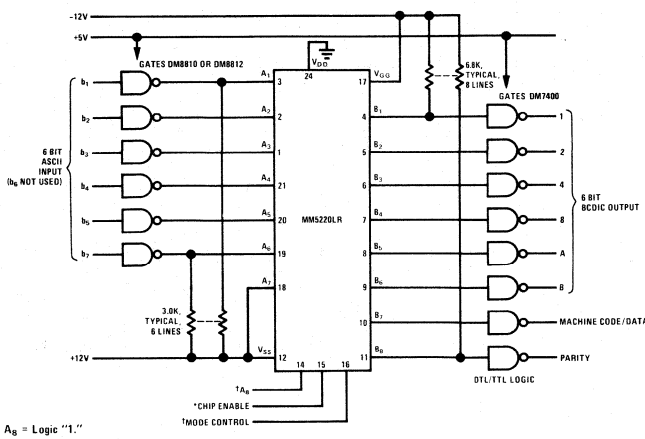
Dual-In-Line Package



Order Number MM4220LR/J or MM5220LR/J
See NS Package J24A

Order Number MM5220LR/N
See NS Package N24B

ASCII to BCDIC



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

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code conversion tables

ASCII to BCDIC

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT							OUTPUT								
	ASCII SYMBOL	BCDIC SYMBOL	CODE	ASCII b_7	b_5	b_4	b_3	b_2	b_1	MC/ DATA	EP	BCDIC B	A	8	4	2	1
0	SP	SP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	!	!	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0	1
2	"	+++	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1
3	#	#	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1	1
4	$	$	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1	1
5	%	%	0	0	0	0	1	0	1	0	1	0	1	1	1	1	0	0
6	&	&	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0
7	'	V	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	1
8	(	Blank	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0
9	)	Δ	0	0	0	1	0	0	1	0	1	1	0	1	1	1	1	1
10	*	*	0	0	0	1	0	1	0	0	1	1	0	1	1	1	0	0
11	VT	‡	0	0	0	1	0	1	1	1	0	0	1	1	0	1	0	
12	,	,	0	0	0	1	1	0	0	0	0	0	1	1	0	1	1	
13	CR	‡	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	
14	.	.	0	0	0	1	1	1	0	0	1	1	1	1	0	1	1	
15	/	/	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1	
16	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	
17	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	1	
18	2	2	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	
19	3	3	0	0	1	0	0	1	1	0	0	0	0	0	0	1	1	
20	4	4	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	
21	5	5	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1	
22	6	6	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0	
23	7	7	0	0	1	0	1	1	1	0	1	0	0	0	1	1	1	
24	8	8	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0	
25	9	9	0	0	1	1	0	0	1	0	0	0	0	1	0	0	1	
26	:	:	0	0	1	1	0	1	0	0	1	0	0	1	1	0	1	
27	;	;	0	0	1	1	0	1	1	0	0	1	0	1	1	1	0	
28	<	<	0	0	1	1	1	0	0	0	1	1	1	1	1	1	0	
29	=	√	0	0	1	1	1	0	1	0	0	0	0	1	1	1	1	
30	>	>	0	0	1	1	1	1	0	0	1	0	0	1	1	1	0	
31	?	?	0	0	1	1	1	1	1	0	0	1	1	1	0	1	0	
32	@	@	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	
33	A	A	0	1	0	0	0	0	1	0	1	1	1	0	0	0	1	
34	B	B	0	1	0	0	0	1	0	0	1	1	1	0	0	1	0	
35	C	C	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1	
36	D	D	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0	
37	E	E	0	1	0	0	1	0	1	0	0	1	1	0	1	0	1	
38	F	F	0	1	0	0	1	1	0	0	0	1	1	0	1	1	0	
39	G	G	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1	
40	H	H	0	1	0	1	0	0	0	0	1	1	1	1	0	0	0	
41	I	I	0	1	0	1	0	0	1	0	0	1	1	1	0	0	1	
42	J	J	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1	
43	K	K	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0	
44	L	L	0	1	0	1	1	0	0	0	1	1	0	0	0	1	1	
45	M	M	0	1	0	1	1	0	1	0	0	1	0	0	1	0	0	
46	N	N	0	1	0	1	1	1	0	0	1	1	0	0	1	0	1	
47	O	O	0	1	0	1	1	1	1	0	1	1	0	0	1	1	0	
48	P	P	0	1	1	0	0	0	0	0	0	1	0	0	1	1	1	
49	Q	Q	0	1	1	0	0	0	1	0	0	1	0	1	0	0	0	
50	R	R	0	1	1	0	0	1	0	0	1	1	0	1	0	0	1	
51	S	S	0	1	1	0	0	1	1	0	0	0	1	0	0	1	0	
52	T	T	0	1	1	0	1	0	0	0	1	0	1	0	0	1	1	
53	U	U	0	1	1	0	1	0	1	0	0	0	1	0	1	0	0	
54	V	V	0	1	1	0	1	1	0	0	1	0	1	0	1	0	1	
55	W	W	0	1	1	0	1	1	1	0	1	0	1	0	1	1	0	
56	X	X	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	
57	Y	Y	0	1	1	1	0	0	1	0	0	0	1	1	0	0	0	
58	Z	Z	0	1	1	1	0	1	0	0	1	0	1	1	0	0	1	
59	[	[	0	1	1	1	0	1	1	0	1	1	1	1	1	0	1	
60	\	\	0	1	1	1	1	0	0	0	0	0	1	1	1	1	0	
61	]	]	0	1	1	1	1	0	1	0	0	1	0	1	1	0	1	
62	^	¤	0	1	1	1	1	1	0	0	0	1	1	1	1	0	0	
63	—	–	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0	
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	

code conversion tables(con't)

BCDIC to ASCII

ROM ADDRESS	FUNCTION INPUT BCDIC, SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT BCDIC CODE	B	A	8	4	2	1	PARITY	OUTPUT ASCII b_7	b_6	b_5	b_4	b_3	b_2	b_1
64	SP	SP	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
65	1	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1
66	2	2	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0
67	3	3	1	0	0	0	0	1	1	0	0	1	1	0	0	1	1
68	4	4	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0
69	5	5	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1
70	6	6	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0
71	7	7	1	0	0	0	1	1	1	1	0	1	1	0	1	1	1
72	8	8	1	0	0	1	0	0	0	1	0	1	1	1	0	0	0
73	9	9	1	0	0	1	0	0	1	0	0	1	1	1	0	0	1
74	0	0	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0
75	#	#	1	0	0	1	0	1	1	1	0	1	0	0	0	1	1
76	@	@	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0
77	:	:	1	0	0	1	1	0	1	0	0	1	1	1	0	1	0
78	>	>	1	0	0	1	1	1	0	1	0	1	1	1	1	1	0
79	√	=	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1
80	Blank	(	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0
81	/	/	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1
82	S	S	1	0	1	0	0	1	0	0	1	0	1	0	0	1	1
83	T	T	1	0	1	0	0	1	1	1	1	0	1	0	1	0	0
84	U	U	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1
85	V	V	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0
86	W	W	1	0	1	0	1	1	0	1	1	0	1	0	1	1	1
87	X	X	1	0	1	0	1	1	1	1	1	0	1	1	0	0	0
88	Y	Y	1	0	1	1	0	0	0	0	1	0	1	1	0	0	1
89	Z	Z	1	0	1	1	0	0	1	0	1	0	1	1	0	1	0
90	‡	VT	1	0	1	1	0	1	0	1	0	0	0	1	0	1	1
91	,	,	1	0	1	1	0	1	1	1	0	1	0	1	1	0	0
92	%	%	1	0	1	1	1	0	0	1	0	1	0	0	1	0	1
93	V	'	1	0	1	1	1	0	1	0	0	1	0	0	1	1	1
94	\	\	1	0	1	1	1	1	0	0	1	0	1	1	1	0	0
95	+++	"	1	0	1	1	1	1	1	0	0	1	0	0	0	1	0
96	–	–	1	1	0	0	0	0	0	0	1	0	1	1	1	1	1
97	J	J	1	1	0	0	0	0	1	1	1	0	0	1	0	1	0
98	K	K	1	1	0	0	0	1	0	0	1	0	0	1	0	1	1
99	L	L	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
100	M	M	1	1	0	0	1	0	0	0	1	0	0	1	1	0	1
101	N	N	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0
102	O	O	1	1	0	0	1	1	0	1	1	0	0	1	1	1	1
103	P	P	1	1	0	0	1	1	1	0	1	0	1	0	0	0	0
104	Q	Q	1	1	0	1	0	0	0	1	1	0	1	0	0	0	1
105	R	R	1	1	0	1	0	0	1	1	1	0	1	0	0	1	0
106	!	!	1	1	0	1	0	1	0	0	0	1	0	0	0	0	1
107	$	$	1	1	0	1	0	1	1	0	0	1	0	0	1	0	0
108	*	*	1	1	0	1	1	0	0	1	0	1	0	1	0	1	0
109	]	]	1	1	0	1	1	0	1	1	1	0	1	1	1	0	1
110	;	;	1	1	0	1	1	1	0	1	0	1	1	1	0	1	1
111	Δ	)	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1
112	&	&	1	1	1	0	0	0	0	1	0	1	0	0	1	1	0
113	A	A	1	1	1	0	0	0	1	0	1	0	0	0	0	0	1
114	B	B	1	1	1	0	0	1	0	0	1	0	0	0	0	1	0
115	C	C	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
116	D	D	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0
117	E	E	1	1	1	0	1	0	1	1	1	0	0	0	1	0	1
118	F	F	1	1	1	0	1	1	0	1	1	0	0	0	1	1	0
119	G	G	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1
120	H	H	1	1	1	1	0	0	0	0	1	0	0	1	0	0	0
121	I	I	1	1	1	1	0	0	1	1	1	0	0	1	0	0	1
122	?	?	1	1	1	1	0	1	0	0	0	1	1	1	1	1	1
123	.	.	1	1	1	1	0	1	1	0	0	1	0	1	1	1	0
124	¤	↑	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0
125	[	[	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1
126	<	<	1	1	1	1	1	1	0	0	0	1	1	1	1	0	0
127	‡	CR	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

National Semiconductor

MM4221RQ/MM5221RQ ASCII-7-to-EIA RS244A/ EIA RS244A-to-ASCII-7 Code Converter

general description

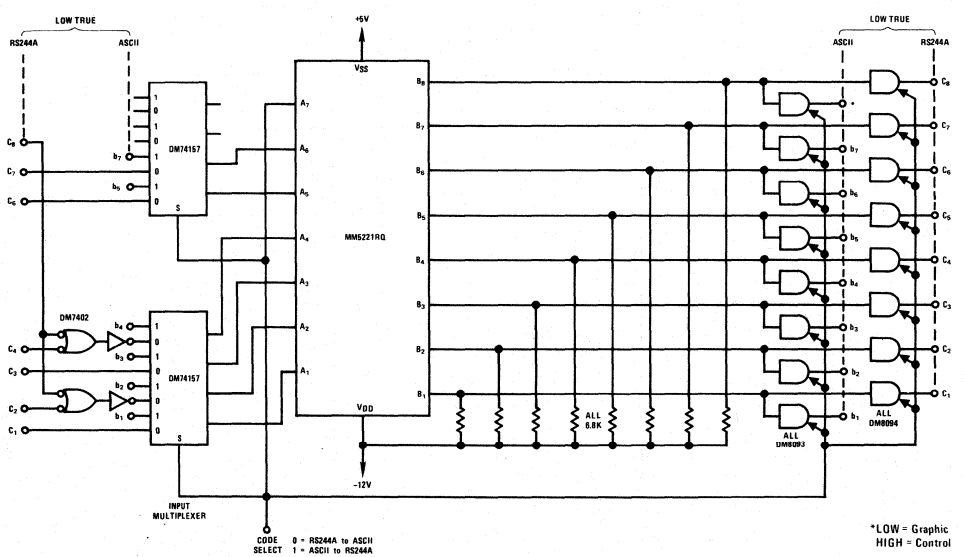
The MM4221RQ/MM5221RQ is a 1024-bit read only memory that has been programmed to convert between the American Standard Code for Information Interchange, compressed to six bits, and the Electronic Industries Association numerical control standard code, RS244A. The second group of addresses, from 64 to 127, effects the reverse conversion.

applications information

In the first 64 entries, compression of ASCII-7 to six bits has been accomplished by dropping bit b_6, and substituting the control codes listed for certain unused ASCII graphic symbols.

In the second 64 entries, the RS244A parity check bit, C_5 is ignored. The bit C_8, used only for the end of block code (EOB) is used externally to detect existence of this symbol, and to insert a redundant code, $C_4 \cdot C_2$ (ROM address 74). This code will be translated arbitrarily as an ASCII EXT.

typical application



Order Number MM4221RQ/J or MM5221RQ/J
See NS Package J24A

Order Number MM5221RQ/N
See NS Package N24B

code conversion tables

ASCII to RS244A

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EIA SYMBOL	CODE	CODE INPUT b_7	b_5	b_4	b_3	b_2	b_1	CODE OUTPUT c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1
0	SP	SP	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1			0	0	0	0	0	0	1								
2			0	0	0	0	0	1	0								
3	ETX	EOB	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
4	EOT	EOR	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1
5	%	%	0							0	1	0	1	1	0	1	1
6	&	&	0							0	0	0	0	1	1	1	0
7			0														
8	BS	BS	0							0	0	1	0	1	0	1	0
9	HT	TAB	0							0	0	1	1	1	1	1	0
10			0							0	0	0	0	0	0	0	0
11	+	+	0							0	1	1	1	0	0	0	0
12	,	,	0							0	0	1	1	1	0	1	1
13	–	–	0							0	1	0	0	0	0	0	0
14	.	.	0							0	1	1	0	1	0	1	1
15	/	/	0							0	0	1	1	0	0	0	1
16	0	0	0							0	0	1	0	0	0	0	0
17	1	1	0							0	0	0	0	0	0	0	1
18	2	2	0							0	0	0	0	0	0	1	0
19	3	3	0							0	0	0	1	0	0	1	1
20	4	4	0							0	0	0	0	0	1	0	0
21	5	5	0							0	0	0	1	0	1	0	1
22	6	6	0							0	0	0	1	0	1	1	0
23	7	7	0							0	0	0	0	0	1	1	1
24	8	8	0							0	0	0	0	1	0	0	0
25	9	9	0							0	0	0	1	1	0	0	1
26			0														
27		UC	0														
28	FS	LC	0							0	1	1	1	1	0	1	0
29	GS		0							0	1	1	1	1	1	0	0
30			0														
31			0														
32			0														
33	a	a	0							0	1	1	0	0	0	0	1
34	b	b	0							0	1	1	0	0	0	1	0
35	c	c	0							0	1	1	1	0	0	1	1
36	d	d	0							0	1	1	0	0	1	0	0
37	e	e	0							0	1	1	0	0	1	0	0
38	f	f	0							0	1	1	1	0	1	1	0
39	g	g	0							0	1	1	0	0	1	1	1
40	h	h	0							0	1	1	0	1	0	0	0
41	i	i	0							0	1	1	1	1	0	0	1
42	j	j	0							0	1	0	1	0	0	0	1
43	k	k	0							0	1	0	1	0	0	1	0
44	l	l	0							0	1	0	0	0	0	1	1
45	m	m	0							0	1	0	1	0	1	0	0
46	n	n	0							0	1	0	0	0	1	0	1
47	o	o	0							0	1	0	0	0	1	1	0
48	p	p	0							0	1	0	1	0	1	1	1
49	q	q	0							0	1	0	1	1	0	0	0
50	r	r	0							0	1	0	0	1	0	0	1
51	s	s	0							0	0	1	1	0	0	1	0
52	t	t	0							0	0	1	0	0	0	1	1
53	u	u	0							0	0	1	1	0	1	0	0
54	v	v	0							0	0	1	0	0	1	0	1
55	w	w	0							0	0	1	0	0	1	1	0
56	x	x	0							0	0	1	1	0	1	1	1
57	y	y	0							0	0	1	1	1	0	0	0
58	z	z	0							0	0	1	0	1	0	0	1
59			0														
60			0														
61			0														
62			0														
63	DEL	DEL	0							0	1	1	1	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

Increasing Binary Sequence

code conversion tables(con't)

RS244A to ASCII

ROM ADDRESS	FUNCTION INPUT EIA SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE	CODE INPUT c_7	c_6	c_4	c_3	c_2	c_1	OUTPUT CC/G	b_7	b_6	b_5	b_4	b_3	b_2	b_1
64	Space	Space	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
65	1	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1
66	2	2	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0
67	3	3	1	0	0	0	0	1	1	1	0	1	1	0	0	1	1
68	4	4	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0
69	5	5	1	0	0	0	1	0	1	1	0	1	1	0	1	0	1
70	6	6	1							1	0	1	1	0	1	1	0
71	7	7	1							1	0	1	1	0	1	1	1
72	8	8	1							1	0	1	1	1	0	0	0
73	9	9	1							1	0	1	1	1	0	0	1
74	EOB	ETX	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1
75	EOR	EOT	1							0	0	0	0	0	1	0	0
76			1														
77			1														
78	&	&	1							1	0	1	0	0	1	1	0
79			1														
80	0	0	1							1	0	1	1	0	0	0	0
81	1	1	1							1	0	1	0	1	1	1	1
82	s	s	1							1	1	1	1	0	0	1	1
83	t	t	1							1	1	1	1	0	1	0	0
84	u	u	1							1	1	1	1	0	1	0	1
85	v	v	1							1	1	1	1	0	1	1	0
86	w	w	1							1	1	1	1	0	1	1	1
87	x	x	1							1	1	1	1	1	0	0	0
88	y	y	1							1	1	1	1	1	0	0	1
89	z	z	1							1	1	1	1	1	0	1	0
90	BS	BS	1							0	0	0	0	1	0	0	0
91	,	,	1							1	0	1	0	1	1	0	0
92			1														
93			1														
94	TAB	HT	1							0	0	0	0	1	0	0	1
95			1														
96	–	-	1	1	0	0	0	0	0	1	0	1	0	1	1	0	1
97	j	j	1	1	0	0	0	0	1	1	1	1	0	1	0	1	0
98	k	k	1							1	1	1	0	1	0	1	1
99	l	l	1							1	1	1	0	1	1	0	0
100	m	m	1							1	1	1	0	1	1	0	1
101	n	n	1							1	1	1	0	1	1	1	0
102	o	o	1							1	1	1	0	1	1	1	1
103	p	p	1							1	1	1	1	0	0	0	0
104	q	q	1							1	1	1	1	0	0	0	1
105	r	r	1							1	1	1	1	0	0	1	0
106			1														
107	%	%	1							1	0	1	0	0	1	0	1
108			1														
109			1														
110			1														
111			1														
112	+	+	1							1	0	1	0	1	0	1	1
113	a	a	1							1	1	1	0	0	0	0	1
114	b	b	1							1	1	1	0	0	0	1	0
115	c	c	1							1	1	1	0	0	0	1	1
116	d	d	1							1	1	1	0	0	1	0	0
117	e	e	1							1	1	1	0	0	1	0	1
118	f	f	1							1	1	1	0	0	1	1	0
119	g	g	1							1	1	1	0	0	1	1	1
120	h	h	1							1	1	1	0	1	0	0	0
121	i	i	1							1	1	1	0	1	0	0	1
122	LC	GS	1							0	0	0	1	1	1	0	1
123	.	.	1							1	0	1	0	1	1	1	0
124	UC	FS	1							0	0	0	1	1	1	0	0
125			1														
126			1														
127	DEL	DEL	1							0	1	1	1	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

Increasing Binary Sequence

MM4221RR/MM5221RR ASCII-7-to-EBCDIC Code Converter

general description

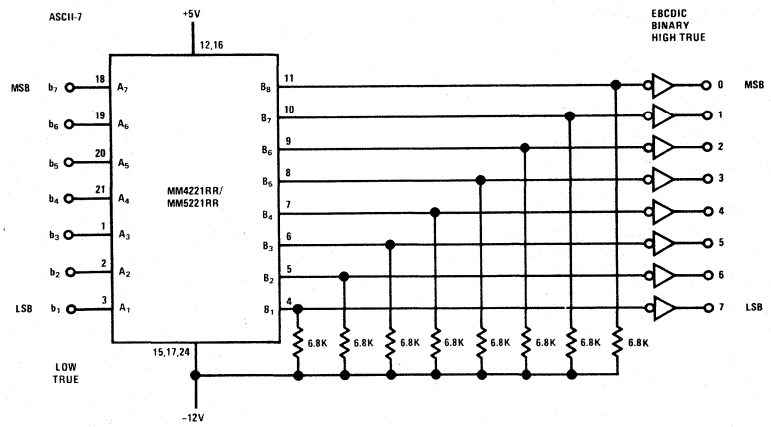
The MM4221RR/MM5221RR is a 1024-bit read-only memory that has been programmed to convert between the 128 characters of ASCII-7, the American Standard Code for Information Interchange in seven bits, and EBCDIC, an extended binary coded decimal interchange code. This conversion follows the EBCDIC character assignments used in the IBM 1130 computer.

Certain arbitrary assignments have also been made for maximum usefulness, and in these two areas the part differs from the MM4230QY/MM5230QY, which follows American National Standard ANSI X3.26 recommendations for character assignments.

For electrical, environmental and mechanical details, refer to the MM4221/MM5221 data sheet.

typical application

ASCII-7 to EBCDIC



Order Number MM4221RR/J or MM5221RR/J
See NS Package J24A

Order Number MM5221RR/N
See NS Package N24B

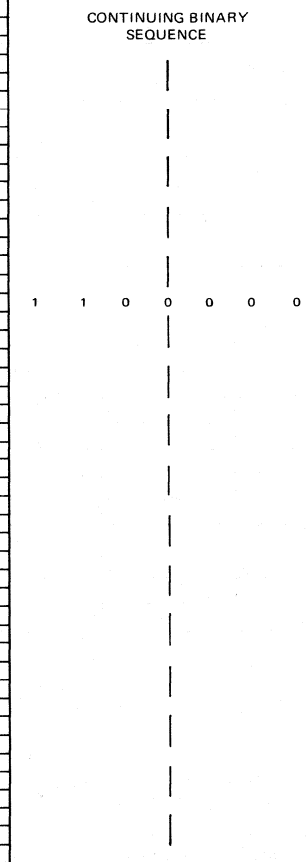
code conversion tables

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT MSB						LSB	CODE OUTPUT MSB							LSB
0	NULL	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	SOH	SOH	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
2	STX	STX	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
3	ETX	ETX	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
4	EOT	EOT	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1
5	ENQ	ENQ	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1
6	ACK	ACK	0	0	0	0	1	1	0	0	0	1	0	1	1	1	0
7	BEL	BEL	0	0	0	0	1	1	1	0	0	1	0	1	1	1	1
8	BS	BS	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0
9	HT	HT	0	0	0	1	0	0	1	0	0	0	0	0	1	0	1
10	LF	LF	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1
11	VT	VT	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1
12	FF	FF	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0
13	CR	CR	0	0	0	1	1	0	1	0	0	0	0	1	1	0	1
14	S0	S0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0
15	S1	S1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
16	DLE	DLE	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
17	DC1	DC1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
18	DC2	DC2								0	0	0	1	0	0	1	0
19	DC3	DC3								0	0	0	1	0	0	1	1
20	DC4	RS								0	0	1	1	0	1	0	1
21	NAK	NAK								0	0	1	1	1	1	0	1
22	SYN	SYN								0	0	1	1	0	0	1	0
23	ETB	EOB								0	0	1	0	0	1	1	0
24	CAN	CAN								0	0	0	1	1	0	0	0
25	EM	EM								0	0	0	1	1	0	0	1
26	SUB	SUB								0	0	1	1	1	1	1	1
27	ESC	BYP								0	0	1	0	0	1	0	0
28	FS	FLS								0	0	0	1	1	1	0	0
29	GS	GS								0	0	0	1	1	1	0	1
30	RS	RDS								0	0	0	1	1	1	1	0
31	US	US								0	0	0	1	1	1	1	1
32	SP	SP	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
33	!	!								0	1	0	1	1	0	1	0
34	"	"								0	1	1	1	1	1	1	1
35	#	#								0	1	1	1	1	0	1	1
36	$	$								0	1	0	1	1	0	1	1
37	%	%								0	1	1	0	1	1	0	0
38	&	&								0	1	0	1	0	0	0	0
39	'	'								0	1	1	1	1	1	0	1
40	(	(								0	1	0	0	1	1	0	1
41	)	)								0	1	0	1	1	1	0	1
42	*	*								0	1	0	1	1	1	0	0
43	+	+								0	1	0	0	1	1	1	0
44	,	,								0	1	1	0	1	0	1	1
45	–	–								0	1	1	0	0	0	0	0
46	.	.								0	1	0	0	1	0	1	1
47	/	/								0	1	1	0	0	0	0	1
48	0	0								1	1	1	1	0	0	0	0
49	1	1								1	1	1	1	0	0	0	1
50	2	2								1	1	1	1	0	0	1	0
51	3	3								1	1	1	1	0	0	1	1
52	4	4								1	1	1	1	0	1	0	0
53	5	5								1	1	1	1	0	1	0	1
54	6	6								1	1	1	1	0	1	1	0
55	7	7								1	1	1	1	0	1	1	1
56	8	8								1	1	1	1	1	0	0	0
57	9	9								1	1	1	1	1	0	0	1
58	:	:								0	1	1	1	1	0	1	0
59	;	;								0	1	0	1	1	1	1	0
60	<	<								0	1	0	0	1	1	0	0
61	=	=								0	1	1	1	1	1	1	0
62	>	>								0	1	1	0	1	1	1	0
63	?	?								0	1	1	0	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

CONTINUING BINARY SEQUENCE

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT MSB						LSB	CODE OUTPUT MSB							LSB
64	@	@	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
65	A	A								1	1	0	0	0	0	0	1
66	B	B								1	1	0	0	0	0	1	0
67	C	C								1	1	0	0	0	0	1	1
68	D	D								1	1	0	0	0	1	0	0
69	E	E								1	1	0	0	0	1	0	1
70	F	F								1	1	0	0	0	1	1	0
71	G	G								1	1	0	0	0	1	1	1
72	H	H								1	1	0	0	1	0	0	0
73	I	I								1	1	0	0	1	0	0	1
74	J	J								1	1	0	1	0	0	0	1
75	K	K								1	1	0	1	0	0	1	0
76	L	L								1	1	0	1	0	0	1	1
77	M	M								1	1	0	1	0	1	0	0
78	N	N								1	1	0	1	0	1	0	1
79	O	O								1	1	0	1	0	1	1	0
80	P	P								1	1	0	1	0	1	1	1
81	Q	Q								1	1	0	1	1	0	0	0
82	R	R								1	1	0	1	1	0	0	1
83	S	S								1	1	1	0	0	0	1	0
84	T	T								1	1	1	0	0	0	1	1
85	U	U								1	1	1	0	0	1	0	0
86	V	V								1	1	1	0	0	1	0	1
87	W	W								1	1	1	0	0	1	1	0
88	X	X								1	1	1	0	0	1	1	1
89	Y	Y								1	1	1	0	1	0	0	0
90	Z	Z								1	1	1	0	1	0	0	1
91	[	[								1	0	1	0	1	1	0	1
92	\	NL								0	0	0	1	0	1	0	1
93	]	]								1	0	1	1	1	1	0	1
94	^	¬								0	1	0	1	1	1	1	1
95	_	_								0	1	1	0	1	1	0	1
96	`	RES	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0
97	a	a								1	0	0	0	0	0	0	1
98	b	b								1	0	0	0	0	0	1	0
99	c	c								1	0	0	0	0	0	1	1
100	d	d								1	0	0	0	0	1	0	0
101	e	e								1	0	0	0	0	1	0	1
102	f	f								1	0	0	0	0	1	1	0
103	g	g								1	0	0	0	0	1	1	1
104	h	h								1	0	0	0	1	0	0	0
105	i	i								1	0	0	0	1	0	0	1
106	j	j								1	0	0	1	0	0	0	1
107	k	k								1	0	0	1	0	0	1	0
108	l	l								1	0	0	1	0	0	1	1
109	m	m								1	0	0	1	0	1	0	0
110	n	n								1	0	0	1	0	1	0	1
111	o	o								1	0	0	1	0	1	1	0
112	p	p								1	0	0	1	0	1	1	1
113	q	q								1	0	0	1	1	0	0	0
114	r	r								1	0	0	1	1	0	0	1
115	s	s								1	0	1	0	0	0	1	0
116	t	t								1	0	1	0	0	0	1	1
117	u	u								1	0	1	0	0	1	0	0
118	v	v								1	0	1	0	0	1	0	1
119	w	w								1	0	1	0	0	1	1	0
120	x	x								1	0	1	0	0	1	1	1
121	y	y								1	0	1	0	1	0	0	0
122	z	z								1	0	1	0	1	0	0	1
123	{	{								1	0	0	0	1	0	1	1
124	|	|								0	1	0	0	1	1	1	1
125	}	}								1	0	0	1	1	0	1	1
126	~	¢								0	1	0	0	1	0	1	0
127	DEL	DEL								0	0	0	0	0	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1



National Semiconductor

MM4221TM/MM5221TM, MM3501TL ASCII-6-to-Baudot/Baudot-to-ASCII-6 Code Converter

General Description

These parts are used for hardware code conversion in either direction between communications equipment, using 5-level Baudot code and the more modern ASCII data interchange code.

Electrical Characteristics

For full electrical, environmental and mechanical details, refer to the MM4221/MM5221 or MM3501 data sheets.

							0	0	1	1
							0	1	0	1
BITS	b6	b5	b4	b3	b2	b1	COLUMN / ROW	0	1	2	3
			0	0	0	0	0	SP	0	Nul	P
			0	0	0	1	1	F1	1	A	Q
			0	0	1	0	2	LF	2	B	R
			0	0	1	1	3	F3	3	C	S
			0	1	0	0	4	F4	4	D	T
			0	1	0	1	5	CR	5	E	U
			0	1	1	0	6	SO	6	F	V
			0	1	1	1	7	SI	7	G	W
			1	0	0	0	8	(	8	H	X
			1	0	0	1	9	)	9	I	Y
			1	0	1	0	10	*	:	J	Z
			1	0	1	1	11	+	;	K	([)
			1	1	0	0	12	,	$	L	(£)
			1	1	0	1	13	–	%	M	(])
			1	1	1	0	14	.	&	N	Esc
			1	1	1	1	15	/	'	O	Del

FIGURE 1. ASCII-6 (From ISO Recommendation R646)

Order Number MM4221TM/J or MM5221TM/J
See NS Package J24A

Order Number MM5221TM/N
See NS Package N24B

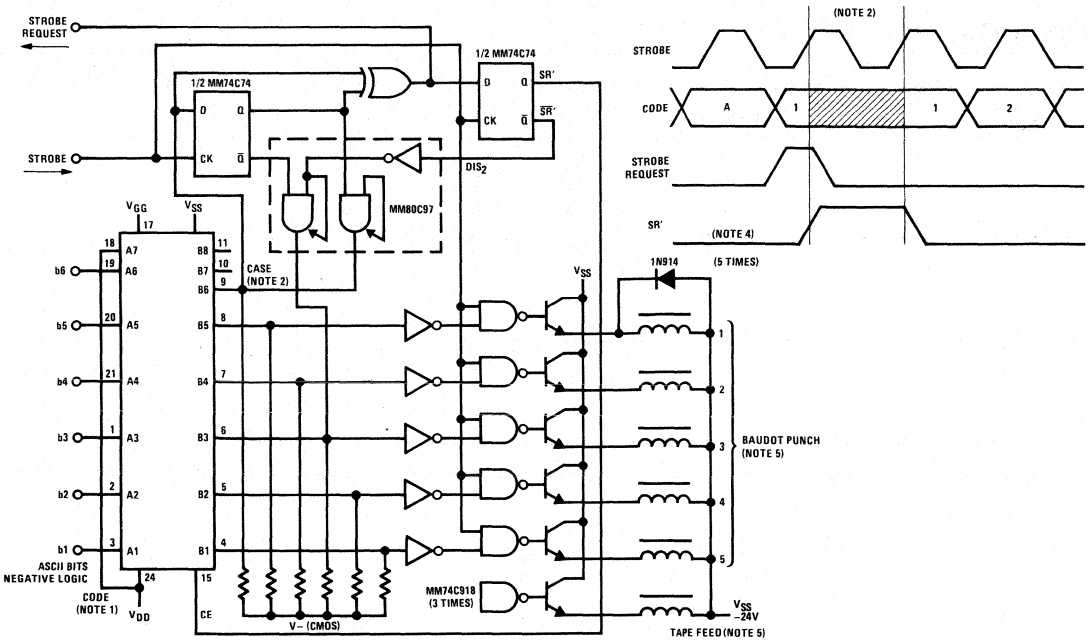


FIGURE 2. ASCII-6 to Baudot Punch

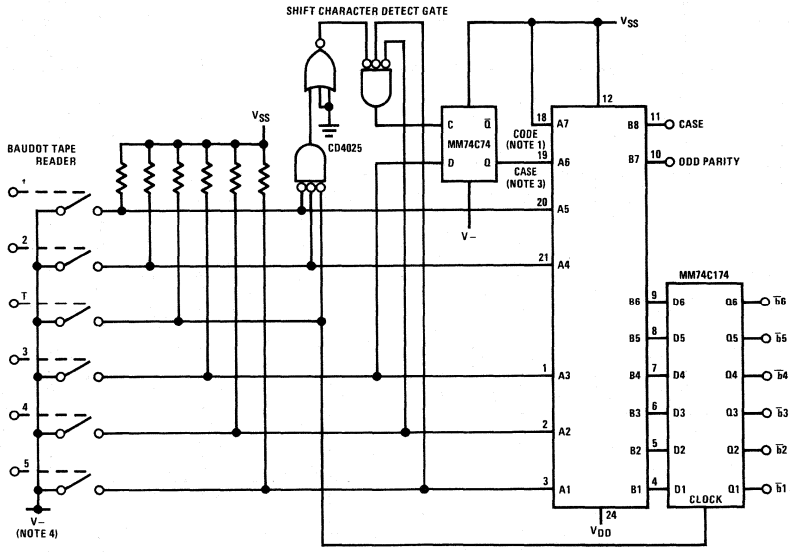


FIGURE 3. Baudot Tape Reader to ASCII-6 Converter

Note 1: CODE line is fixed to a logical "1" (negative supply) to access addresses 64-127, which contain the translation in the desired direction.

Note 2: Where the ASCII-code is to be converted to a Baudot code where the previous character was of unlike case (upper or lower), the case shift character must be inserted in the punch stream, and punched using an extra pulse, generated by the ASCII source machine in response to a "strobe request".

Note 3: Where the ASCII-code is to be converted to a Baudot code where the previous character was of unlike case (upper or lower), the case shift character must be inserted in the punch stream, and punched using an extra strobe pulse, generated by the ASCII source machine in response to a "strobe request". Where the punch must maintain some specific punch rate, the ASCII will be delayed. Where the ASCII is arriving at a specific frequency, the punch must be good enough to permit a momentary doubling of speed, in order to interpose the shift code.

Note 4: SR' disables the ROM allowing all its inputs to be pulled down to V_{DD}, hence generating a code 11111 (lower case shift) $\overline{SR'}$ takes the stored case bit of the code which is being delayed, and puts it on Baudot line B3, so that a code 11011 (upper case shift) will be punched when it is needed. SR' also enables the stored case bit back onto the case line, thus keeping the strobe request line inactive in all cases.

Note 5: The use of the MM74C918 high current emitter follower current source is shown. It will stand off –30V and source 250 mA. Inductors should be shunted by a diode. No Baudot "all zeros" punch is required, so that a simple ratchet advance mechanism may be used. Where a tape feed solenoid must be used, use an MM74C221 dual monostable fired off the trailing edge of STROBE, driving the spare driver.

Code Conversion Table

ROM ADDRESS	FUNCTION INPUT BAUDOT SYMBOL	FUNCTION OUTPUT ASCII-6 SYMBOL	CASE	CODE INPUT BAUDOT 1	2	3	4	5	CASE	P	OUTPUT ASCII B6	B5	B4	B3	B2	B1
0	Blank	Null	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	T	T	0	0	0	0	0	1	0	0	1	1	0	1	0	0
2	CR	CR	0	0	0	0	1	0	0	1	0	0	1	1	0	1
3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1
4	Space	Space	0	0	0	1	0	0	0	1	0	0	0	0	0	0
5	H	H	0	0	0	1	0	1	0	1	1	0	1	0	0	0
6	N	N	0	0	0	1	1	0	0	1	1	0	1	1	1	0
7	M	M	0	0	0	1	1	1	0	1	1	0	1	1	0	1
8	LF	LF	0	0	1	0	0	0	0	0	0	0	1	0	1	0
9	L	L	0	0	1	0	0	1	0	0	1	0	1	1	0	0
10	R	R	0	0	1	0	1	0	0	0	1	1	0	0	1	0
11	G	G	0	0	1	0	1	1	0	1	1	0	0	1	1	1
12	I	I	0	0	1	1	0	0	0	0	1	0	1	0	0	1
13	P	P	0	0	1	1	0	1	0	1	1	1	0	0	0	0
14	C	C	0	0	1	1	1	0	0	0	1	0	0	0	1	1
15	V	V	0	0	1	1	1	1	0	1	1	1	0	1	1	0
16	E	E	0	1	0	0	0	0	0	0	1	0	0	1	0	1
17	Z	Z	0	1	0	0	0	1	0	1	1	1	1	0	1	0
18	D	D	0	1	0	0	1	0	0	1	1	0	0	1	0	0
19	B	B	0	1	0	0	1	1	0	1	1	0	0	0	1	0
20	S	S	0	1	0	1	0	0	0	1	1	1	0	0	1	1
21	Y	Y	0	1	0	1	0	1	0	1	1	1	1	0	0	1
22	F	F	0	1	0	1	1	0	0	0	1	0	0	1	1	0
23	X	X	0	1	0	1	1	1	0	0	1	1	1	0	0	0
24	A	A	0	1	1	0	0	0	0	1	1	0	0	0	0	1
25	W	W	0	1	1	0	0	1	0	0	1	1	0	1	1	1
26	J	J	0	1	1	0	1	0	0	0	1	0	1	0	1	0
27	Upper	F4	0	1	1	0	1	1	0	0	0	1	1	0	0	0
28	U	U	0	1	1	1	0	0	0	1	1	1	0	1	0	1
29	Q	Q	0	1	1	1	0	1	0	0	1	1	0	0	0	1
30	K	K	0	1	1	1	1	0	0	1	1	0	1	0	1	1
31	Lower	Delete	0	1	1	1	1	1	0	1	1	1	1	1	1	1
32	Blank	Null	1	0	0	0	0	0	1	0	1	0	0	0	0	0
33	5	5	1	0	0	0	0	1	1	0	0	1	0	1	0	1
34	CR	CR	1	0	0	0	1	0	1	1	0	0	1	1	0	1
35	9	9	1	0	0	0	1	1	1	0	0	1	1	0	0	1
36	Space	Space	1	0	0	1	0	0	1	1	0	0	0	0	0	0
37	S/S		1	0	0	1	0	1	1	1	0	0	1	0	0	0
38	'	'	1	0	0	1	1	0	1	1	0	0	1	1	0	0
39	,	,	1	0	0	1	1	1	1	0	0	0	1	1	1	0
40	LF	LF	1	0	1	0	0	0	1	0	0	0	1	0	1	0
41	)	)	1	0	1	0	0	1	1	1	0	0	1	0	0	1
42	4	4	1	0	1	0	1	0	1	1	0	1	0	1	0	0
43	&	&	1	0	1	0	1	1	1	1	0	0	0	1	1	0
44	8	8	1	0	1	1	0	0	1	1	0	1	1	0	0	0
45	0	0	1	0	1	1	0	1	1	0	0	1	0	0	0	0
46	:	:	1	0	1	1	1	0	1	0	0	1	1	0	1	0
47	;	;	1	0	1	1	1	1	1	1	0	1	1	0	1	1
48	3	3	1	1	0	0	0	0	1	0	0	1	0	0	1	1
49	"	"	1	1	0	0	0	1	1	0	1	0	0	0	1	0
50	$	$	1	1	0	0	1	0	1	0	0	0	0	1	0	0
51	?	?	1	1	0	0	1	1	1	0	1	1	1	1	1	1
52	Bell	SI	1	1	0	1	0	0	1	0	0	0	0	1	1	1
53	6	6	1	1	0	1	0	1	1	0	0	1	0	1	1	0
54	!	!	1	1	0	1	1	0	1	0	0	0	0	0	0	1
55	/	/	1	1	0	1	1	1	1	1	0	0	1	1	1	1
56	-	-	1	1	1	0	0	0	1	0	0	0	1	1	0	1
57	2	2	1	1	1	0	0	1	1	1	0	1	0	0	1	0
58	'	'	1	1	1	0	1	0	1	0	0	0	0	1	1	1
59	Upper	F4	1	1	1	0	1	1	1	0	0	1	1	0	0	0
60	7	7	1	1	1	1	0	0	1	1	0	1	0	1	1	1
61	1	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1
62	(	(	1	1	1	1	1	0	1	0	0	0	1	0	0	0
63	Lower	Delete	1	1	1	1	1	1	1	1	1	1	1	1	1	1
64	Space	Space	0	0	0	0	0	0	0	0	0	0	0	0	0	0
65	!	!	0	0	0	0	0	1	0	1	1	1	0	1	1	0
66	LF	LF	0	0	0	0	1	0	0	0	0	0	1	0	0	0
67	F3	Null	0	0	0	0	1	1	0	1	0	0	0	0	0	0
68	F4	Upper	0	0	0	1	0	0	0	1	0	1	1	0	1	1
69	CR	CR	0	0	0	1	0	1	0	0	0	0	0	0	1	0

Code Conversion Table (Continued)

ROM ADDRESS	FUNCTION INPUT BAUDOT SYMBOL	FUNCTION OUTPUT ASCII-6 SYMBOL	CASE	CODE INPUT BAUDOT 1	2	3	4	5	CASE	CODE OUTPUT ASCII P	B6	B5	B4	B3	B2	B1
70	SO	Null	0	0	0	1	1	0	0	1	0	0	0	0	0	0
71	SI	Bell	0	0	0	1	1	1	0	0	1	1	0	1	0	0
72	(	(	0	0	1	0	0	0	0	0	1	1	1	1	1	0
73	)	)	0	0	1	0	0	1	0	0	1	0	1	0	0	1
74	*	S/S	0	0	1	0	1	0	0	0	1	0	0	1	0	1
75	+	Null	0	0	1	0	1	1	0	1	0	0	0	0	0	0
76	,	,	0	0	1	1	0	0	0	0	1	0	0	1	1	0
77	-	-	0	0	1	1	0	1	0	0	1	1	1	0	0	0
78	.	.	0	0	1	1	1	0	0	1	1	0	0	1	1	1
79	/	/	0	0	1	1	1	1	0	0	1	1	0	1	1	1
80	0	0	0	1	0	0	0	0	0	1	1	0	1	1	0	1
81	1	1	0	1	0	0	0	1	0	1	0	0	1	1	0	0
82	2	2	0	1	0	0	1	0	0	1	1	1	1	0	0	1
83	3	3	0	1	0	0	1	1	0	1	1	1	1	0	0	0
84	4	4	0	1	0	1	0	0	0	0	1	0	1	0	1	0
85	5	5	0	1	0	1	0	1	0	1	1	0	0	0	0	1
86	6	6	0	1	0	1	1	0	0	1	1	1	0	1	0	1
87	7	7	0	1	0	1	1	1	0	1	1	1	1	1	0	0
88	8	8	0	1	1	0	0	0	0	0	1	0	1	1	0	0
89	9	9	0	1	1	0	0	1	0	0	1	0	0	0	1	1
90	:	:	0	1	1	0	1	0	0	1	1	0	1	1	1	0
91	;	;	0	1	1	0	1	1	0	0	1	0	1	1	1	1
92	$	$	0	1	1	1	0	0	0	0	1	1	0	0	1	0
93	%	Null	0	1	1	1	0	1	0	1	0	0	0	0	0	0
94	&	&	0	1	1	1	1	0	0	1	1	0	1	0	1	1
95	'	'	0	1	1	1	1	1	0	1	1	1	1	0	1	0
96	Null	Null	1	0	0	0	0	0	1	1	0	0	0	0	0	0
97	A	A	1	0	0	0	0	1	1	1	0	1	1	0	0	0
98	B	B	1	0	0	0	1	0	1	0	0	1	0	0	1	1
99	C	C	1	0	0	0	1	1	1	0	0	0	1	1	1	0
100	D	D	1	0	0	1	0	0	1	1	0	1	0	0	1	0
101	E	E	1	0	0	1	0	1	1	0	0	1	0	0	0	0
102	F	F	1	0	0	1	1	0	1	0	0	1	0	1	1	0
103	G	G	1	0	0	1	1	1	1	0	0	0	1	0	1	1
104	H	H	1	0	1	0	0	0	1	1	0	0	0	1	0	1
105	I	I	1	0	1	0	0	1	1	1	0	0	1	1	0	0
106	J	J	1	0	1	0	1	0	1	0	0	1	1	0	1	0
107	K	K	1	0	1	0	1	1	1	1	0	1	1	1	1	0
108	L	L	1	0	1	1	0	0	1	1	0	0	1	0	0	1
109	M	M	1	0	1	1	0	1	1	0	0	0	0	1	1	1
110	N	N	1	0	1	1	1	0	1	1	0	0	0	1	1	0
111	O	O	1	0	1	1	1	1	1	1	0	0	0	0	1	1
112	P	P	1	1	0	0	0	0	1	0	0	0	1	1	0	1
113	Q	Q	1	1	0	0	0	1	1	1	0	1	1	1	0	1
114	R	R	1	1	0	0	1	0	1	1	0	0	1	0	1	0
115	S	S	1	1	0	0	1	1	1	1	0	1	0	1	0	0
116	T	T	1	1	0	1	0	0	1	0	0	0	0	0	0	1
117	U	U	1	1	0	1	0	1	1	0	0	1	1	1	0	0
118	V	V	1	1	0	1	1	0	1	1	0	0	1	1	1	1
119	W	W	1	1	0	1	1	1	1	0	0	1	1	0	0	1
120	X	X	1	1	1	0	0	0	1	1	0	1	0	1	1	1
121	Y	Y	1	1	1	0	0	1	1	0	0	1	0	1	0	1
122	Z	Z	1	1	1	0	1	0	1	1	0	1	0	0	0	1
123	[	"	1	1	1	0	1	1	1	0	1	1	0	0	0	1
124	£	Null	1	1	1	1	0	0	1	1	0	0	0	0	0	0
125	]	?	1	1	1	1	0	1	1	1	1	1	0	0	1	1
126	Esc	Null	1	1	1	1	1	0	1	1	0	0	0	0	0	0
127	Del	Lower	1	1	1	1	1	1	1	1	1	1	1	1	1	1

National Semiconductor

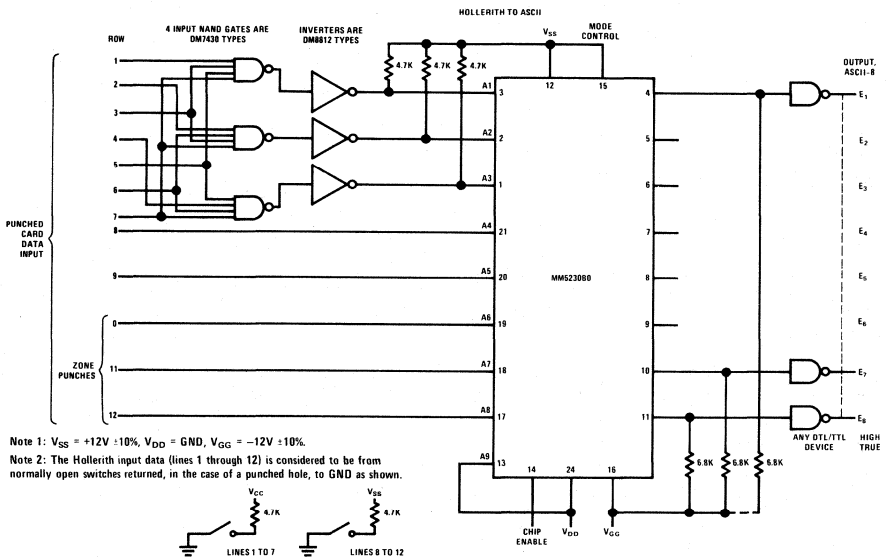
MM4230BO/MM5230BO, MM4231CMU/MM5231CMU Hollerith-to-ASCII Code Converter

general description

The MM4230BO/MM5230BO 2048-bit MOS read-only memory has been programmed to convert the 12 line Hollerith punched card code to eight level ASCII. This conversion conforms to the American National Standard (ANSI x 3.26 – 1970). Three TTL 4-input NAND gates, and three inverters are used to compress the 12 Hollerith lines to eight-line binary encoded form suitable for use by the read-only memory. This application is shown below.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 or the MM4231/MM5231 data sheets.

typical application

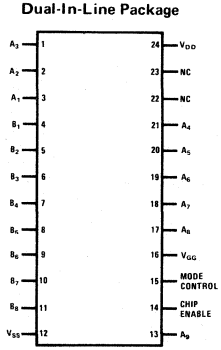


Note 1: V_{SS} = +12V ±10%, V_{DD} = GND, V_{GG} = −12V ±10%.

Note 2: The Hollerith input data (lines 1 through 12) is considered to be from normally open switches returned, in the case of a punched hole, to GND as shown.

connection diagram

Dual-In-Line Package



Order Number MM4230BO/J, MM5230BO/J, MM4231CMU/J or MM5231CMU/J
See NS Package J24A

Order Number MM5230BO/N or MM5231CMU/N
See NS Package N24B

code conversion table

Hollerith to ASCII

	12	11	0		12 0	12 11	11 0	12 11 0	12	11	0		12 0	12 11	11 0	12 11 0	
	&	-	ϕ	SP	{	¦	}	11/10	10/8	11/1	11/9	`	12/3	12/10	13/1	13/8	8-1
1	A	J	/	1	a	j	~	13/9	SOH	DC1	8/1	9/1	10/0	10/9	9/15	11/11	9 -1
2	B	K	S	2	b	k	s	13/10	STX	DC2	8/2	SYN	10/1	10/10	11/2	11/12	9 -2
3	C	L	T	3	c	l	t	13/11	ETX	DC3	8/3	9/3	10/2	10/11	11/3	11/13	9 -3
4	D	M	U	4	d	m	u	13/12	9/12	9/13	8/4	9/4	10/3	10/12	11/4	11/14	9 -4
5	E	N	V	5	e	n	v	13/13	HT	8/5	LF	9/5	10/4	10/13	11/5	11/15	9 -5
6	F	O	W	6	f	o	w	13/14	8/6	BS	ETB	9/6	10/5	10/14	11/6	12/0	9 -6
7	G	P	X	7	g	p	x	13/15	DEL	8/7	ESC	EOT	10/6	10/15	11/7	12/1	9 -7
8	H	Q	Y	8	h	q	y	14/0	9/7	CAN	8/8	9/8	10/7	11/0	11/8	12/2	9 -8
9	I	R	Z	9	i	r	z	14/1	8/13	EM	8/9	9/9	NUL	DLE	8/0	9/0	9-8-1
8-2	[	]	\	:	12/4	12/11	13/2	14/2	8/14	9/2	8/10	9/10	14/8	14/14	15/4	15/10	9-8-2
8-3	.	$	,	#	12/5	12/12	13/3	14/3	VT	8/15	8/11	9/11	14/9	14/15	15/5	15/11	9-8-3
8-4	<	*	%	@	12/6	12/13	13/4	14/4	FF	FS	8/12	DC4	14/10	15/0	15/6	15/12	9-8-4
8-5	(	)	_	'	12/7	12/14	13/5	14/5	CR	GS	ENQ	NAK	14/11	15/1	15/7	15/13	9-8-5
8-6	+	;	>	=	12/8	12/15	13/6	14/6	SO	RS	ACK	9/14	14/12	15/2	15/8	15/14	9-8-6
8-7	! ①	^ ②	?	"	12/9	13/0	13/7	14/7	SI	US	BEL	SUB	14/13	15/3	15/9	15/15	9-8-7

① may be "|"
② may be "¬"

Note: The entries of Form A/B refer to the unassigned locations in the right hand side of the ASII table (bit $E_8 = 1$) designated for specialist use. (See National Bureau of Standards Technical Note No. 478.

Note: For the full ASCII-8 Code Table, see MM4230QY/MM5230QY data sheet.

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National Semiconductor

MM4230FE/MM5230FE Selectric-to-EBCDIC/EBCDIC-to-Selectric Code Converter

general description

The MM4230FE/MM5230FE provides for the conversion of IBM Selectric Correspondence Code to Extended Binary Coded Decimal Interchange Code (EBCDIC) in both directions. These two decoders are contained on a monolithic MOS device.

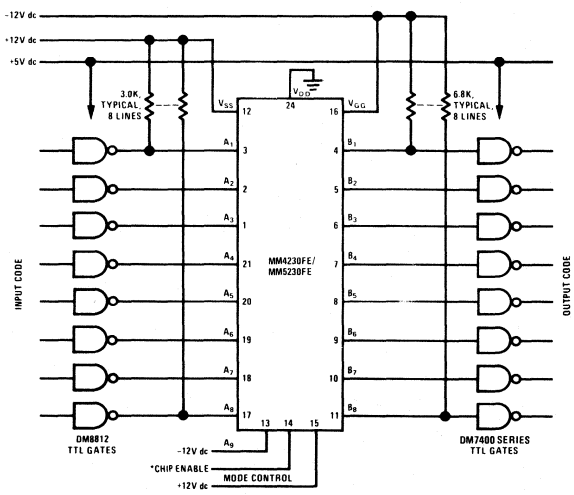
The Selectric-to-EBCDIC converter is located in binary addresses 0 through 127. Input bit A7 is used as a single line command to determine whether upper (denoted by a "1") or a lower (denoted by a "0") case has been selected.

The EBCDIC-to-Selectric converter is located in binary addresses 128 through 255. Since not all EBCDIC control commands have Selectric code counterparts, it is not necessary to encode bit position 0 (A8), which is used instead as the code converter selection bit. In addition to the Selectric Correspondence output code bits there is a bit to indicate upper or lower case. The odd parity bit generated does not account for the case bit.

device characteristics

For full electrical, environmental, and mechanical details refer to the MM4230/MM5230 2048-bit read only memory data sheet.

typical application

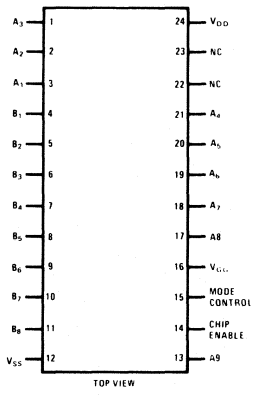


*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4230FE/J or MM5230FE/J
See NS Package J24A

Order Number MM5230FE/N
See NS Package N24B

code conversion table—selectric-to-EBCDIC

ROM ADDRESS	FUNCTION INPUT SELECTRIC SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT CODE	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2	OUTPUT EBCDIC 0	1	2	3	4	5	6	7
0	–	–	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
1	b	b	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0
2	w	w	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	0
3	9	9	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1
4	q	q	0	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0
5	k	k	0	0	0	0	0	1	0	1	1	0	0	1	0	0	1	0
6	i	i	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0	1
7	6	6	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0
8	y	y	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0
9	h	h	0	0	0	0	1	0	0	1	1	0	0	0	1	0	0	0
10	s	s	0	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0
11	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0
12	p	p	0	0	0	0	1	1	0	0	1	0	0	1	0	1	1	1
13	e	e	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	1
14	'	'	0	0	0	0	1	1	1	0	0	1	1	1	1	1	0	1
15	5	5	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	1
16		NULL	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17		NULL	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
18		NULL	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
19		NULL	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
20	=	=	0	0	0	1	0	1	0	0	0	1	1	1	1	1	1	0
21	n	n	0	0	0	1	0	1	0	1	1	0	0	1	0	1	0	1
22	.	.	0	0	0	1	0	1	1	0	0	1	0	0	1	0	1	1
23	2	2	0	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0
24		NULL	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
25		NULL	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0
26		NULL	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
27		NULL	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
28	j	j	0	0	0	1	1	1	0	0	1	0	0	1	0	0	0	1
29	t	t	0	0	0	1	1	1	0	1	1	0	1	0	0	0	1	1
30		NULL	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
31	z	z	0	0	0	1	1	1	1	1	1	0	1	0	1	0	0	1
32		NULL	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33		NULL	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
34		NULL	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
35		NULL	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0
36	,	,	0	0	1	0	0	1	0	0	0	1	1	0	1	0	1	1
37	c	c	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	1
38	a	a	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	1
39	8	8	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0
40	/	/	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1
41	l	l	0	0	1	0	1	0	0	1	1	0	0	1	0	0	1	1
42	o	o	0	0	1	0	1	0	1	0	1	0	0	1	0	1	1	0
43	4	4	0	0	1	0	1	0	1	1	1	1	1	1	0	1	0	0
44	;	;	0	0	1	0	1	1	0	0	0	1	0	1	1	1	1	0
45	d	d	0	0	1	0	1	1	0	1	1	0	0	0	0	1	0	0
46	r	r	0	0	1	0	1	1	1	0	1	0	0	1	1	0	0	1
47	7	7	0	0	1	0	1	1	1	1	1	1	1	1	0	1	1	1
48		NULL	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
49		NULL	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
50		NULL	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
51		NULL	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
52	f	f	0	0	1	1	0	1	0	0	1	0	0	0	0	1	1	0
53	u	u	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0
54	v	v	0	0	1	1	0	1	1	0	1	0	1	0	0	1	0	1
55	3	3	0	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1
56		NULL	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
57		NULL	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0
58		NULL	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
59		NULL	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
60	g	g	0	0	1	1	1	1	0	0	1	0	0	0	0	1	1	1
61	x	x	0	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1
62	m	m	0	0	1	1	1	1	1	0	1	0	0	1	0	1	0	0
63	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

code conversion table—selectric-to-EBCDIC(con't)

ROM ADDRESS	FUNCTION INPUT SELECTRIC SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT CODE	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2	OUTPUT EBCDIC 0	1	2	3	4	5	6	7
64	–	–	0	1	0	0	0	0	0	0	0	1	1	0	1	1	0	1
65	B	B	0	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0
66	W	W	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	0
67	(	(	0	1	0	0	0	0	1	1	0	1	0	0	1	1	0	1
68	Q	Q	0	1	0	0	0	1	0	0	1	1	0	1	1	0	0	0
69	K	K	0	1	0	0	0	1	0	1	1	1	0	1	0	0	1	0
70	I	I	0	1	0	0	0	1	1	0	1	1	0	0	1	0	0	1
71	¢	¢	0	1	0	0	0	1	1	1	0	1	0	0	1	0	1	0
72	Y	Y	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0	0
73	H	H	0	1	0	0	1	0	0	1	1	1	0	0	1	0	0	0
74	S	S	0	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0
75	)	)	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	1
76	P	P	0	1	0	0	1	1	0	0	1	1	0	1	0	1	1	1
77	E	E	0	1	0	0	1	1	0	1	1	1	0	0	0	1	0	1
78	"	"	0	1	0	0	1	1	1	0	0	1	1	1	1	1	1	1
79	%	%	0	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0
80		NULL	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
81		NULL	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0
82		NULL	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
83		NULL	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0
84	+	+	0	1	0	1	0	1	0	0	0	1	0	0	1	1	1	0
85	N	N	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1
86	.	.	0	1	0	1	0	1	1	0	0	1	0	0	1	0	1	1
87	@	@	0	1	0	1	0	1	1	1	0	1	1	1	1	1	0	0
88		NULL	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
89		NULL	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0
90		NULL	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
91		NULL	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0
92	J	J	0	1	0	1	1	1	0	0	1	1	0	1	0	0	0	1
93	T	T	0	1	0	1	1	1	0	1	1	1	1	0	0	0	1	1
94		NULL	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0
95	Z	Z	0	1	0	1	1	1	1	1	1	1	1	0	1	0	0	1
96		NULL	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
97		NULL	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
98		NULL	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
99		NULL	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0
100	,	,	0	1	1	0	0	1	0	0	0	1	1	0	1	0	1	1
101	C	C	0	1	1	0	0	1	0	1	1	1	0	0	0	0	1	1
102	A	A	0	1	1	0	0	1	1	0	1	1	0	0	0	0	0	1
103	*	*	0	1	1	0	0	1	1	1	0	1	0	1	1	1	0	0
104	?	?	0	1	1	0	1	0	0	0	0	1	1	0	1	1	1	1
105	L	L	0	1	1	0	1	0	0	1	1	1	0	1	0	0	1	1
106	O	O	0	1	1	0	1	0	1	0	1	1	0	1	0	1	1	0
107	$	$	0	1	1	0	1	0	1	1	0	1	0	1	1	0	1	1
108	:	:	0	1	1	0	1	1	0	0	0	1	1	1	1	0	1	0
109	D	D	0	1	1	0	1	1	0	1	1	1	0	0	0	1	0	0
110	R	R	0	1	1	0	1	1	1	0	1	1	0	1	1	0	0	1
111	&	&	0	1	1	0	1	1	1	1	0	1	0	1	0	0	0	0
112		NULL	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
113		NULL	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
114		NULL	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
115		NULL	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0
116	F	F	0	1	1	1	0	1	0	0	1	1	0	0	0	1	1	0
117	U	U	0	1	1	1	0	1	0	1	1	1	1	0	0	1	0	0
118	V	V	0	1	1	1	0	1	1	0	1	1	1	0	0	1	0	1
119	#	#	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1
120		NULL	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
121		NULL	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
122		NULL	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
123		NULL	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
124	G	G	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1	1
125	X	X	0	1	1	1	1	1	0	1	1	1	1	0	0	1	1	1
126	M	M	0	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0
127	±	NULL	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

code conversion table—EBCDIC-to-selectric

ROM ADDRESS	FUNCTION INPUT: EBCDIC SYMBOL	FUNCTION OUTPUT: SELECTRIC SYMBOL	CODE INPUT: EBCDIC CODE	1	2	3	4	5	6	7	OUTPUT: PARITY	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2
128	NUL	–	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
129	SOH a	a	1	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0
130	STX b	b	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
131	ETX c	c	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1
132	PF d	d	1	0	0	0	0	1	0	0	1	0	1	0	1	1	0	1
133	HT e	e	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1
134	LC f	f	1	0	0	0	0	1	1	0	0	0	1	1	0	1	0	0
135	DEL g	g	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0
136	h	h	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1
137	i	i	1	0	0	0	1	0	0	1	1	0	0	0	0	1	1	0
138	SMM	–	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
139	VT	–	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0
140	FF	–	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
141	CR	–	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0
142	SO	–	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
143	SI	–	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
144	DLE	–	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
145	DC1 j	j	1	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0
146	DC2 k	k	1	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1
147	TM l	l	1	0	0	1	0	0	1	1	0	0	1	0	1	0	0	1
148	RES m	m	1	0	0	1	0	1	0	0	0	0	1	1	1	1	1	0
149	NL n	n	1	0	0	1	0	1	0	1	0	0	0	1	0	1	0	1
150	BS o	o	1	0	0	1	0	1	1	0	0	0	1	0	1	0	1	0
151	IL p	p	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0
152	CAN q	q	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0
153	EM r	r	1	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0
154	CC	–	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
155	CU1	–	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
156	IFS	–	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
157	IGS	–	1	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0
158	IRS	–	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
159	IUS	–	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
160	DS	–	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
161	SOS	–	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
162	FS s	s	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0
163	t	t	1	0	1	0	0	0	1	1	1	0	0	1	1	1	0	1
164	BYP u	u	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	1
165	LF v	v	1	0	1	0	0	1	0	1	1	0	1	1	0	1	1	0
166	ETB w	w	1	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0
167	ESC x	x	1	0	1	0	0	1	1	1	0	0	1	1	1	1	0	1
168	y	y	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0
169	z	z	1	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1
170	SM	–	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
171	CU2	–	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0
172		–	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
173	ENQ	–	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0
174	ACK	–	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
175	BEL	–	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0
176		–	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
177		–	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
178	SYN	–	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
179		–	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
180	PN	–	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
181	RS	–	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0
182	UC	–	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
183	EOT	–	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0
184		–	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
185		–	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0
186		–	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
187	CU3	–	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
188	DC4	–	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
189	NAK	–	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0
190		–	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0
191	SUB	–	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

code conversion table—EBCDIC-to-selectric(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT SELECTRIC SYMBOL	CODE INPUT EBCDIC CODE	1	2	3	4	5	6	7	OUTPUT PARITY	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2
192	Space	—	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
193	A	A	1	1	0	0	0	0	0	1	0	1	1	0	0	1	1	0
194	B	B	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1
195	C	C	1	1	0	0	0	0	1	1	0	1	1	0	0	1	0	1
196	D	D	1	1	0	0	0	1	0	0	1	1	1	0	1	1	0	1
197	E	E	1	1	0	0	0	1	0	1	0	1	0	0	1	1	0	1
198	F	F	1	1	0	0	0	1	1	0	0	1	1	1	0	1	0	0
199	G	G	1	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0
200	H	H	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1
201	I	I	1	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0
202	¢	¢	1	1	0	0	1	0	1	0	0	1	0	0	0	1	1	1
203	.	.	1	1	0	0	1	0	1	1	0	0	0	1	0	1	1	0
204	<	—	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
205	(	(	1	1	0	0	1	1	0	1	1	1	0	0	0	0	1	1
206	+	+	1	1	0	0	1	1	1	0	1	1	0	1	0	1	0	0
207	!	—	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
208	&	&	1	1	0	1	0	0	0	0	0	1	1	0	1	1	1	1
209	J	J	1	1	0	1	0	0	0	1	0	1	0	1	1	1	0	0
210	K	K	1	1	0	1	0	0	1	0	1	1	0	0	0	1	0	1
211	L	L	1	1	0	1	0	0	1	1	0	1	1	0	1	0	0	1
212	M	M	1	1	0	1	0	1	0	0	0	1	1	1	1	1	1	0
213	N	N	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
214	O	O	1	1	0	1	0	1	1	0	0	1	1	0	1	0	1	0
215	P	P	1	1	0	1	0	1	1	1	1	1	0	0	1	1	0	0
216	Q	Q	1	1	0	1	1	0	0	0	0	1	0	0	0	1	0	0
217	R	R	1	1	0	1	1	0	0	1	1	1	1	0	1	1	1	0
218	!	—	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
219	$	$	1	1	0	1	1	0	1	1	1	1	1	0	1	0	1	1
220	* or *	*	1	1	0	1	1	1	0	0	1	1	1	0	0	1	1	1
221	)	)	1	1	0	1	1	1	0	1	0	1	0	0	1	0	1	1
222	;	;	1	1	0	1	1	1	1	0	0	0	1	0	1	1	0	0
223	¬	—	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0
224	—	—	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
225	/	/	1	1	1	0	0	0	0	1	1	0	1	0	1	0	0	0
226	S	S	1	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0
227	T	T	1	1	1	0	0	0	1	1	1	1	0	1	1	1	0	1
228	U	U	1	1	1	0	0	1	0	0	1	1	1	1	0	1	0	1
229	V	V	1	1	1	0	0	1	0	1	1	1	1	1	0	1	1	0
230	W	W	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0
231	X	X	1	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1
232	Y	Y	1	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0
233	Z	Z	1	1	1	0	1	0	0	1	0	1	0	1	1	1	1	1
234		—	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
235	,	,	1	1	1	0	1	0	1	1	1	0	1	0	0	1	0	0
236	%	%	1	1	1	0	1	1	0	0	1	1	0	0	1	1	1	1
237	- or —	-	1	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0
238	>	—	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0
239	?	?	1	1	1	0	1	1	1	1	1	1	1	0	1	0	0	0
240	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1
241	1	1	1	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1
242	2	2	1	1	1	1	0	0	1	0	1	0	0	1	0	1	1	1
243	3	3	1	1	1	1	0	0	1	1	0	0	1	1	0	1	1	1
244	4	4	1	1	1	1	0	1	0	0	1	0	1	0	1	0	1	1
245	5	5	1	1	1	1	0	1	0	1	1	0	0	0	1	1	1	1
246	6	6	1	1	1	1	0	1	1	0	0	0	0	0	0	1	1	1
247	7	7	1	1	1	1	0	1	1	1	0	0	1	0	1	1	1	1
248	8	8	1	1	1	1	1	0	0	0	1	0	1	0	0	1	1	1
249	9	9	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1
250	:	:	1	1	1	1	1	0	1	0	0	1	1	0	1	1	0	0
251	#	#	1	1	1	1	1	0	1	1	0	1	1	1	0	1	1	1
252	@	@	1	1	1	1	1	1	0	0	1	1	0	1	0	1	1	1
253	'	'	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	0
254	=	=	1	1	1	1	1	1	1	0	1	0	0	1	0	1	0	0
255	"	"	1	1	1	1	1	1	1	1	0	1	0	0	1	1	1	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

National Semiconductor

MM4230JT/MM5230JT BCDIC-to-EBCDIC/EBCDIC-to-BCDIC Code Converter

general description

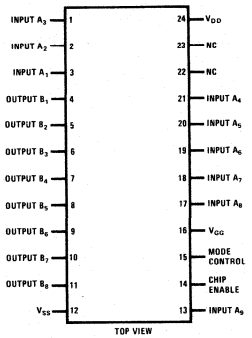
The MM4230JT/MM5230JT is a 2048-bit read-only memory that has been programmed to convert from the 64-entry, 6-bit Binary Coded Decimal Interchange Code (BCDIC) to the eight-bit extended BCD interchange code (EBCDIC) and back again. The tables show the two translations in binary.

Character assignments for the EBCDIC are given to IBM1130 specifications. All the non-alphanumeric assignments in BCDIC are subject to specialist usage, and care should be taken over them.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

connection diagram

Dual-In-Line Package

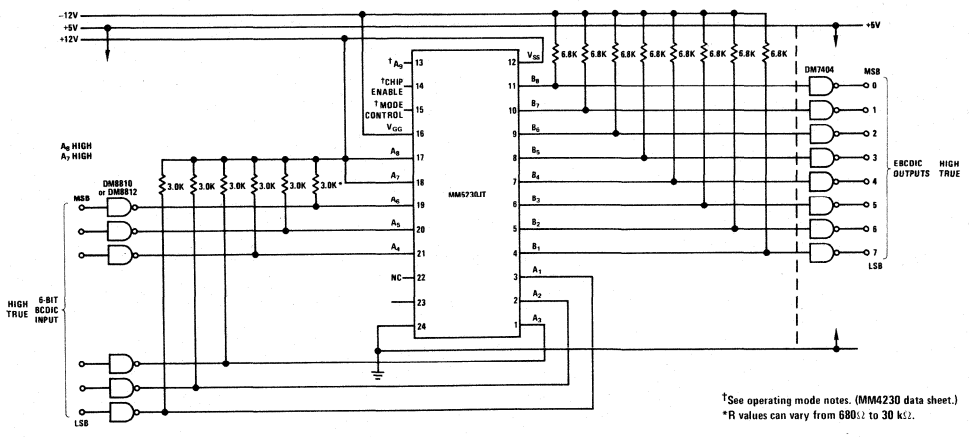


Order Number MM4230JT/J
or MM5230JT/J
See NS Package J24A

Order Number MM5230JT/N
See NS Package N24B

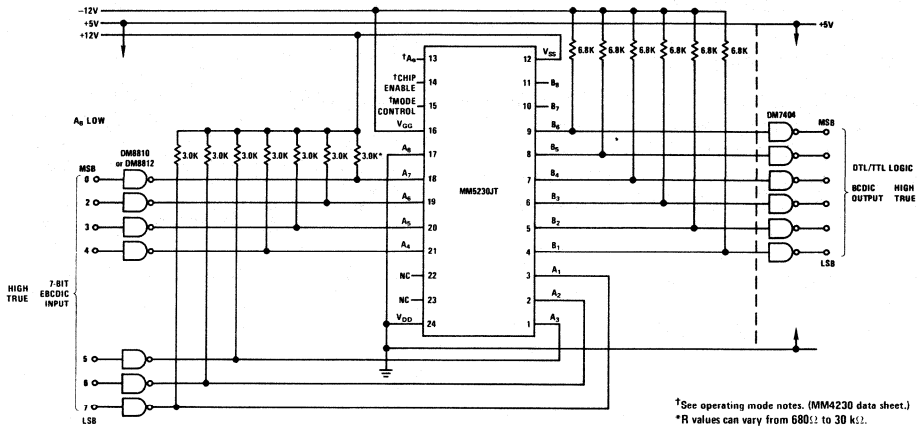
typical applications

BCDIC to EBCDIC



typical applications (con't)

EBCDIC to BCDIC



†See operating mode notes. (MM4230 data sheet.)
*R values can vary from 680Ω to 30 kΩ.

code conversion tables

BCDIC to EBCDIC

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	BCDIC SYMBOL	EBCDIC SYMBOL	EBCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
0	NULL	NULL	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	1
2	2	2	1	1	1	1	0	0	1	0
3	3	3	1	1	1	1	0	0	1	1
4	4	4	1	1	1	1	0	1	0	0
5	5	5	1	1	1	1	0	1	0	1
6	6	6	1	1	1	1	0	1	1	0
7	7	7	1	1	1	1	0	1	1	1
8	8	8	1	1	1	1	1	0	0	0
9	9	9	1	1	1	1	1	0	0	1
10	0	0	1	1	1	1	0	0	0	0
11	#	#	0	1	1	1	1	0	1	1
12	@	@	0	1	1	1	1	1	0	0
13	'	'	0	1	1	1	1	1	0	1
14	=	=	0	1	1	1	1	1	1	0
15	"	"	0	1	1	1	1	1	1	1
16	Space	Space	0	1	0	0	0	0	0	0
17	/	/	0	1	1	0	0	0	0	1
18	S	S	1	1	1	0	0	0	1	0
19	T	T	1	1	1	0	0	0	1	1
20	U	U	1	1	1	0	0	1	0	0
21	V	V	1	1	1	0	0	1	0	1
22	W	W	1	1	1	0	0	1	1	0
23	X	X	1	1	1	0	0	1	1	1
24	Y	Y	1	1	1	0	1	0	0	0
25	Z	Z	1	1	1	0	1	0	0	1
26	NULL	NULL	0	1	0	0	0	0	0	0
27	.	.	0	1	1	0	1	0	1	1
28	%	%	0	1	1	0	1	1	0	0
29	—	—	0	1	1	0	1	1	0	1
30	>	>	0	1	1	0	1	1	1	0
31	?	?	0	1	1	0	1	1	1	1
32	–	–	0	1	1	0	0	0	0	0
33	J	J	1	1	0	1	0	0	0	1
34	K	K	1	1	0	1	0	0	1	0
35	L	L	1	1	0	1	0	0	1	1
36	M	M	1	1	0	1	0	1	0	0
37	N	N	1	1	0	1	0	1	0	1
38	O	O	1	1	0	1	0	1	1	0
39	P	P	1	1	0	1	1	1	1	1
40	Q	Q	1	1	0	1	1	0	0	0
41	R	R	1	1	0	1	1	0	0	1
42	!	!	0	1	0	1	1	0	1	0
43	$	$	0	1	0	1	1	0	1	1
44	*	*	0	1	0	1	1	1	0	0
45	)	)	0	1	0	1	1	1	0	1
46	;	;	0	1	0	1	1	1	1	0
47	¬	¬	0	1	0	1	1	1	1	1
48	&	&	0	1	0	1	0	0	0	0
49	A	A	1	1	0	0	0	0	0	1
50	B	B	1	1	0	0	0	0	1	0
51	C	C	1	1	0	0	0	0	1	1
52	D	D	1	1	0	0	0	1	0	0
53	E	E	1	1	0	0	0	1	0	1
54	F	F	1	1	0	0	0	1	1	0
55	G	G	1	1	0	0	0	1	1	1
56	H	H	1	1	0	0	1	0	0	0
57	I	I	1	1	0	0	1	0	0	1
58	¢	¢	0	1	0	0	1	0	1	0
59	.	.	0	1	0	0	1	0	1	1
60	<	<	0	1	0	0	1	1	0	0
61	(	(	0	1	0	0	1	1	0	1
62	+	+	0	1	0	0	1	1	1	0
63	!	!	0	1	0	0	1	1	1	1

code conversion tables(con't)

BCDIC to EBCDIC (con't)

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	BCDIC	EBCDIC	EBCDIC							
	SYMBOL	SYMBOL	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
64	0	0	1	1	1	1	0	0	0	0
65	1	1	1	1	1	1	0	0	0	1
66	2	2	1	1	1	1	0	0	1	0
67	3	3	1	1	1	1	0	0	1	1
68	4	4	1	1	1	1	0	1	0	0
69	5	5	1	1	1	1	0	1	0	1
70	6	6	1	1	1	1	0	1	1	0
71	NULL	NULL	0	0	0	0	0	0	0	0
72	7	7	1	1	1	1	0	1	1	1
73	8	8	1	1	1	1	1	0	0	0
74	9	9	1	1	1	1	1	0	0	1
75	NULL	NULL	0	0	0	0	0	0	0	0
76	NULL	NULL	0	0	0	0	0	0	0	0
77	NULL	NULL	0	0	0	0	0	0	0	0
78	NULL	NULL	0	0	0	0	0	0	0	0
79	NULL	NULL	0	0	0	0	0	0	0	0
80	NULL	NULL	0	0	0	0	0	0	0	0
81	NULL	NULL	0	0	0	0	0	0	0	0
82	NULL	NULL	0	0	0	0	0	0	0	0
83	NULL	NULL	0	0	0	0	0	0	0	0
84	NULL	NULL	0	0	0	0	0	0	0	0
85	NULL	NULL	0	0	0	0	0	0	0	0
86	NULL	NULL	0	0	0	0	0	0	0	0
87	NULL	NULL	0	0	0	0	0	0	0	0
88	NULL	NULL	0	0	0	0	0	0	0	0
89	NULL	NULL	0	0	0	0	0	0	0	0
90	NULL	NULL	0	0	0	0	0	0	0	0
91	NULL	NULL	0	0	0	0	0	0	0	0
92	NULL	NULL	0	0	0	0	0	0	0	0
93	NULL	NULL	0	0	0	0	0	0	0	0
94	NULL	NULL	0	0	0	0	0	0	0	0
95	NULL	NULL	0	0	0	0	0	0	0	0
96	NULL	NULL	0	0	0	0	0	0	0	0
97	NULL	NULL	0	0	0	0	0	0	0	0
98	NULL	NULL	0	0	0	0	0	0	0	0
99	NULL	NULL	0	0	0	0	0	0	0	0
100	NULL	NULL	0	0	0	0	0	0	0	0
101	NULL	NULL	0	0	0	0	0	0	0	0
102	NULL	NULL	0	0	0	0	0	0	0	0
103	NULL	NULL	0	0	0	0	0	0	0	0
104	NULL	NULL	0	0	0	0	0	0	0	0
105	NULL	NULL	0	0	0	0	0	0	0	0
106	NULL	NULL	0	0	0	0	0	0	0	0
107	NULL	NULL	0	0	0	0	0	0	0	0
108	NULL	NULL	0	0	0	0	0	0	0	0
109	NULL	NULL	0	0	0	0	0	0	0	0
110	NULL	NULL	0	0	0	0	0	0	0	0
111	NULL	NULL	0	0	0	0	0	0	0	0
112	NULL	NULL	0	0	0	0	0	0	0	0
113	NULL	NULL	0	0	0	0	0	0	0	0
114	NULL	NULL	0	0	0	0	0	0	0	0
115	NULL	NULL	0	0	0	0	0	0	0	0
116	NULL	NULL	0	0	0	0	0	0	0	0
117	NULL	NULL	0	0	0	0	0	0	0	0
118	NULL	NULL	0	0	0	0	0	0	0	0
119	NULL	NULL	0	0	0	0	0	0	0	0
120	NULL	NULL	0	0	0	0	0	0	0	0
121	NULL	NULL	0	0	0	0	0	0	0	0
122	NULL	NULL	0	0	0	0	0	0	0	0
123	NULL	NULL	0	0	0	0	0	0	0	0
124	NULL	NULL	0	0	0	0	0	0	0	0
125	NULL	NULL	0	0	0	0	0	0	0	0
126	NULL	NULL	0	0	0	0	0	0	0	0
127	NULL	NULL	0	0	0	0	0	0	0	0

code conversion tables(con't)

EBCDIC to BCDIC

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	EBCDIC SYMBOL	BCDIC SYMBOL	BCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
128	NULL	NULL	0	0	0	0	0	0	0	0
129	NULL	NULL	0	0	0	0	0	0	0	0
130	NULL	NULL	0	0	0	0	0	0	0	0
131	NULL	NULL	0	0	0	0	0	0	0	0
132	NULL	NULL	0	0	0	0	0	0	0	0
133	–	–	0	0	0	1	0	0	0	0
134	–	–	0	0	0	1	0	0	0	0
135	NULL	NULL	0	0	0	0	0	0	0	0
136	NULL	NULL	0	0	0	0	0	0	0	0
137	–	–	0	0	0	1	0	0	0	0
138	¢	¢	0	0	1	1	1	0	1	0
139	.	.	0	0	1	1	1	0	1	1
140	<	<	0	0	1	1	1	1	0	0
141	(	(	0	0	1	1	1	1	0	1
142	+	+	0	0	1	1	1	1	1	0
143	|	|	0	0	1	1	1	1	1	1
144	&	&	0	0	1	1	0	0	0	0
145	NULL	NULL	0	0	0	0	0	0	0	0
146	NULL	NULL	0	0	0	0	0	0	0	0
147	NULL	NULL	0	0	0	0	0	0	0	0
148	NULL	NULL	0	0	0	0	0	0	0	0
149	–	–	0	0	0	1	0	0	0	0
150	–	–	0	0	0	1	0	0	0	0
151	NULL	NULL	0	0	0	0	0	0	0	0
152	NULL	NULL	0	0	0	0	0	0	0	0
153	!	!	0	0	0	0	0	0	0	0
154	$	$	0	0	1	0	1	0	1	0
155	*	*	0	0	1	0	1	0	1	1
156	)	)	0	0	1	0	1	1	0	0
157	;	;	0	0	1	0	1	1	0	1
158	¬	¬	0	0	1	0	1	1	1	0
159	–	–	0	0	1	0	1	1	1	1
160	/	/	0	0	1	0	0	0	0	0
161	⌟	⌟	0	0	0	1	0	0	0	1
162	NULL	NULL	0	0	0	0	0	0	0	0
163	NULL	NULL	0	0	0	0	0	0	0	0
164	NULL	NULL	0	0	0	0	0	0	0	0
165	NULL	NULL	0	0	0	0	0	0	0	0
166	NULL	NULL	0	0	0	0	0	0	0	0
167	NULL	NULL	0	0	0	0	0	0	0	0
168	NULL	NULL	0	0	0	0	0	0	0	0
169	NULL	NULL	0	0	0	0	0	0	0	0
170	NULL	NULL	0	0	0	0	0	0	0	0
171	,	,	0	0	0	1	1	0	1	1
172	%	%	0	0	0	1	1	1	0	0
173	–	–	0	0	0	1	1	1	0	1
174	>	>	0	0	0	1	1	1	1	0
175	?	?	0	0	0	1	1	1	1	1
176	NULL	NULL	0	0	0	0	0	0	0	0
177	NULL	NULL	0	0	0	0	0	0	0	0
178	NULL	NULL	0	0	0	0	0	0	0	0
179	NULL	NULL	0	0	0	0	0	0	0	0
180	NULL	NULL	0	0	0	0	0	0	0	0
181	–	–	0	0	0	1	0	0	0	0
182	–	–	0	0	0	1	0	0	0	0
183	NULL	NULL	0	0	0	0	0	0	0	0
184	NULL	NULL	0	0	0	0	0	0	0	0
185	NULL	NULL	0	0	0	0	0	0	0	0
186	:	:	0	0	0	0	0	0	0	0
187	#	#	0	0	0	0	1	0	1	1
188	@	@	0	0	0	0	1	1	0	0
189	'	'	0	0	0	0	1	1	0	1
190	=	=	0	0	0	0	1	1	1	0
191	"	"	0	0	0	0	1	1	1	1

code conversion tables(con't)

EBCDIC to BCDIC (con't)

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	EBCDIC SYMBOL	BCDIC SYMBOL	BCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
192	_	_	0	0	0	1	0	0	0	0
193	A	A	0	0	1	1	0	0	0	1
194	B	B	0	0	1	1	0	0	1	0
195	C	C	0	0	1	1	0	0	1	1
196	D	D	0	0	1	1	0	1	0	0
197	E	E	0	0	1	1	0	1	0	1
198	F	F	0	0	1	1	0	1	1	0
199	G	G	0	0	1	1	0	1	1	1
200	H	H	0	0	1	1	1	0	0	0
201	I	I	0	0	1	1	1	0	0	1
202	NULL	NULL	0	0	0	0	0	0	0	0
203	NULL	NULL	0	0	0	0	0	0	0	0
204	NULL	NULL	0	0	0	0	0	0	0	0
205	NULL	NULL	0	0	0	0	0	0	0	0
206	NULL	NULL	0	0	0	0	0	0	0	0
207	NULL	NULL	0	0	0	0	0	0	0	0
208	NULL	NULL	0	0	0	0	0	0	0	0
209	J	J	0	0	1	0	0	0	0	1
210	K	K	0	0	1	0	0	0	1	0
211	L	L	0	0	1	0	0	0	1	1
212	M	M	0	0	1	0	0	1	0	0
213	N	N	0	0	1	0	0	1	0	1
214	O	O	0	0	1	0	0	1	1	0
215	P	P	0	0	1	0	0	1	1	1
216	Q	Q	0	0	1	0	1	0	0	0
217	R	R	0	0	1	0	1	0	0	1
218	NULL	NULL	0	0	0	0	0	0	0	0
219	NULL	NULL	0	0	0	0	0	0	0	0
220	NULL	NULL	0	0	0	0	0	0	0	0
221	NULL	NULL	0	0	0	0	0	0	0	0
222	NULL	NULL	0	0	0	0	0	0	0	0
223	NULL	NULL	0	0	0	0	0	0	0	0
224	NULL	NULL	0	0	0	0	0	0	0	0
225	NULL	NULL	0	0	0	0	0	0	0	0
226	S	S	0	0	0	1	0	0	1	0
227	T	T	0	0	0	1	0	0	1	1
228	U	U	0	0	0	1	0	1	0	0
229	V	V	0	0	0	1	0	1	0	1
230	W	W	0	0	0	1	0	1	1	0
231	X	X	0	0	0	1	0	1	1	1
232	Y	Y	0	0	0	1	1	0	0	0
233	Z	Z	0	0	0	1	1	0	0	1
234	NULL	NULL	0	0	0	0	0	0	0	0
235	NULL	NULL	0	0	0	0	0	0	0	0
236	NULL	NULL	0	0	0	0	0	0	0	0
237	NULL	NULL	0	0	0	0	0	0	0	0
238	NULL	NULL	0	0	0	0	0	0	0	0
239	NULL	NULL	0	0	0	0	0	0	0	0
240	0	0	0	0	0	0	1	0	1	0
241	1	1	0	0	0	0	0	0	0	1
242	2	2	0	0	0	0	0	0	1	0
243	3	3	0	0	0	0	0	0	1	1
244	4	4	0	0	0	0	0	1	0	0
245	5	5	0	0	0	0	0	1	0	1
246	6	6	0	0	0	0	0	1	1	0
247	7	7	0	0	0	0	0	1	1	1
248	8	8	0	0	0	0	1	0	0	0
249	9	9	0	0	0	0	1	0	0	1
250	NULL	NULL	0	0	0	0	0	0	0	0
251	NULL	NULL	0	0	0	0	0	0	0	0
252	NULL	NULL	0	0	0	0	0	0	0	0
253	NULL	NULL	0	0	0	0	0	0	0	0
254	NULL	NULL	0	0	0	0	0	0	0	0
255	NULL	NULL	0	0	0	0	0	0	0	0

National Semiconductor

MM4230KP/MM5230KP
ASCII-7-to-Selectric Code Converter

general description

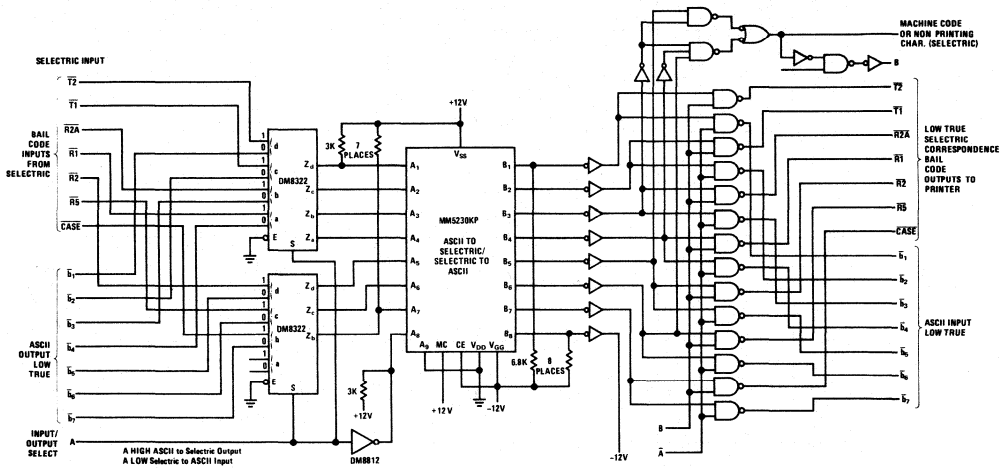
The MM4230KP/MM5230KP MOS read-only memory has been programmed to perform the conversion between the American Standard Code for Information Interchange in seven bits (ASCII) and the Selectric correspondence bail code transmitted and received by the IBM Series 7 input/output printers.

application hints

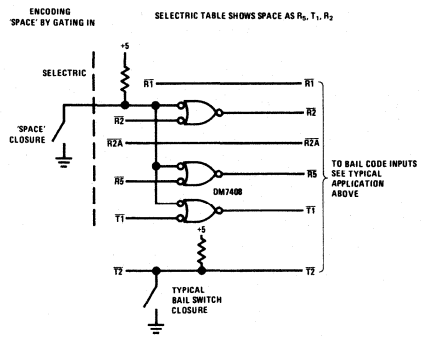
The ASCII field and Selectric bail code field as defined do not map exactly: for instance "space" is handled as a normal 7-bit code in ASCII, but is handled as a unique switch and solenoid pair in the Selectric printer. And even among the graphic characters, ± and ¢ exist only for Selectric, and > and < only for ASCII. The former problem is handled in the MM4230KP/MM5230KP by exploiting the inherent redundancy of the bail code (see Table 2). The latter inconsistency is resolved by making arbitrary equivalences between the unique characters. The two tables show the treatment of both the characters which have equivalents in both codes, and those characters, and the functions, which do not. Encoding and decoding the Selectric functions that the user requires is a matter of conventional Boolean logic. A typical example is shown below.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

typical applications

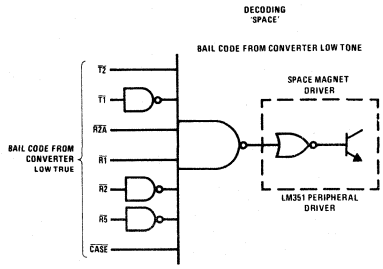


Encoding 'Space' by Gating In on Input



Order Number MM4230KP/J or MM5230KP/J
See NS Package J24A

Decoding 'Space' on Output



Order Number MM5230KP/N
See NS Package N24B

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code conversion tables

Table 1. ASCII-7 to Selectric

b_4	b_3	b_2	b_1	Row ↓ / Column →	0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)
0	0	0	0	0	NUL 02	DLE 0A	SP 62	0	@	P	` 25	p
0	0	0	1	1	SOH 12	DCI IA	!	1	A	Q	a	q
0	0	1	0	2	STX 22	DC2 2A	"	2	B	R	b	r
0	0	1	1	3	ETX 32	DC3 3A	#	3	C	S	c	s
0	1	0	0	4	EOT 03	DC4 0B	$	4	D	T	d	t
0	1	0	1	5	ENQ 13	NAK 1B	%	5	E	U	e	u
0	1	1	0	6	ACK 23	SYN 2B	&	6	F	V	f	v
0	1	1	1	7	BEL 33	ETB 3B	' 25	7	G	W	g	w
1	0	0	0	8	BS 42	CAN 4A	(	8	H	X	h	x
1	0	0	1	9	HT 52	EM 5A	)	9	I	Y	i	y
1	0	1	0	A	LF 53	SUB 6A	*	:	J	Z	j	z
1	0	1	1	B	VT 72	ESC 7A	+	;	K	[7F	k	{ 7F
1	1	0	0	C	FF 72	FS 4B	,	< 40	L	\ 60	l	¦ 48
1	1	0	1	D	CR 53	GS 5B	–	=	M	] 77	m	} 77
1	1	1	0	E	SO 63	RS 6B	.	> 50	N	^ 70	n	~ 58
1	1	1	1	F	SI 73	US 7B	/	?	O	_	o	DEL 00

code conversion tables (con't)

Table 2. Selectric to ASCII-7

R_5 → T_1 → T_2 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
S ↓	R_{2A} ↓	R_2 ↓	R_1 ↓	Row → / Column →	0	1	2	3	4	5	6	7
0	0	0	0	0	¯ 2/D	b	w	9	< 3/C	> 3/E	\ 5/C	^ 5/E
0	0	0	1	1	y	h	s	0 3/0	/	! 6/C	° 6/F	4
0	0	1	0	2	NUL 0/0	SOH 0/1	STX 0/2	ETX 0/3	BS 0/8	TAB 0/9	SP 2/0	IND 0/A
0	0	1	1	3	EOT C/4	ENQ 0/5	ACK 0/6	BELL 0/7		CR 0/D	SO 0/E	SI 0/F
0	1	0	0	4	Q	k	i	6	' 2/C	c	a	8
0	1	0	1	5	P	e	' 2/7	5	; 3/B	d	r	7
0	1	1	0	6	= 3/D	n	. 2/E	2	f	u	v	3
0	1	1	1	7	J	t	½! 2/1	z	g	x	m	1
1	0	0	0	8	_	B	W	(	{ 7/C	~ 7/E		
1	0	0	1	9	Y	H	S	)	?	L	o 4/F	$
1	0	1	0	A	DLE 1/0	DC1 1/1	DC2 1/2	DC3 1/3	CAN 1/8	EM 1/9	SUB 1/A	ESC 1/B
1	0	1	1	B	DC4 1/4	NAK 1/5	SYN 1/6	ETB 1/7	FS 1/C	GS 1/0	RS 1/E	US 1/F
1	1	0	0	C	Q	K	! 4/9	¢ 6/3	, 2/C	C	A	*
1	1	0	1	D	P	E	"	%	:	D	R	&
1	1	1	0	E	+	N	. 2/E	@	F	U	V	#
1	1	1	1	F	J	T	¼° F/F	Z	G	X	M	±[5/B

Entries Thus are Redundant Bail Codes

ASCII shown thus: Column No./Row No.

National Semiconductor

MM4230QW/MM5230QW Hollerith-to-EBCDIC Code Converter

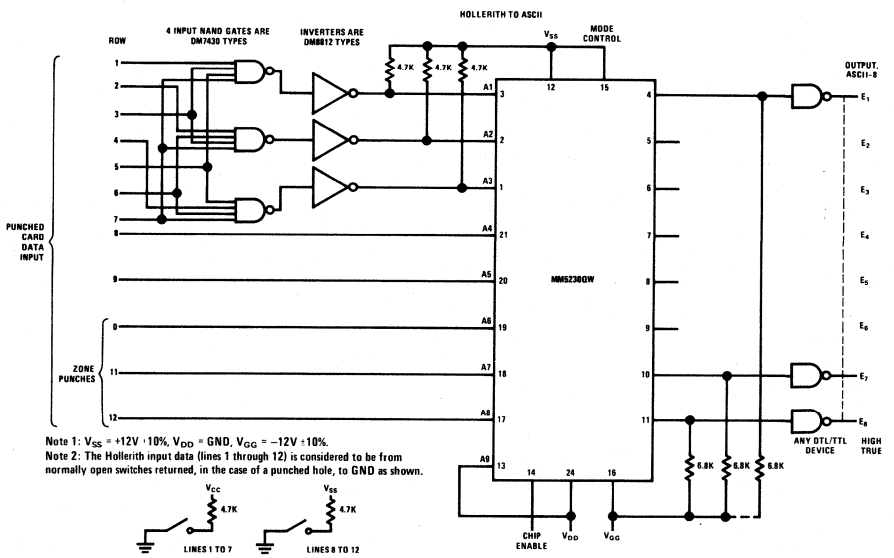
general description

The MM4230QW/MM5230QW 2048-bit MOS read only memory has been programmed to convert the 12 line Hollerith Code to the 8 line EBCDIC Code. Three TTL 4-input NAND gates and three TTL inverters are used to compress the 12 Hollerith lines to eight line binary encoded form suitable for use by the ROM.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

typical application

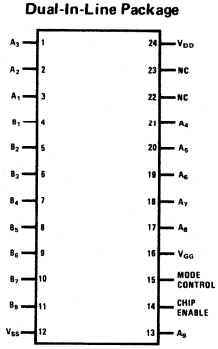
Hollerith to EBCDIC



Note 1: V_{SS} = +12V ±10%, V_{DD} = GND, V_{GG} = −12V ±10%.
Note 2: The Hollerith input data (lines 1 through 12) is considered to be from normally open switches returned, in the case of a punched hole, to GND as shown.

connection diagram

Dual-In-Line Package



Order Number MM4230QW/J or MM5230QW/J
See NS Package J24A

Order Number MM5230QW/N
See NS Package N24B

code conversion table

Hollerith to EBCDIC

	12	11	0		12 0	12 11	11 0	12 11 0	12	11	0		12 0	12 11	11 0	12 11 0	
	&	-	ϕ	SP	{	¦	}	70	49	59	69	`	80	90	A0	B0	8-1
1	A	J	/	1	a	j	~	B1	SOH	DC1	21	31	41	51	E1	71	9 -1
2	B	K	S	2	b	k	s	B2	STX	DC2	22	SYN	42	52	62	72	9 -2
3	C	L	T	3	c	l	t	B3	ETX	DC3	23	33	43	53	63	73	9 -3
4	D	M	U	4	d	m	u	B4	04	14	24	34	44	54	64	74	9 -4
5	E	N	V	5	e	n	v	B5	HT	15	LF	35	45	55	65	75	9 -5
6	F	O	W	6	f	o	w	B6	06	BS	ETB	36	46	56	66	76	9 -6
7	G	P	X	7	g	p	x	B7	DEL	17	ESC	EOT	47	57	67	77	9 -7
8	H	Q	Y	8	h	q	y	B8	08	CAN	28	38	48	58	68	78	9 -8
9	I	R	Z	9	i	r	z	B9	09	EM	29	39	NUL	DLE	20	30	9-8-1
8-2	[	]	\	:	8A	9A	AA	BA	0A	1A	2A	3A	CA	DA	EA	FA	9-8-2
8-3	.	$	,	#	8B	9B	AB	BB	VT	1B	2B	3B	CB	DB	EB	FB	9-8-3
8-4	<	*	%	@	8C	9C	AC	BC	FF	FS	2C	DC4	CC	DC	EC	FC	9-8-4
8-5	(	)	–	'	8D	9D	AD	BD	CR	GS	ENQ	NAK	CD	DD	ED	FD	9-8-5
8-6	+	;	>	=	8E	9E	AE	BE	SO	RS	ACK	3E	CE	DE	EE	FE	9-8-6
8-7	! ①	^ ②	?	"	8F	9F	AF	BF	SI	US	BEL	SUB	CF	DF	EF	FF	9-8-7

① may be "|"
② may be "¬"

Note: Unassigned entries e.g. AF refer to the EBCDIC code as a 16 x 16 table, column then row, in hexidecimal notation.
Note: The relationship between Hollerith as 256 valid punch combinations and EBCDIC as eight binary digits is well established. This converter conforms to this practice. The assignments shown in the table above are the recommendations of the American National Standards Institute. For details on alternate non-alphanumeric graphic and control codes, see ANSI x 3.26 – 1970.

National Semiconductor

MM4230QX/MM5230QX EBCDIC-8-to-ASCII-8 Code Converter

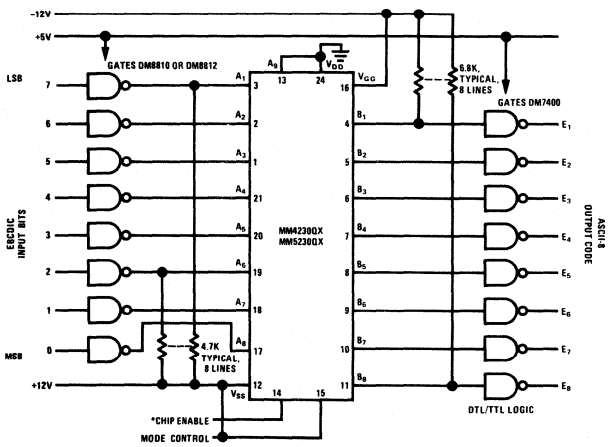
general description

The MM4230QX/MM5230QX is a 2048-bit read only memory that has been programmed to convert Extended Binary Coded Decimal Interchange Code (EBCDIC) to the American Standard Code for Information Interchange extended to eight bits (ASCII-8).

The conversion conforms to the practice established by the American National Standard ANSIx 3.26–1970. Exact details are shown in the code table.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 2048-bit read only memory data sheet.

typical application

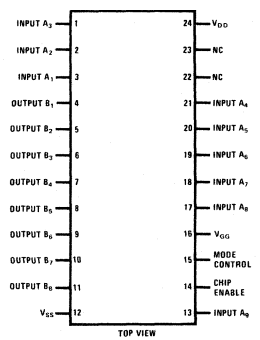


*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

connection diagram

Dual-In-Line Package

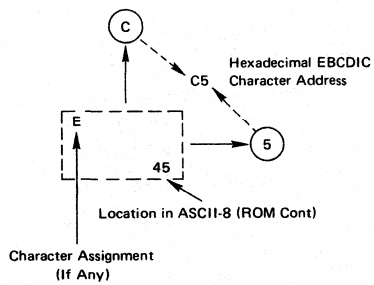


Order Number MM4230QX/J or MM5230QX/J
See NS Package J24A

Order Number MM5230QX/N
See NS Package N24B

code conversion table

4 5 6 7	Column → / Row ↓	0 (0 0 0 0)	1 (0 0 0 1)	2 (0 0 1 0)	3 (0 0 1 1)	4 (0 1 0 0)	5 (0 1 0 1)	6 (0 1 1 0)	7 (0 1 1 1)	8 (1 0 0 0)	9 (1 0 0 1)	A (1 0 1 0)	B (1 0 1 1)	C (1 1 0 0)	D (1 1 0 1)	E (1 1 1 0)	F (1 1 1 1)	
0 0 0 0	0	NUL 00	DLE 10	80	90	SP 20	& 26	– 2D	BA	C3	CA	D1	D8	| 7B	| 7D	\ 5C	0 30	0
0 0 0 1	1	SOH 01	DC1 11	81	91	A0	A9	/ 2F	BB	a 61	i 6A	~ 7E	D9	A 41	J 4A	9F	1 31	1
0 0 1 0	2	STX 02	DC2 12	82	SYN 16	A1	AA	B2	BC	b 62	k 6B	s 73	DA	B 42	K 4B	S 53	2 32	2
0 0 1 1	3	ETX 03	DC3 13	83	93	A2	AB	B3	BD	c 63	l 6C	t 74	DB	C 43	L 4C	T 54	3 33	3
0 1 0 0	4	9C	9D	84	94	A3	AC	B4	BE	d 64	m 6D	u 75	DC	D 44	M 4D	U 55	4 34	4
0 1 0 1	5	HT 09	85	LF 0A	95	A4	AD	B5	BF	e 65	n 6E	v 76	DD	E 45	N 4E	V 56	5 35	5
0 1 1 0	6	86	BS 08	ETB 17	96	A5	AE	B6	C0	f 66	o 6F	w 77	DE	F 46	O 4F	W 57	6 36	6
0 1 1 1	7	DEL 7F	87	ESC 1B	EOT 04	A6	AF	B7	C1	h 67	p 70	x 78	DF	G 47	P 50	X 58	7 37	7
1 0 0 0	8	97	CAN 18	88	98	A7	B0	B8	C2	i 68	q 71	y 79	E0	H 48	Q 51	Y 59	8 38	8
1 0 0 1	9	8D	EM 19	89	99	A8	B1	B9	` 60	' 69	r 72	z 7A	E1	I 49	R 52	Z 5A	9 39	9
1 0 1 0	A	8E	92	8A	9A	[5B	] 5D	; 7C	: 3A	C4	CB	D2	E2	E8	EE	F4	FA	A
1 0 1 1	B	VT 0B	8F	8B	9B	. 2E	$ 24	, 2C	# 23	C5	CC	D3	E3	E9	EF	F5	FB	B
1 1 0 0	C	FF 0C	FS 1C	8C	DC4 14	< 3C	* 2A	% 25	@ 40	C6	CD	D4	E4	EA	F0	F6	FC	C
1 1 0 1	D	CR 0D	GS 1D	ENQ 05	NAK 15	(28	) 29	_ 5F	' 27	C7	CE	D5	E5	EB	F1	F7	FD	D
1 1 1 0	E	SO 0E	RS 1E	ACK 06	9E	+ 2B	: 3B	> 3E	= 3D	C8	CF	D6	E6	EC	F2	F8	FE	E
1 1 1 1	F	SI 0F	US 1F	BEL 07	SUB 1A	! 21	^ 5E	? 3F	" 22	C9	D0	D7	E7	ED	F3	F9	EO FF	F



National Semiconductor

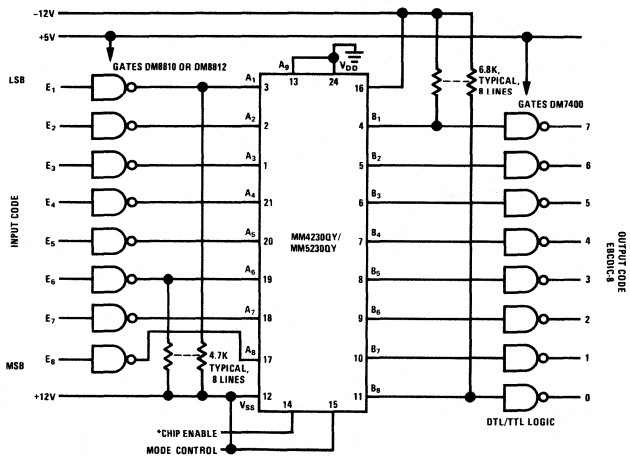
MM4230QY/MM5230QY ASCII-8-to-EBCDIC-8 Code Converter

general description

The MM4230QY/MM5230QY is a 2048-bit read only memory that has been programmed to convert the American Standard Code for Information Interchange extended to eight bits, (ASCII-8) to Extended Binary Coded Decimal Interchange Code (EBCDIC-8). The conversion conforms to the practice established by the American National Standard ANSIx3.26 1970. Exact details are shown in the code table.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 2048-bit read only memory data sheet.

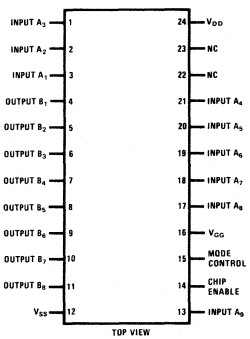
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4230QY/J or MM5230QY/J
See NS Package J24A

Order Number MM5230QY/N
See NS Package N24B

code conversion table

b_4 b_3 b_2 b_1	Row ↓ / Column →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Column ← / Row ↓
	b_8 → 0, b_7 → 0, b_6 → 0, b_5 → 0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
		0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	
		0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
0 0 0 0	0	NUL 00	DLE 10	SP 40	0 0F0	@ 7C	P D7	\ 79	p 97	20	30	41	58	76	9F	B8	DC	0
0 0 0 1	1	SOH 01	DC1 11	! ① 4F	1 F1	A C1	Q D8	a 81	q 98	21	31	42	59	77	AO	B9	DD	1
0 0 1 0	2	STX 02	DC2 12	" 7F	2 F2	B C2	R D9	b 82	r 99	22	1A	43	62	78	AA	BA	DE	2
0 0 1 1	3	ETX 03	DC3 13	# 7B	3 F3	C C3	S E2	c 83	s A2	23	33	44	63	80	AB	BB	DF	3
0 1 0 0	4	ECT 37	DC4 3C	$ 5B	4 F4	D C4	T E3	d 84	t A3	24	34	45	64	8A	AC	BC	EA	4
0 1 0 1	5	ENQ 2D	NAK 3D	% 6C	5 F5	E C5	U E4	e 85	u A4	15	35	46	65	8B	AD	BD	EB	5
0 1 1 0	6	ACK 2E	SYN 32	& 50	6 F6	F C6	V E5	f 86	v A5	06	36	47	66	8C	AE	BE	EC	6
0 1 1 1	7	BEL 2F	ETB 26	' 7D	7 F7	G C7	W E6	g 87	w A6	17	08	48	67	8D	AF	BF	ED	7
1 0 0 0	8	BS 16	CAN 18	(4D	8 F8	H C8	X E7	h 88	x A7	28	38	49	68	8E	B0	CA	EE	8
1 0 0 1	9	HT 05	EM 19	) 5D	9 F9	I C9	Y E8	i 89	y A8	29	39	51	69	8F	B1	CB	EF	9
1 0 1 0	A	IF 25	SUB 3F	* 5C	7A	J D1	Z E9	j 91	z A9	2A	3A	52	70	90	B2	CC	FA	10
1 0 1 1	B	VT 0B	ESC 27	+ 4E	; 5E	K D2	[4A	k 92	{ CO	2B	3B	53	71	9A	B3	CD	FB	11
1 1 0 0	C	FF OC	FS 1C	, 6B	< 4C	L D3	\ E0	l 93	¦ 6A	2C	04	54	72	9B	B4	CE	FC	12
1 1 0 1	D	CR OD	GS 1D	- 60	= 7E	M D4	] 5A	m 94	} D0	09	14	55	73	9C	B5	CF	FD	13
1 1 1 0	E	SO OE	RS 1E	. 4B	> 6E	N D5	^ ② 5F	n 95	~ A1	0A	3E	56	74	9D	B6	DA	FE	14
1 1 1 1	F	SI OF	US 1F	/ 61	? 6F	O D6	_ 6D	o 96	DEL 07	1B	E1	57	75	9E	B7	DB	EO FF	15

1 may be "1"
2 may be "¬"
3 The top line in each entry to the table represents an assigned character (Columns 0 to 7). The bottom line in each entry is the corresponding EBCDIC Code, in hexadecimal notation.

The Hexadecimal EBCDIC entry is formed thus:

Eight EBCDIC bits

MSB 0 1 2 3 4 5 6 7 LSB

1st Digit 2nd Digit

Example: 0 1 0 1 1 1 0 0 or *

5 C

To convert ASCII-8 asterisk (*) to EBCDIC-8

E_8 E_1

* in ASCII is a 2A or binary 0010 1010

applying this as an address to the MM5230QY/MM4230QY

bit-0 bit-7

gives the output 0101 1100, which is an EBCDIC-8 asterisk.

10

National Semiconductor

MM4230RS/MM5230RS Binary-to-Modulo-n Divider Code Converter

general description

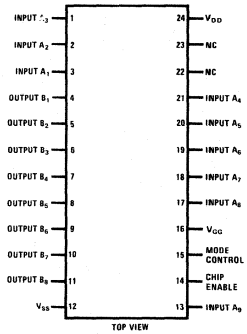
The MM4230RS/MM5230RS binary to modulo-n divider code converter is set up to generate the program input settings for a pair of DM7520/DM8520 modulo-n dividers, in order to divide by any binary number from one to 255. Detailed instructions for use of the DM7520/DM8520 are given in its data sheet.

Applying the required division ratio, in binary, to the inputs of the ROM as shown, generates two sets of four program inputs, one for each of the 2 DM7520/DM8520 dividers.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

connection diagram

Dual-In-Line Package



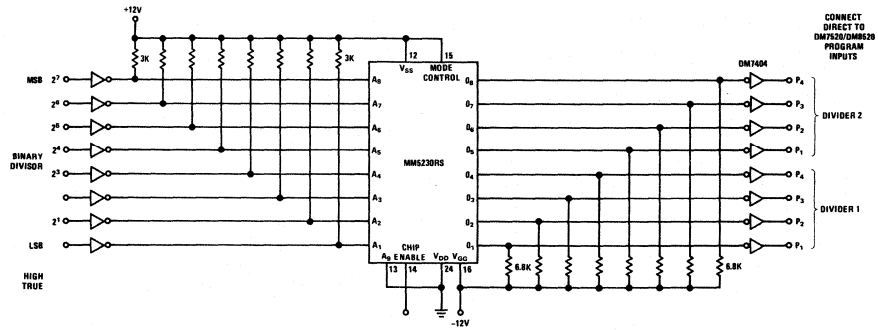
TOP VIEW

Order Number MM4230RS/J or MM5230RS/J
See NS Package J24A

Order Number MM5230RS/N
See NS Package N24B

typical application

Binary to Modulo-n Divider



code conversion table

SETTING								÷ BY
DIVIDER 1				DIVIDER 2				
B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	
0	1	1	1	1	1	1	1	255
1	0	1	1	1	1	1	1	254
0	1	0	1	1	1	1	1	253
0	0	1	0	1	1	1	1	252
1	0	0	1	0	1	1	1	251
0	1	0	0	1	0	1	1	250
0	0	1	0	0	1	0	1	249
0	0	0	1	0	0	1	0	248
0	0	0	0	1	0	0	1	247
0	0	0	0	0	1	0	0	246
0	0	0	0	0	0	1	0	245
0	0	0	0	0	0	0	1	244
1	0	0	0	0	0	0	0	243
1	1	0	0	0	0	0	0	242
1	1	1	0	0	0	0	0	241
0	1	1	1	0	0	0	0	240
1	0	1	1	0	0	0	0	239
1	1	0	1	1	1	0	0	238
0	1	1	0	1	1	1	0	237
0	0	1	1	0	1	1	1	236
0	0	0	1	1	0	1	1	235
0	0	0	0	1	1	0	1	234
0	0	0	0	0	1	1	0	233
0	0	0	0	0	0	1	1	232
1	0	0	0	0	0	0	1	231
0	1	0	0	0	0	0	0	230
0	0	1	0	0	0	0	0	229
1	0	0	1	0	0	0	0	228
1	1	0	0	1	0	0	0	227
0	1	1	0	0	1	0	0	226
1	0	1	1	0	0	1	0	225
0	1	0	1	1	0	0	1	224
0	0	1	0	1	1	0	0	223
0	0	0	1	0	1	1	0	222
0	0	0	0	1	0	1	1	221
0	0	0	0	0	1	0	1	220
1	0	0	0	0	0	1	0	219
1	1	0	0	0	0	0	1	218
0	1	1	0	0	0	0	0	217
1	0	1	1	0	0	0	0	216
0	1	0	1	1	0	0	0	215
1	0	1	0	1	1	0	0	214
1	1	0	1	0	1	1	0	213
1	1	1	0	1	0	1	1	212
0	1	1	1	0	1	0	1	211
0	0	1	1	1	0	1	0	210
0	0	0	1	1	1	0	1	209
0	0	0	0	1	1	1	0	208
1	0	0	0	0	1	1	1	207
0	1	0	0	0	0	1	1	206
1	0	1	0	0	0	0	1	205
1	1	0	1	0	0	0	0	204
1	1	1	0	1	0	0	0	203
1	1	1	1	0	1	0	0	202
0	1	1	1	1	0	1	0	201
0	0	1	1	1	1	0	1	200
1	0	0	1	1	1	1	0	199
0	1	0	0	1	1	1	1	198
0	0	1	0	0	1	1	1	197
0	0	0	1	0	0	1	1	196
1	0	0	0	1	0	0	1	195
1	1	0	0	0	1	0	0	194
1	1	1	0	0	0	1	0	193
0	1	1	1	0	0	0	1	192
0	0	1	1	1	0	0	0	191
0	0	0	1	1	1	0	0	190
1	0	0	0	1	1	1	0	189
0	1	0	0	0	1	1	1	188
1	0	1	0	0	0	1	1	187
1	1	0	1	0	0	0	1	186
0	1	1	0	1	0	0	0	185
0	0	1	1	0	1	0	0	184
1	0	0	1	1	0	1	0	183
0	1	0	0	1	1	0	1	182
0	0	1	0	0	1	1	0	181
1	0	0	1	0	0	1	1	180
0	1	0	0	1	0	0	1	179
0	0	1	0	0	1	0	0	178
1	0	0	1	0	0	1	0	177
1	1	0	0	1	0	0	1	176
1	1	1	0	0	1	0	0	175
0	1	1	1	0	0	1	0	174
1	0	1	1	1	0	0	1	173
0	1	0	1	1	1	0	0	172
1	0	1	0	1	1	1	0	171
1	1	0	1	0	1	1	1	170
0	1	1	0	1	0	1	1	169
1	0	1	1	0	1	0	1	168
1	1	0	1	1	0	1	0	167
0	1	1	0	1	1	0	1	166
1	0	1	1	0	1	1	0	165
0	1	0	1	1	0	1	1	164
0	0	1	0	1	1	0	1	163
1	0	0	1	0	1	1	0	162
1	1	0	0	1	0	1	1	161
0	1	1	0	0	1	0	1	160
1	1	1	1	0	0	1	0	159
0	1	1	0	1	1	0	0	158
1	0	1	1	1	1	0	0	157
0	1	0	1	1	1	1	0	156
0	1	1	0	1	1	1	1	155
1	0	1	1	0	0	1	1	154
1	1	0	1	1	0	1	1	153
0	1	1	0	1	1	0	1	152
0	0	1	1	0	1	1	0	151
1	0	0	1	1	0	1	1	150
0	1	0	0	1	1	0	1	149
0	0	1	0	1	1	1	0	148
0	0	0	1	0	1	1	1	147
1	0	0	0	1	0	1	1	146
1	1	0	0	0	1	0	1	145
1	1	1	0	0	0	1	0	144
1	1	1	1	0	0	0	1	143
1	1	1	1	1	0	0	0	142
0	1	1	1	1	1	0	0	141
0	0	1	1	1	1	1	0	140
0	0	0	1	1	1	1	1	139
1	0	0	0	1	1	1	1	138
1	1	0	0	0	1	1	1	137
0	1	1	0	0	0	1	1	136
0	0	1	1	0	0	0	1	135
0	0	0	1	1	0	0	0	134
1	0	0	0	1	1	0	0	133
0	1	0	0	0	1	1	0	132
0	0	1	0	0	0	1	1	131
0	0	0	1	0	0	0	1	130
1	0	0	0	1	0	0	0	129
0	1	0	0	0	1	0	0	128
0	0	1	0	0	0	1	0	127
1	0	0	1	0	0	0	1	126
0	1	0	0	1	0	0	0	125
1	0	1	0	0	1	0	0	124
0	1	0	1	0	0	1	0	123
0	0	1	0	1	0	0	1	122
1	0	0	1	0	1	0	0	121
1	1	0	0	1	0	1	0	120
0	1	1	0	0	1	0	1	119
0	0	1	1	0	0	1	0	118
1	0	0	1	1	0	0	1	117
1	1	0	0	1	1	0	0	116
0	1	1	1	0	0	1	1	115
1	0	1	1	1	0	0	1	114
1	1	0	1	1	1	0	0	113
1	1	1	0	1	1	1	0	112
0	1	1	1	0	1	1	1	111
0	0	1	1	1	0	1	1	110
1	0	0	1	1	1	1	1	109
0	1	0	0	1	1	1	1	108
0	0	1	0	0	1	1	1	107
0	0	0	1	0	0	1	1	106
1	0	0	0	1	0	0	1	105
1	1	0	0	0	1	0	0	104
1	1	1	0	0	0	1	0	103
0	1	1	1	0	0	0	1	102
0	0	1	1	1	0	0	0	101
0	0	0	1	1	1	0	0	100
1	0	0	0	1	1	1	0	99
0	1	0	0	0	1	1	1	98
1	0	1	0	0	0	1	1	97
1	1	0	1	0	0	0	1	96
0	1	1	0	1	0	0	0	95
0	0	1	1	0	1	0	0	94
1	0	0	1	1	0	1	0	93
0	1	0	0	1	1	0	1	92
0	0	1	0	0	1	1	0	91
1	0	0	1	0	0	1	1	90
0	1	0	0	1	0	0	1	89
0	0	1	0	0	1	0	0	88
1	0	0	1	0	0	1	0	87
1	1	0	0	1	0	0	1	86
1	1	1	0	0	1	0	0	85
0	1	1	1	0	0	1	0	84
1	0	1	1	1	0	0	1	83
0	1	0	1	1	1	0	0	82
1	0	1	0	1	1	1	0	81
1	1	0	1	0	1	1	1	80
0	1	1	0	1	0	1	1	79
1	0	1	1	0	1	0	1	78
1	1	0	1	1	0	1	0	77
0	1	1	0	1	1	0	1	76
1	1	1	0	0	0	1	1	75
1	1	1	1	0	0	1	0	74
1	1	1	1	1	0	0	1	73
0	1	1	1	1	1	0	0	72
1	1	1	1	0	1	1	0	71
1	1	1	1	1	1	1	1	70
1	1	1	1	1	1	0	1	69
1	1	1	1	1	0	1	0	68
1	1	1	1	0	1	0	1	67
1	1	1	1	0	0	1	0	66
1	1	1	1	0	0	0	1	65
1	1	1	1	0	0	0	0	64
1	1	1	1	1	0	0	0	63
1	1	1	1	1	1	0	0	62
1	1	1	1	1	1	1	0	61
1	1	1	1	1	1	1	1	60
1	1	1	1	1	1	1	0	59
1	1	1	1	1	1	0	1	58
1	1	1	1	1	0	1	1	57
1	1	1	1	1	0	0	0	56
1	1	1	1	0	0	1	1	55
1	1	1	1	0	0	1	0	54
1	1	1	1	0	0	0	1	53
1	1	1	1	0	0	0	0	52
1	1	1	1	1	0	0	0	51
1	1	1	1	1	1	0	0	50
1	1	1	1	1	1	1	0	49
1	1	1	1	1	1	1	1	48
1	1	1	1	0	1	1	1	47
1	1	1	1	0	1	1	0	46
1	1	1	1	0	1	0	1	45
1	1	1	1	0	1	0	0	44
1	1	1	1	1	1	0	0	43
1	1	1	1	1	1	1	0	42
1	1	1	1	1	1	1	1	41
1	1	1	1	1	0	1	1	40
1	1	1	1	1	0	0	0	39
1	1	1	1	1	0	0	1	38
1	1	1	1	0	0	0	0	37
1	1	1	1	0	0	0	1	36
1	1	1	1	0	0	1	0	35
1	1	1	1	0	1	0	0	34
1	1	1	1	0	1	1	0	33
1	1	1	1	1	0	0	0	32
1	1	1	1	1	0	0	1	31
1	1	1	1	1	0	1	0	30
1	1	1	1	1	0	1	1	29
1	1	1	1	1	1	0	0	28
1	1	1	1	1	1	0	1	27
1	1	1	1	1	1	1	0	26
1	1	1	1	1	1	1	1	25
1	1	1	1	1	1	1	0	24
1	1	1	1	1	1	0	1	23
1	1	1	1	1	1	0	0	22
1	1	1	1	1	0	1	1	21
1	1	1	1	1	0	1	0	20
1	1	1	1	1	0	0	1	19
1	1	1	1	1	0	0	0	18
1	1	1	1	0	1	1	1	17
1	1	1	1	0	1	1	0	16
1	1	1	1	0	1	0	1	15
1	1	1	1	0	1	0	0	14
1	1	1	1	0	0	1	1	13
1	1	1	1	0	0	1	0	12
1	1	1	1	0	0	0	1	11
1	1	1	1	0	0	0	0	10
1	1	1	1	1	1	1	1	9
1	1	1	1	1	1	1	0	8
1	1	1	1	1	1	0	1	7
1	1	1	1	1	1	0	0	6
1	1	1	1	1	0	1	1	5
1	1	1	1	1	0	1	0	4
1	1	1	1	1	0	0	1	3
1	1	1	1	1	0	0	0	2

National Semiconductor

MM4231RP/MM5231RP EBCDIC-to-ASCII-7 Code Converter

general description

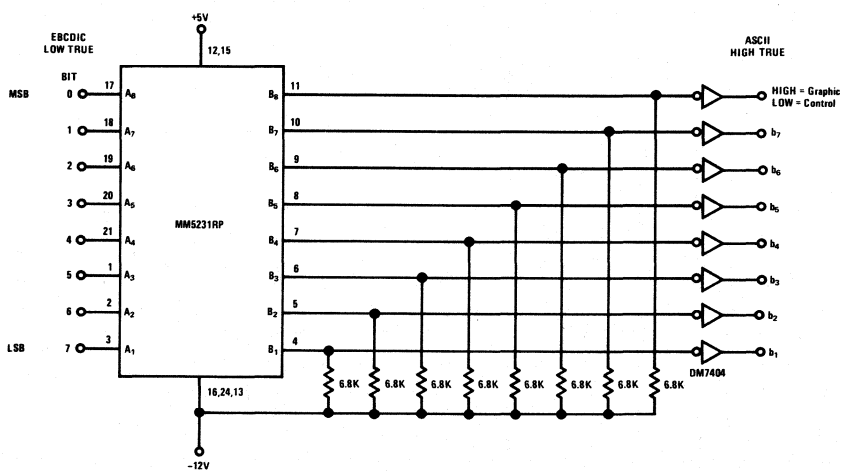
The MM4231RP/MM5231RP is a 2048-bit read-only memory that has been programmed to convert from EBCDIC, an extended binary coded decimal interchange code used in the IBM1130 computer, to ASCII-7, the American Standard Code for Information Interchange in seven bits.

This conversion differs from the ANSI x 3.26 conversion of the MM4230QX/MM5230QX in that it follows certain earlier IBM1130 character assignments. Also certain EBCDIC control codes are arbitrarily preserved and translated (see translation chart on truth table).

For electrical, environmental and mechanical details, refer to the MM4231/MM5231 data sheet.

typical application

EBCDIC TO ASCII-7



Order Number MM4231RP/J or MM5231RP/J
See NS Package J24A

Order Number MM5231RP/N
See NS Package N24B

code conversion tables

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT								OUTPUT							
	EBCDIC SYMBOL	ASCII SYMBOL	MSB							LSB	CC/G	MSB						LSB
0	NULL	NUL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	SOH	SOH	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
2	STX	STX	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
3	ETX	ETX	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
4	PF		0	0	0	0	0	1	0	0								
5	HT	HT									0	0	0	0	1	0	0	1
6	LC																	
7	DEL	DEL									0	1	1	1	1	1	1	1
8																		
9																		
10	SMM																	
11	VT	VT									0	0	0	0	1	0	1	1
12	FF	FF									0	0	0	0	1	1	0	0
13	CR	CR									0	0	0	0	1	1	0	1
14	S0	S0									0	0	0	0	1	1	1	0
15	S1	S1									0	0	0	0	1	1	1	1
16	DLE	DLE									0	0	0	1	0	0	0	0
17	DC1	DC1									0	0	0	1	0	0	0	1
18	DC2	DC2									0	0	0	1	0	0	1	0
19	DC3	DC3									0	0	0	1	0	0	1	1
20	RES	'									1	1	1	0	0	0	0	0
21	NL	\									1	1	0	1	1	1	0	0
22	BS	BS									0	0	0	0	1	0	0	0
23	IDL																	
24	CAN	CAN									0	0	0	1	1	0	0	0
25	EM	EM									0	0	0	1	1	0	0	1
26	CC																	
27	CUI																	
28	FLS	FS									0	0	0	1	1	1	0	0
29	GS	GS									0	0	0	1	1	1	0	1
30	RDS	RS									0	0	0	1	1	1	1	0
31	US	US									0	0	0	1	1	1	1	1
32	DS																	
33	SOS																	
34	FS																	
35																		
36	BYP										0	0	0	0	0	0	0	0
37	LF	LF									0	0	0	0	1	0	1	0
38	EOB	ETB									0	0	0	1	0	1	1	1
39	PRE	ESC									0	0	0	1	1	0	1	1
40																		
41																		
42	SM																	
43	CU2																	
44																		
45	ENQ	ENQ									0	0	0	0	0	1	0	1
46	ACK	ACK									0	0	0	0	0	1	1	0
47	BEL	BEL									0	0	0	0	0	1	1	1
48																		
49																		
50	SYN	SYN									0	0	0	1	0	1	1	0
51																		
52	PN																	
53	RS	DC4									0	0	0	1	0	1	0	0
54	UC																	
55	EOT	EOT									0	0	0	0	0	1	0	0
56																		
57																		
58																		
59	CU3																	
60	DCA																	
61	NAK	NAK									0	0	0	1	0	1	0	1
62																		
63	SUB	SUB									0	0	0	1	1	0	1	0
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

CONTINUING BINARY SEQUENCE

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB ... LSB	CODE OUTPUT CC/G	OUTPUT MSB						LSB
64	SP	SP		1	0	1	0	0	0	0	0
65											
66											
67											
68											
69											
70											
71											
72											
73											
74	¢	~		1	1	1	1	1	1	1	0
75	.	.		1	0	1	0	1	1	1	0
76	<	<		1	0	1	1	1	1	0	0
77	(	(		1	0	1	0	1	0	0	0
78	+	+		1	0	1	0	1	0	1	1
79	¦	¦		1	1	1	1	1	1	0	0
80	&	&		1	0	1	0	0	1	1	0
81											
82											
83											
84											
85											
86											
87											
88											
89											
90	!	!		1	0	1	0	0	0	0	1
91	$	$		1	0	1	0	0	1	0	0
92	*	*		1	0	1	0	1	0	1	0
93	)	)		1	0	1	0	1	0	0	1
94	;	;	CONTINUING BINARY SEQUENCE	1	0	1	1	1	0	1	1
95	¬	^		1	1	0	1	1	1	1	0
96	–	–		1	0	1	0	1	1	0	1
97	/	/		1	0	1	0	1	1	1	1
98											
99											
100											
101											
102											
103											
104											
105											
106											
107	,	,		1	0	1	0	1	1	0	0
108	%	%		1	0	1	0	0	1	0	1
109	—	—		1	1	0	1	1	1	1	1
110	>	>		1	0	1	1	1	1	1	0
111	?	?		1	0	1	1	1	1	1	1
112											
113											
114											
115											
116											
117											
118											
119											
120											
121											
122	:	:		1	0	1	1	1	0	1	0
123	#	#		1	0	1	0	0	0	1	1
124	@	@		1	1	0	0	0	0	0	0
125	'	'		1	0	1	0	0	1	1	1
126	=	=		1	0	1	1	1	1	0	1
127	"	"		1	0	1	0	0	0	1	0
			A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB ... LSB	CC/G	OUTPUT MSB						LSB
128											
129	a	a		1	1	1	0	0	0	0	1
130	b	b		1	1	1	0	0	0	1	0
131	c	c		1	1	1	0	0	0	1	1
132	d	d		1	1	1	0	0	1	0	0
133	e	e		1	1	1	0	0	1	0	1
134	f	f		1	1	1	0	0	1	1	0
135	g	g		1	1	1	0	0	1	1	1
136	h	h		1	1	1	0	1	0	0	0
137	i	i		1	1	1	0	1	0	0	1
138											
139	}	}		1	1	1	1	1	0	1	1
140											
141											
142											
143											
144											
145	j	j		1	1	1	0	1	0	1	0
146	k	k		1	1	1	0	1	0	1	1
147	l	l		1	1	1	0	1	1	0	0
148	m	m		1	1	1	0	1	1	0	1
149	n	n		1	1	1	0	1	1	1	0
150	o	o		1	1	1	0	1	1	1	1
151	p	p		1	1	1	1	0	0	0	0
152	q	q		1	1	1	1	0	0	0	1
153	r	r		1	1	1	1	0	0	1	0
154											
155	}	}		1	1	1	1	1	1	0	1
156											
157											
158			CONTINUING BINARY SEQUENCE								
159											
160											
161											
162	s	s		1	1	1	1	0	0	1	1
163	t	t		1	1	1	1	0	1	0	0
164	u	u		1	1	1	1	0	1	0	1
165	v	v		1	1	1	1	0	1	1	0
166	w	w		1	1	1	1	0	1	1	1
167	x	x		1	1	1	1	1	0	0	0
168	y	y		1	1	1	1	1	0	0	1
169	z	z		1	1	1	1	1	0	1	0
170											
171											
172											
173	[	[		1	1	0	1	1	0	1	1
174											
175											
176											
177											
178											
179											
180											
181											
182											
183											
184											
185											
186											
187											
188											
189	]	]		1	1	0	1	1	1	0	1
190											
191											
			A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

code conversion tables(con't)

	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT								OUTPUT							
ROM ADDRESS	EBCDIC SYMBOL	ASCII SYMBOL	MSB							LSB	CC/G	MSB						LSB
192	+ ZERO																	
193	A	A									1	1	0	0	0	0	0	1
194	B	B									1	1	0	0	0	0	1	0
195	C	C									1	1	0	0	0	0	1	1
196	D	D									1	1	0	0	0	1	0	0
197	E	E									1	1	0	0	0	1	0	1
198	F	F									1	1	0	0	0	1	1	0
199	G	G									1	1	0	0	0	1	1	1
200	H	H									1	1	0	0	1	0	0	0
201	I	I									1	1	0	0	1	0	0	1
202																		
203																		
204																		
205																		
206																		
207																		
208	-ZERO																	
209	J	J									1	1	0	0	1	0	1	0
210	K	K									1	1	0	0	1	0	1	1
211	L	L									1	1	0	0	1	1	0	0
212	M	M									1	1	0	0	1	1	0	1
213	N	N									1	1	0	0	1	1	1	0
214	O	O									1	1	0	0	1	1	1	1
215	P	P									1	1	0	1	0	0	0	0
216	Q	Q									1	1	0	1	0	0	0	1
217	R	R									1	1	0	1	0	0	1	0
218																		
219																		
220																		
221																		
222			CONTINUING BINARY SEQUENCE															
223																		
224																		
225																		
226	S	S									1	1	0	1	0	0	1	1
227	T	T									1	1	0	1	0	1	0	0
228	U	U									1	1	0	1	0	1	0	1
229	V	V									1	1	0	1	0	1	1	0
230	W	W									1	1	0	1	0	1	1	1
231	X	X									1	1	0	1	1	0	0	0
232	Y	Y									1	1	0	1	1	0	0	1
233	Z	Z									1	1	0	1	1	0	1	0
234																		
235																		
236																		
237																		
238																		
239																		
240	0	0									1	0	1	1	0	0	0	0
241	1	1									1	0	1	1	0	0	0	1
242	2	2									1	0	1	1	0	0	1	0
243	3	3									1	0	1	1	0	0	1	1
244	4	4									1	0	1	1	0	1	0	0
245	5	5									1	0	1	1	0	1	0	1
246	6	6									1	0	1	1	0	1	1	0
247	7	7									1	0	1	1	0	1	1	1
248	8	8									1	0	1	1	1	0	0	0
249	9	9									1	0	1	1	1	0	0	1
250																		
251			1	1	1	1	1	0	1	1								
252			1	1	1	1	1	1	0	0								
253			1	1	1	1	1	1	0	1								
254			1	1	1	1	1	1	1	0								
255			1	1	1	1	1	1	1	1								
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

National Semiconductor

MM4232/MM5232 AEI, AEJ, AEK Sine Look-Up Table

general description

The MM4232/MM5232 AEI, AEJ and AEK are all P-channel enhancement mode MOS read-only memories, each storing 4096 bits. They are programmed to generate the sine function of any angle expressed as a binary fraction of a right-angle. They may be combined and arranged to provide a look-up table of varying resolution and accuracy, to meet almost any system requirement for generation of the sine function.

application information

Figures 1 through 4 show the four ways that these parts may be combined. The table shows the performance of all combinations.

performance specifications

FIGURE	ROM NO. USED	RESOLUTION (= INPUT WORD LENGTH)	OUTPUT WORD LENGTH	ACCURACY	ADDER PACKAGES REQUIRED
1	AEI	9 bits	8 bits	+0 −1 bit in 8	0
2	AEI + AEJ	9 bits	16 bits	± 1/2 bit in 16	0
3	AEI + AEJ + AEK	12 bits	16 bits	± 3/4 bit in 14	4
4	AEI + AEJ + 2 AEK's	15 bits	16 bits	±1 bit in 14	6

SINE LOOK-UP TABLE WITH HIGH RESOLUTION AND ACCURACY

Theoretical Background

The table is based upon the equation:

$$\sin (M + L) = \sin M \cos L + \cos M \sin L \qquad (1)$$

By splitting M and L each into two parts MM, ML, and LM, LL, and (assuming M >> L) the following equation is obtained.

$$\begin{aligned} &\sin (M + L) \approx \sin (MM + ML) \qquad (2)\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) \sin LM\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) \sin LL\\ &\approx \sin (MM + ML)\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) (\sin LM + \sin LL) \end{aligned}$$

The following approximations have been used:

$$\begin{aligned} &\cos (LM + LL) \approx 1\\ &\sin (LM + LL) \approx \sin (LM) + \sin (LL)\\ &\cos (MM + ML) \approx \cos (MM + 1/2 \text{ LSB of } MM) \end{aligned}$$

By taking MM = 6 bits, ML = 3 bits, LM = 3 bits, and LL = 3 bits, 15 bits resolution is obtained. The accuracy has been computed by comparing the values of Equation 2 with the ideal value of the sine of an angle θ resolved into 2^{15} increments in the range $0 \leq \theta < \pi/2$.

This error, due to the mathematical approximation, is $\pm 3.2 \times 10^{-5}$ maximum, corresponding to ±1 bit in 15 bits. In addition to the mathematical error, an inevitable round-off error in the 16th bit is introduced. As there are 3 LSB outputs to be added (Figure 4), the maximum round-off error will be ±1-1/2 bit in 16 bits or $\pm 2.3 \times 10^{-5}$. The theoretical maximum total error will then be $\pm (3.2 + 2.3) \times 10^{-5} = \pm 5.5 \times 10^{-5}$, which is slightly less than ±1 bit in 14 bits.

A computer analysis shows that the actual errors in the table as implemented are as follows:

$+4.4 \times 10^{-5}$ (at 61.872°)

-4.7×10^{-5} (at 83.142°)

As the sine function is very linear in the LM-LL range, the third term of Equation 2 can be considered as being $1/(2)^3$ of the second term without significant error. Therefore, the same pattern can be used for the two lower ROMs in Figure 4, and a total of three different masks are needed. In addition, six 4-bit adders are used.

Order Number MM4232J or MM5232J
See NS Package J24A

Order Number MM5232N
See NS Package N24B

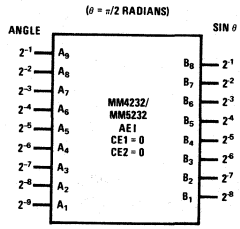


FIGURE 1

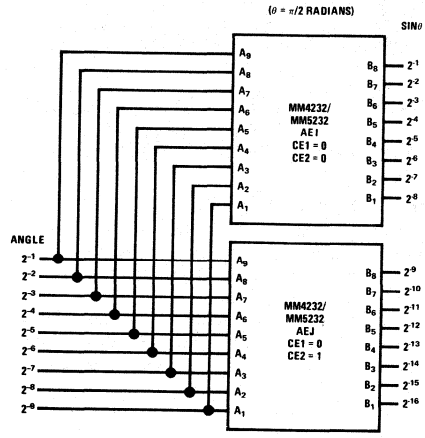


FIGURE 2

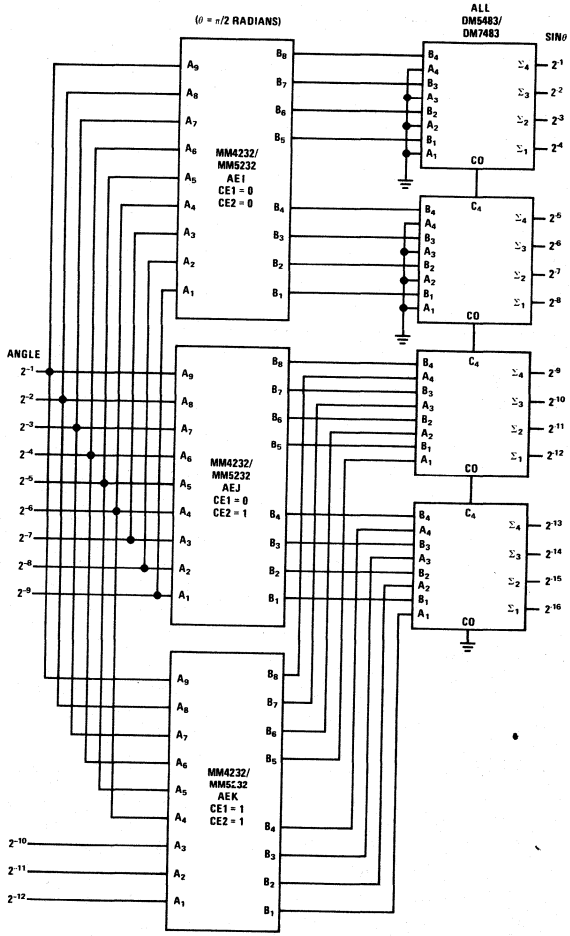


FIGURE 3.

Note: Angles are expressed as binary fractions of a right-angle.

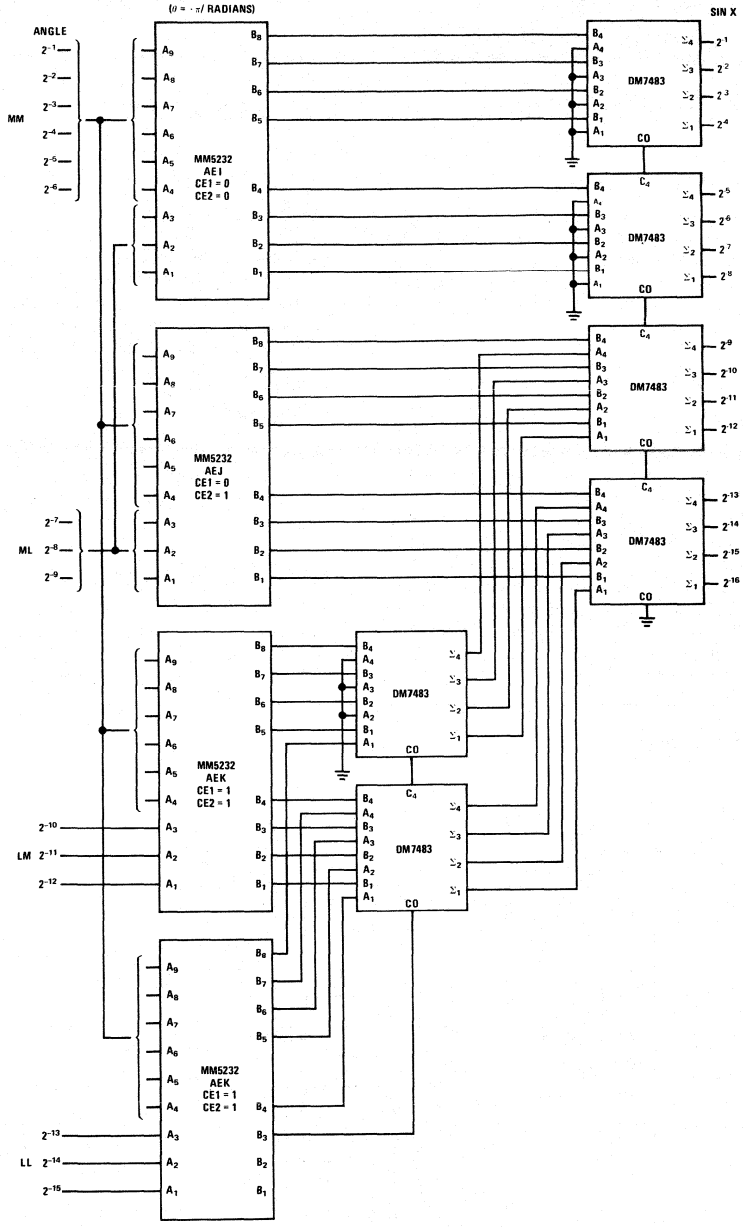


FIGURE 4

Note: Angles are expressed as binary fractions of a right angle.

National Semiconductor

SK0003 Sine/Cosine Look-Up Table Kit

general description

The SK0003 Sine/Cosine Look-Up Table Kit consists of four MOS ROMs: three MM4210/MM5210's and one MM4220/MM5220-1024 bit static read only memories. They are P-channel enhancement mode monolithic MOS integrated circuits utilizing a low threshold technology.

THE SINE FUNCTION

The SK0003 implements the equation $\sin\theta$ = sin M cos L + cos M sin L. Cos L was assumed to be 1 in the equation. However, it is a variable between 1 and 0.99998 and is a function of round off error. Worst case error is 1-5/8 bits in LSB at address 1415 (62.25°). The error increases from zero to .002% every 8 bits, therefore, the MM4220/MM5220 provides the error correction factor $\cos(M - 2.81^\circ)\sin L$ in the equation $\sin\theta = \sin M + \cos(M - 2.81^\circ)\sin L$. The circuitry to perform this function is shown in Figure 1. Additional information is available in *MOS Brief 10*.

THE COSINE FUNCTION

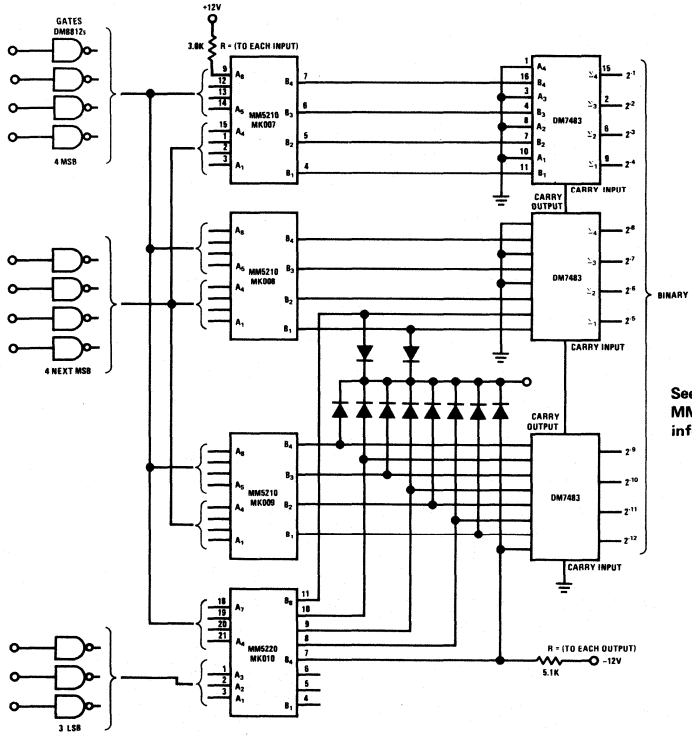
To generate the cosine function $\cos\theta = \sin(\theta - 90^\circ)$, the input must be complemented and a logical "1" added. Figure 2A is a logic diagram of the circuitry used to provide the cosine function, as well as providing both sine and cosine functions in the same system. 11-bit resolution and 12-bit accuracy ±1-5/8-bits is achieved in this configuration.

A reduction in logic can be achieved as shown in Figure 2B if a loss in resolution of 1/2-bit in an 11-bit input or 1/4-bit in a 10-bit input is acceptable.

ELECTRICAL CHARACTERISTICS

Refer to the appropriate data sheet for each device shown in the figures. The devices noted are: MM4210/MM5210, MM4220/MM5220, DM5483/DM7483, DM7812/DM8812 and DM5486/DM7486.

logic diagram



Order Number SK0003C
or
Order Number SK0003M

See MM4210/MM5210 and MM4220/MM5220 data sheets for package information.

FIGURE 1. SK0003 Logic Diagram (Kit Includes ROMs Only). This Circuit Provides 11-Bit Resolution and 12-Bit Accuracy in a θ to Sin θ Converter.

logic diagram

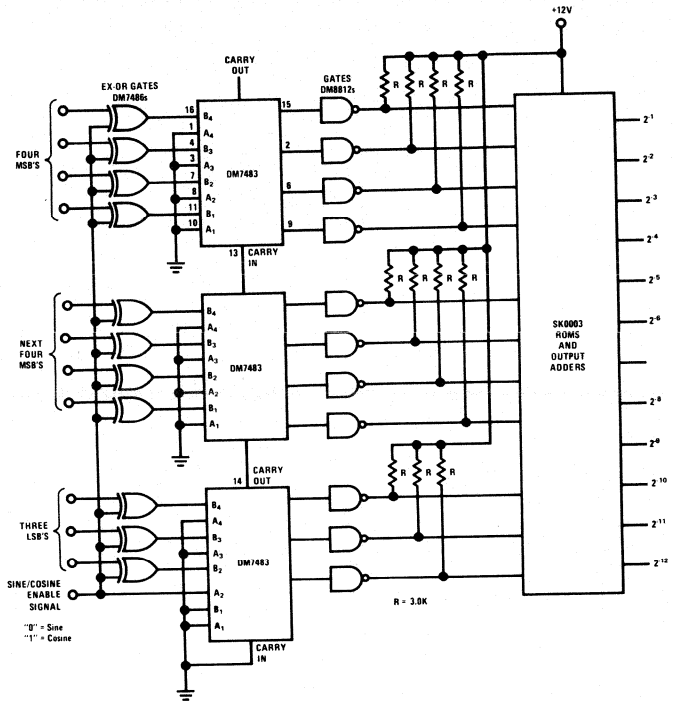


FIGURE 2A. Sine/Cosine Conversion Provides 11-Bit Resolution, 12-Bit ±1-5/8 Bit Accuracy.

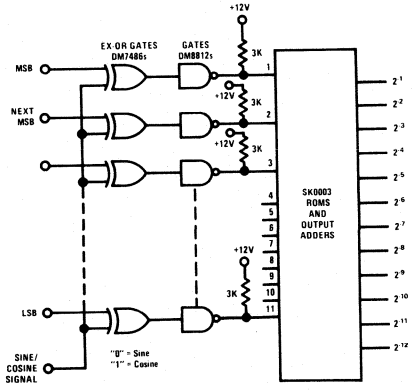


FIGURE 2B. Sine/Cosine Conversion with Cosine Approximated. (Cosine Conversion has 10-Bits Input Resolution and 12-Bit ±1-5/8-Bit Accuracy.)

Section 11

11

Shift Registers

Shift Registers often represent the lowest cost solution to a read/write memory problem, depending on size and speed constraints. National produces the devices shown in this section to support customer's needs for MOS shift registers through 1024 bits per package.

National Semiconductor

MM1402A, MM1403A, MM1404A, MM5024A 1024-Bit Dynamic Shift Registers

general description

The MM1402A, MM1403A, MM1404A, MM5024A 1024-bit dynamic shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. 5 MHz data rates are achieved by on-chip multiplexing. The clock rate is one-half the data rate; i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

All devices in the family can operate from +5V, −5V, or +5V, −9V power supplies.

features

- Guaranteed 5 MHz operation
- Low power dissipation .1 mW/bit at 1 MHz
- DTL/TTL compatible
- Low clock capacitance 125 pF
- Low clock leakage $\leq 1\ \mu A$
- Inputs protected against static charge
- Operation from +5V, −5V or +5V, −9V power supplies
- Seven standard configurations

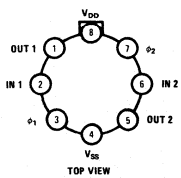
MM1402AD	Quad 256-bit
MM1402AN	Quad 256-bit
MM1403AH	Dual 512-bit
MM1403AN	Dual 512-bit
MM1404AH	Single 1024-bit
MM1404AN	Single 1024-bit
MM5024AH	Single 1024-bit with internal pull-down resistor

applications

- Radar and sonar processors
- CRT displays
- Terminals
- Desk top calculators
- Disk and drum replacement
- Computer peripherals
- Buffer memory
- Special purpose computers—signal processors, digital filtering and correlators, receivers, spectral compressors and digital differential analyzers
- Telephone equipment
- Medical equipment

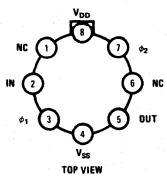
connection diagrams

Metal Can Package



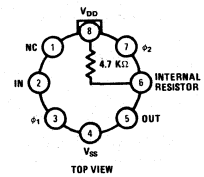
Order Number MM1403AH
See NS Package H08C

Metal Can Package



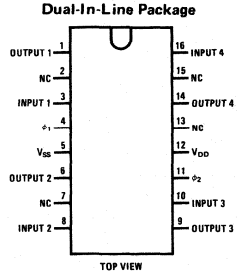
Order Number MM1404AH
See NS Package H08C

Metal Can Package



Order Number MM5024AH
See NS Package H08C

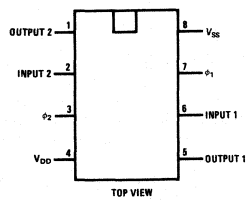
Dual-In-Line Package



Order Number MM1402AD
See NS Package D16C

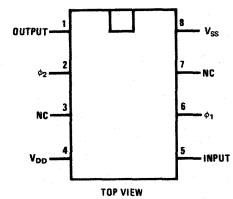
Order Number MM1402AN
See NS Package N16A

Dual-In-Line Package



Order Number MM1403AN
See NS Package N08B

Dual-In-Line Package



Order Number MM1404AN
See NS Package N08B

11

absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW at T_A = 25°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A = −25°C to +70°C, V_{SS} = 5V ±5%, V_{DD} = −5V ±5% or −9V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical Low Level (V_{IL})		V_{SS} − 10.0		V_{SS} − 4.2	V
Logical High Level (V_{IH})		V_{SS} − 1.7		V_{SS} + 0.3	V
Data Input Leakage Current	V_{IN} = −15V, T_A = 25°C, All Other Pins GND		<10	500	nA
Input Capacitance	V_{IN} = V_{SS}		5	10	pF
Clock Input Levels	V_{DD} = −5V ± 5%				
Logical Low Level ($V_{\phi L}$)		V_{SS} − 17		V_{SS} − 15	V
Logical High Level ($V_{\phi H}$)		V_{SS} − 1		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)	V_{DD} = −9V ± 5%	V_{SS} − 14.7		V_{SS} − 12.6	V
Logical High Level ($V_{\phi H}$)		V_{SS} − 1		V_{SS} + 0.3	V
Clock Leakage Current	Min $V_{\phi L}$, T_A = 25°C		10	1000	nA
Clock Capacitance	V_ϕ = V_{SS}		90	125	pF
Data Output Levels					
Logical Low Level (V_{OL})	R_{L1} = 3k to V_{DD}, I_{OL} = 1.6 mA, V_{DD} = −5V ± 5%		−0.3	0.6	V
Logical High Level (V_{OH})	R_{L1} = 3k to V_{DD}, I_{OH} = 100 μA	2.4	3.5		V
Logical Low Level (V_{OL})	R_{L1} = 4.7k to V_{DD}, I_{OL} = 1.6 mA, V_{DD} = −9V ± 5%		−0.3	0.5	V
Logical High Level (V_{OH})	R_{L1} = 4.7k to V_{DD}, I_{OH} = 100 μA	2.4	3.5		V
Logical High Level (V_{OH})	R_{L2} = 4.7k to V_{DD}, V_{DD} = −5V ± 5%	V_{SS} − 1.9	V_{SS} − 1		V
Logical High Level (V_{OH})	R_{L2} = 6.2k to V_{DD}, V_{DD} = −9V ± 5% R_{L3} = 3.9k to V_{SS}	V_{SS} − 1.9	V_{SS} − 1		V
Power Supply Current (I_{DD})	T_A = 25°C, V_{DD} = −5V ± 5% Output Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, $V_{\phi L}$ = V_{SS} − 17V		35	50	mA
	T_A = 0°C			56	mA
	T_A = 25°C, V_{DD} = −9V ± 5% Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, $V_{\phi L}$ = V_{SS} − 14.7V		30	40	mA
	T_A = 0°C			45	mA
Data Output Leakage Current	V_{OUT} = 0.0V, T_A = 25°C, $V_{\phi 1}$ = $V_{\phi 2}$ = V_{SS} − 10V, All Other Pins +5V		<10	1000	nA
Internal Resistor (MM5024A)	T_A = 25°C	3.7	4.7	5.2	kΩ
Output Capacitance	V_{OUT} = V_{SS}, f = 1 MHz		5	10	pF

ac characteristics T_A = −0°C to +70°C, V_{SS} = 5V ±5%

PARAMETER	V_{DD} = −5V ± 5%		V_{DD} = −9V ± 5%		UNITS
	MIN	MAX	MIN	MAX	
Clock Frequency (ϕ_f)	Note 1	2.5	Note 1	1.5	MHz
Data Frequency		5.0		3.0	MHz
Clock Pulse Width (ϕ_{PW})	0.130	10	0.170	10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	10	Note 1	10	Note 1	ns
Clock Transition Times (ϕt_r, ϕt_f)		1000		1000	ns
Data Input Delay Time (t_{ds})	30		60		ns
Data Input Hold Time (t_{dH})	20		20		ns
Data Output Propagation Delay		90		110	ns

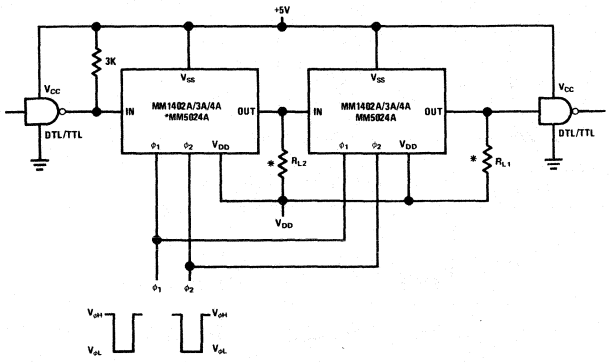
Note 1: Minimum clock frequency is a function of temperature and clock phase delay times, ϕ_d and $\overline{\phi}_d$ as shown by the ϕ_f versus temperature and ϕ_d, $\overline{\phi}_d$ versus temperature curves. The lowest guaranteed clock frequency can be attained by making ϕ_d equal to $\overline{\phi}_d$. The minimum guaranteed clock frequency is:

$\phi_f(\text{min}) \cong 1/(\phi_d + \overline{\phi}_d)$ for the condition ($\phi t_r = \phi t_f << \phi_{PW} << \phi_d$ or $\overline{\phi}_d$), where the variables may not exceed the guaranteed maximums.

Note 2: Capacitance is guaranteed by periodic testing.

typical application

DTL/TTL to MOS Interface



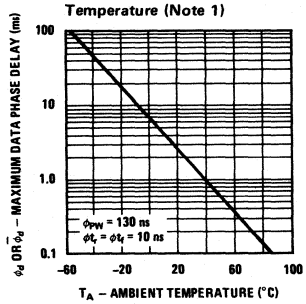
*A 4.7 kΩ resistors is included on the chip in the MM5024A and is connected between Pin 6 and V_{DD}.

R_L Load Resistor Value for Different V_{DD} Supplies

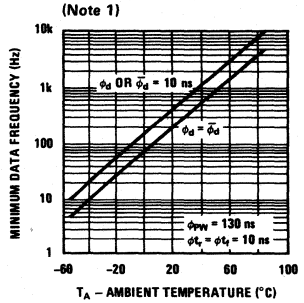
	V_{SS} = 5V V_{DD} = −5V	V_{SS} = 5V V_{DD} = −9V
R_{L1}	3.0k	4.7k
R_{L2}	4.7k	6.8k
R_{L3}	Not required	Not required

performance curves

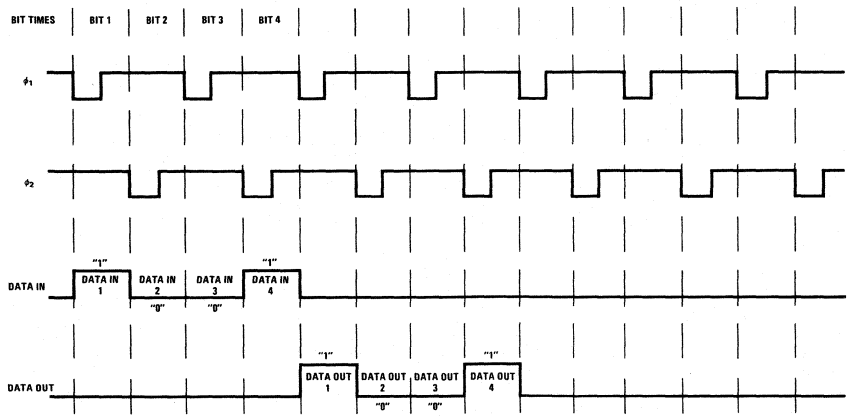
Guaranteed Maximum Data Phase Delay Times vs Temperature (Note 1)



Guaranteed Minimum Data Frequency vs Temperature (Note 1)

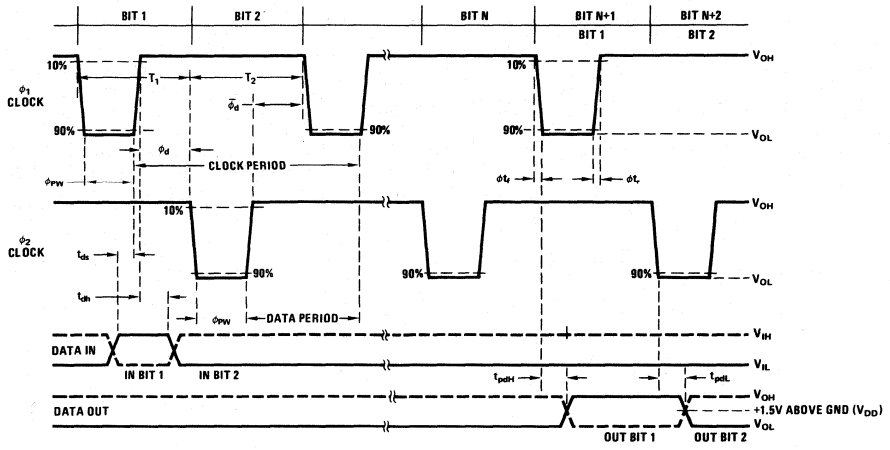


switching time waveforms



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exists at ϕ_1 time. (Beginning on ϕ_1's negative going edge and ending on the succeeding ϕ_2's negative going edge.)

timing diagram



National Semiconductor

MM4016/MM5016 512-Bit Dynamic Shift Register

general description

The MM4016/MM5016 512-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. An input tap provides the option of using the device as either a 500 or 512-bit register.

features

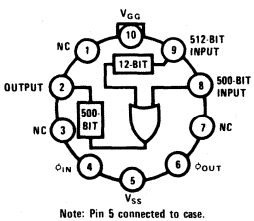
- Bipolar compatibility — +5V, −12V operation. No pull-up or pull-down resistors required.
- Package option — TO-100 or choice of two Dual-In-Line Packages
- Fewer clock drivers required — Clock line capacitance of 100 pF typ
- System flexibility — 300 Hz guaranteed min. operating frequency at 25°C. 500 or 512-bit register length.
- Military and Commercial Temperature Ranges
  - MM4016 −55°C to +125°C
  - MM5016 0°C to +70°C
- Low power dissipation — < 0.17 mW/bit at 1 MHz max. < 30 μW/bit at 100 kHz typ.

applications

- Glass and magnetostrictive delay line replacement.
- CRT refresh memory.
- Radar delay line.
- Drum memory storage (silicon store)
- Long serial memory.

connection diagrams

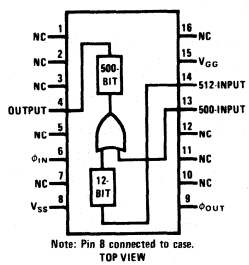
Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4016H or MM5016H
See NS Package H10A

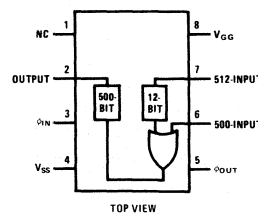
Dual-In-Line Package



Note: Pin 8 connected to case.
TOP VIEW

Order Number MM4016D or MM5016D
See NS Package D16C

Dual-In-Line Package

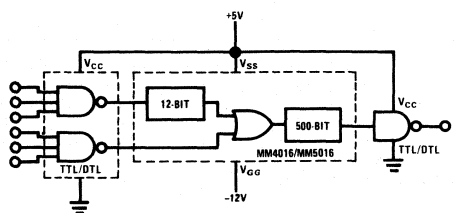


TOP VIEW

Order Number MM5016N
See NS Package N08B

typical application

TTL/MOS Interface



Note: The unused input pin must be connected to V_{SS}.

absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} −22V
Operating Temperature Range	MM4016	−55°C to +125°C
	MM5016	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = − 20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 2)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND, (Note 2)		100	120	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		1.0	2.0	mA
	ϕ_f = 1 MHz		3.5	5.0	mA
	ϕ_f = 2.5 MHz		7.0	10.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f = \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 1)	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			1	μs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit.				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

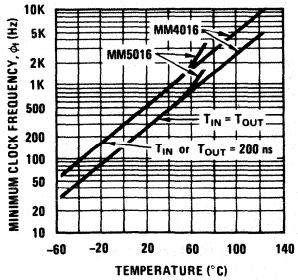
Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}, \text{ where } T_{IN} \text{ and } T_{OUT} \text{ do not exceed the guaranteed maximums.}$$

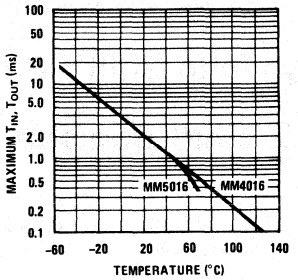
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

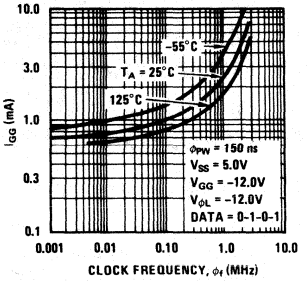
Typical Minimum Clock Frequency vs Temperature (Note 1)



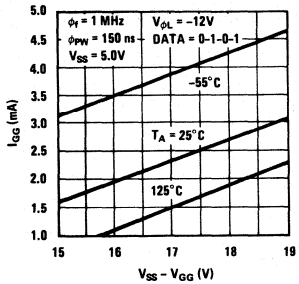
Typical Maximum T_{IN} and T_{OUT} vs Temperature (Note 1)



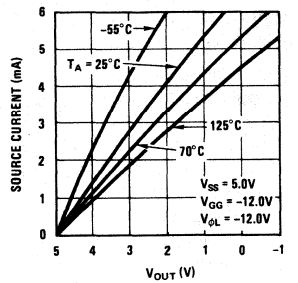
Typical Power Supply Current vs Clock Frequency



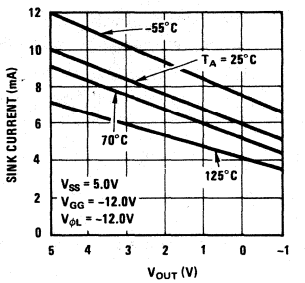
Typical Power Supply Current vs Voltage



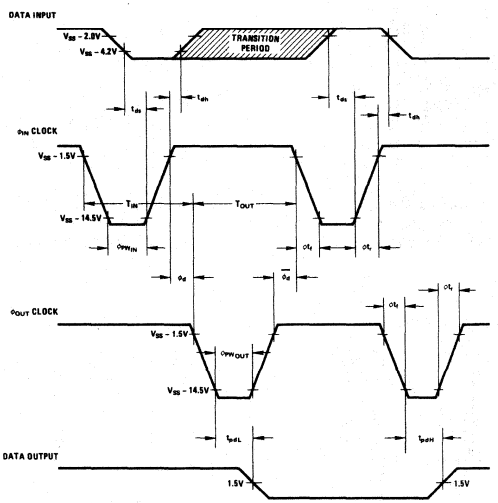
Typical Data Output Source Current vs Voltage



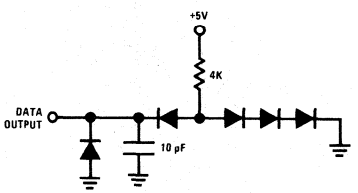
Typical Data Output Sink Current vs Voltage



switching time waveforms



ac test circuit



11

National Semiconductor

MM4025/MM5025 Dual 1024-Bit Dynamic Shift Register MM4026/MM5026 Dual 1024-Bit Dynamic Shift Register MM4027/MM5027 2048-Bit Dynamic Shift Register

general description

These 2048-bit dynamic shift registers are MOS monolithic integrated circuits using P-channel silicon gate technology. They employ a push-pull output for bipolar compatability and on-chip multiplexing to achieve a 6 MHz data rate. The clock rate is one-half the data rate, i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

The MM4025/MM5025 and MM4027/MM5027 have on-chip logic to load and recirculate data.

The MM4026/MM5026 has an individual logic-select line to load one of the two inputs on each of the 1024-bit registers.

features

- Bipolar compatibility — Standard +5V, −12V power supplies
- High frequency of operation — 6 MHz guaranteed
- Low power dissipation — 120 μW/bit at 1 MHz ϕ rate 0°C, guaranteed
- Low clock capacitance — 190 pF max
- Wide operating temperature range
  MM4025,MM4026,MM4027 −55°C to +125°C
  MM5025,MM5026,MM5027 0°C to 70°C

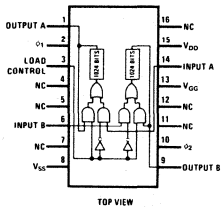
applications

- "Silicon store" replacement for drum and disc memories
- CRT displays
- Buffer memories

logic and connection diagrams

Military Temperature Range

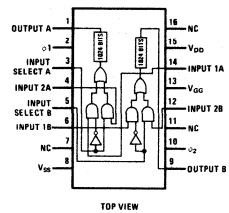
Dual-In-Line Package



TOP VIEW

Order Number MM4025D or MM5025D
See NS Package D16C

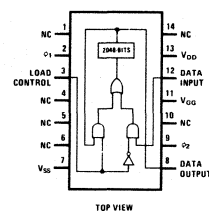
Dual-In-Line Package



TOP VIEW

Order Number MM4026D or MM5026D
See NS Package D16C

Flat Package

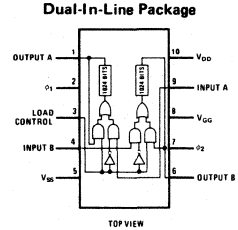


TOP VIEW

Order Number MM4027F or MM5027F
See NS Package F14B

Commercial Temperature Range

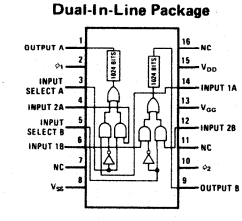
Dual-In-Line Package



TOP VIEW

Order Number MM5025N
See NS Package N10B

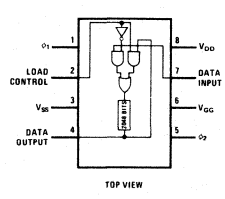
Dual-In-Line Package



TOP VIEW

Order Number MM5026N
See NS Package N16A

Dual-In-Line Package



TOP VIEW

Order Number MM5027N
See NS Package N08B

absolute maximum ratings

Voltage at Any Pin With Respect to V_{SS}	+0.3 to −20.0V
Operating Ambient Temperature Range	
MM4025,MM4026,MM4027	−55°C to +125°C
MM5025,MM5026,MM5027	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics V_{SS} = +5.0V ± 5%, V_{DD} = GND, V_{GG} = −12.0V ±10%

T_A within operating temperature range unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS}−1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS}−10		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −10V, T_A = 25°C, All other pins GND		0.01	1.0	μA
Data Input Capacitance	V_{IN} = 0V, f = 1 MHz, All other pins GND (Note 1)		2.5	5.0	pF
Load/Select Input Levels					
Logical High Level (V_{IH})		V_{SS}−1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Load/Select Input Leakage	V_{IN} = −10V, T_A = 25°C, All other pins GND		0.01	1.0	μA
Load/Select Input Capacitance	V_{IN} = 0V, f = 1 MHz, All other pins GND (Note 1)		4.0	7.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.0		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −15V, T_A = 25°C, All other pins GND		.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0V, f = 1 MHz, All other pins GND (Note 1)		165	190	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA	0.0		0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12.0V, ϕ_{PW} = 160 ns V_{SS} = 5.0V, $V_{\phi L}$ = −12.0V, DATA = Note 4 V_{DD} = 0.0V				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2	3.5	mA
	ϕ_f = 1.0 MHz		2	3.5	mA
	ϕ_f = 3.0 MHz		2	3.5	mA
I_{DD}	0.01 MHz ϕ_f ≤ 0.1 MHz		8	15	mA
	ϕ_f = 1.0 MHz		22	32	mA
	ϕ_f = 3.0 MHz		48	70	mA
Clock Frequency (ϕ_f)					
MM4025,MM4026,MM4027	$\phi t_r = \phi t_f$ = 20 ns (Note 2, Note 3 & Note 5)	0.03	2.0	1.0	MHz
MM5025,MM5026,MM5027		0.003	4.0	1.25	MHz
Clock Pulsewidth (ϕ_{PW})					
MM4025,MM4026,MM4027	$\phi t_r = \phi t_f$ = 20 ns, Data Rate = 2 ϕ_f	0.240		8.0	μs
MM5025,MM5026,MM5027		0.240		10	μs
Clock Phase Delay Times (ϕ_d,$\overline{\phi_d}$)	See Curves	10			ns
Clock Transition Times (ϕt_r, ϕt_f)				0.5	μs
Partial Bit Times (T)	(Note 2, Note 3)				
T_1 Partial Bit Time					
MM4025,MM4026,MM4027		0.5		16.5	μs
MM5025,MM5026,MM5027		0.4		165	μs
T_2 Partial Bit Time					
MM4025,MM4026,MM4027		0.5		16.5	μs
MM5025,MM5026,MM5027		0.4		165	
Data & Load/Select Input Setup Time (t_{ds})		35			ns
Data & Load/Select Input Hold Time (t_{dh})		20			ns
Data Output Propogation Delay from ϕ					
Delay to High Level (t_{pdH})	15 pF Output Capacitance			160	ns
Delay to Low Level (t_{pdL})				160	ns

Note 1: Capacitance is guaranteed by periodic testing.

Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_1 and T_2) as shown by ϕ_f versus temperature and T_1, T_2 versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_1 equal to T_2. The minimum guaranteed clock frequency: $\phi_{f\ (min)} = 1/(T_1 + T_2)$ where T_1 and T_2 do not exceed the guaranteed maximum.

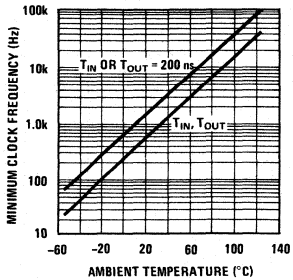
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

Note 4: For data pattern of 1111000011110000 etc.

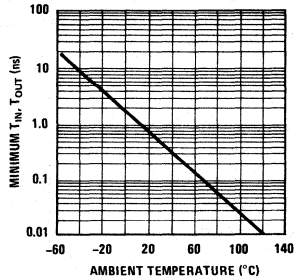
Note 5: Maximum frequency limited by maximum package power dissipation for MM4025, MM4026 and MM4027.

typical performance characteristics

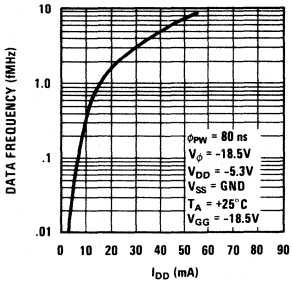
Typical Minimum Clock Frequency vs Temperature (Note 2)



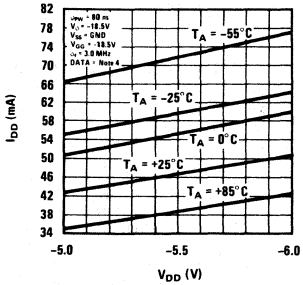
Typical Maximum T_1 and T_2 vs Temperature (Note 2)



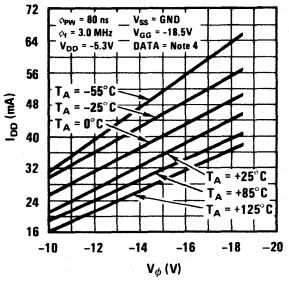
Power Supply Current vs Data Rate



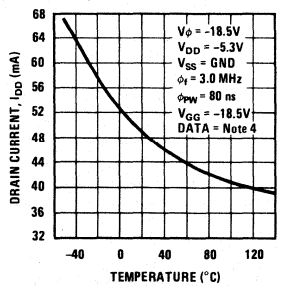
Power Supply Current vs V_{DD}



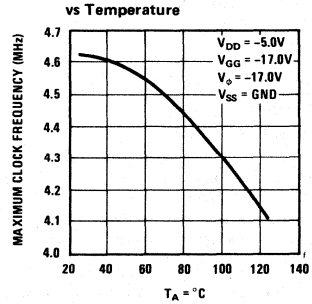
Power Supply Current vs Clock Voltage V_ϕ



Power Supply Current vs Temperature

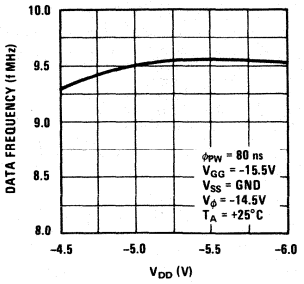


Maximum Clock Frequency vs Temperature

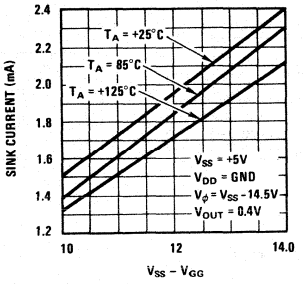


typical performance characteristics (con't)

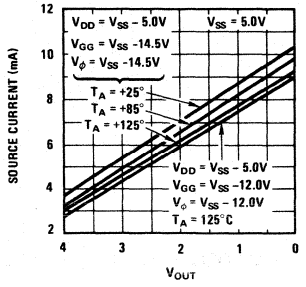
Maximum Data Rate vs V_{DD}



Typical Sink Current vs V_{GG}

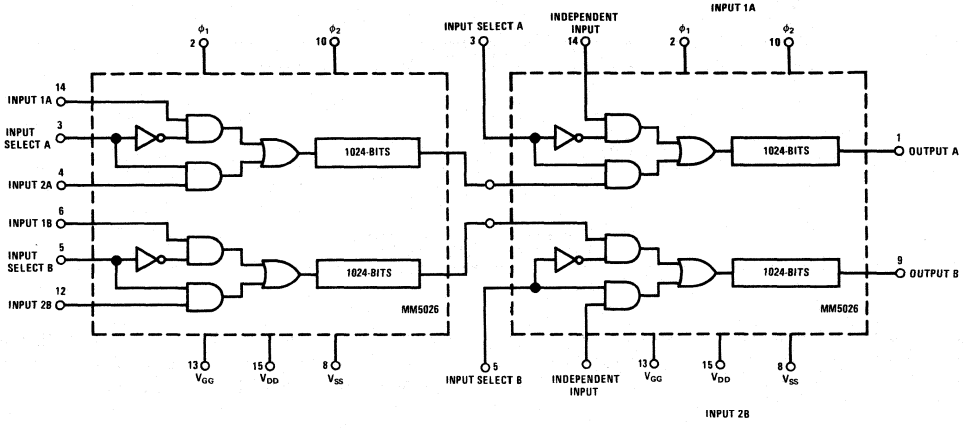


Typical Data Output Source Current vs Data Output Voltage

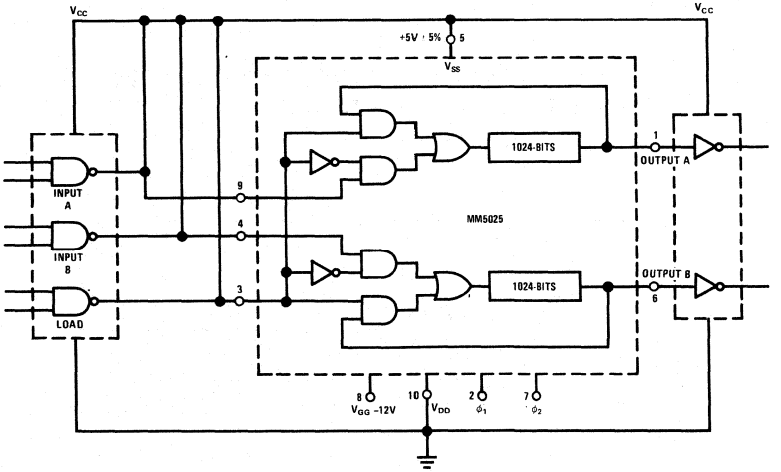


typical applications

Memory Expansion



TTL/MOS Interface



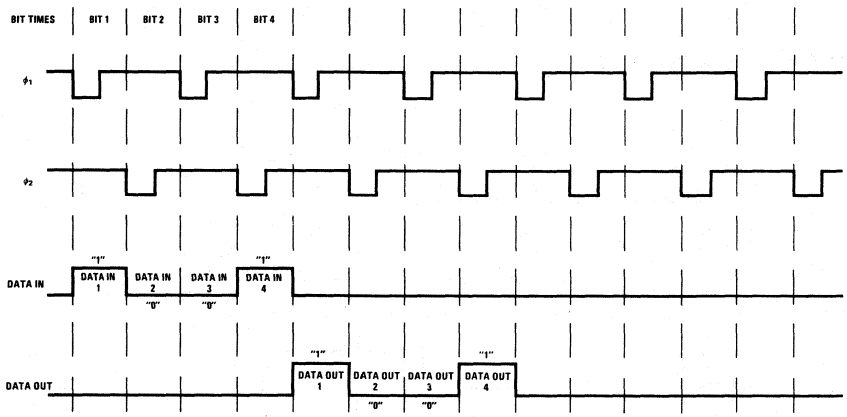
truth tables

Positive Logic
Logic "1" = V_{IH} = Logical High Level Logic "0" = V_{IL} = Logical Low Level

Write/Recirculate	Function
1	Recirculate
0	Load Data

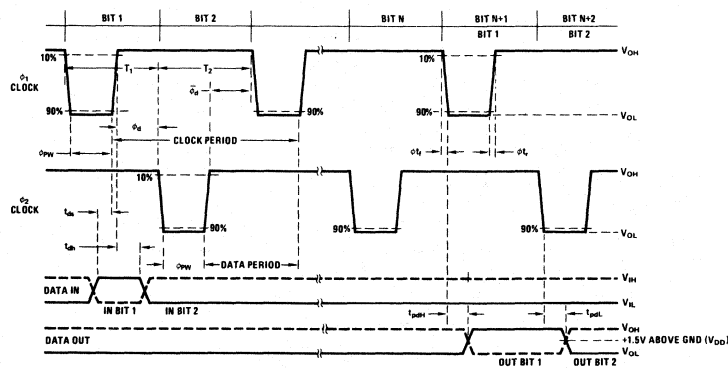
Input Select A	Function
1	Select Input 2A
0	Select Input 1A
Input Select B	**Function**
1	Select Input 2B
0	Select Input 1B

switching time waveforms



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exits at ϕ_1 time, (beginning on $\phi_{1's}$ negative going edge and ending on the succeeding $\phi_{2's}$ negative going edge).

timing diagram



MM5034, MM5035 Octal 80-Bit Static Shift Register

General Description

The MM5034 octal 80-bit shift register is a monolithic MOS integrated circuit utilizing N-channel low threshold enhancement mode and ion-implanted depletion mode devices.

The MM5034 is designed for use in computer display peripherals. All inputs and outputs are TTL compatible. The clocks and recirculate logic are internal to reduce system component count, and TRI-STATE® output buffers provide bus interface. Because of its N-channel characteristics, single 5V power supply operation is required.

Simple interface to the NSC CRT DP8350 controller and character generator to incorporate an entire CRT terminal is feasible with the MM5034.

The MM5034 is available in a 22-lead dual-in-line package.

The MM5035 is a 20-pin version of the MM5034 with the TRI-STATE output select feature omitted, for a simple data in/data out operation.

Features

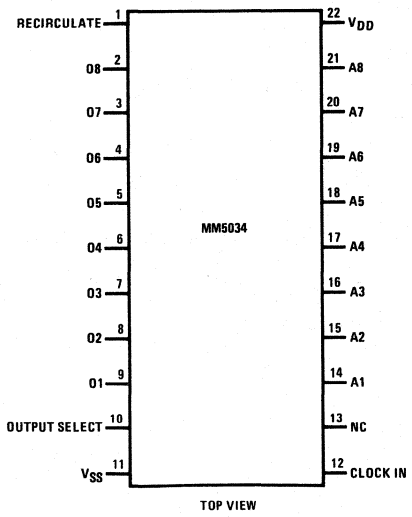
- Single 5V power supply
- Internal clocks
- High speed and static operation
- TRI-STATE output buffer
- Recirculate and output select independent

Applications

- CRT displays
- Computer peripherals

Connection Diagrams

Dual-in-Line-Package

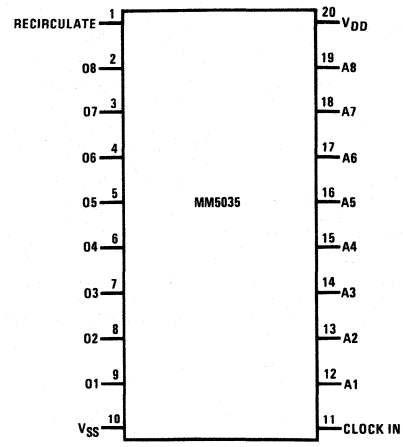


TOP VIEW

Order Number MM5034J
See NS Package J22A

Order Number MM5034N
See NS Package N22A

Dual-in-Line-Package



TOP VIEW

Order Number MM5035J
See NS Package J20B

Order Number MM5035N
See NS Package N20A

Absolute Maximum Ratings

Supply Voltage	7 V_{DC}
Input Voltage	7 V_{DC}
Power Dissipation	750 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics V_{DD} = 5V ±5%, T_A = 0°C to +70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input					
Logical "1" Input Voltage		V_{DD}−0.25			V
Logical "0" Input Voltage				0.4	V
Data and Control Inputs					
Logical "1" Input Voltage		2.0			V
Logical "0" Input Voltage				0.8	V
Data, Clock and Control Inputs					
Logical "1" Input Current	V_{IN} = 5V			5.0	μA
Input Capacitance	V_{IN} = 2.5V		5.0	8.0	pF
Outputs					
Logical "1" Output Voltage	I_{OUT} = 100 μA	2.4	2.8		V
Logical "0" Output Voltage	I_{OUT} = 1.6 mA		0.25	0.4	V
TRI-STATE Output Current	V_{OUT} = 5V			−5.0	μA
	V_{OUT} = 0V			5.0	μA
Supply Current			25	40	mA
Timing					
Clock Frequency		0		5.0	MHz
Clock Pulse Width High	*(Figure 1)*	80		10,000	ns
Clock Pulse Width Low	(Note 1)	80		∞	ns
Output Rise and Fall Time (t_r, t_f)	*(Figure 1)*		40	50	ns
Set-Up Time	*(Figure 1)*	100			ns
Hold Time	*(Figure 1)*	0			ns
Output Enable Time	*(Figure 1)*			100	ns
Output Disable Time	*(Figure 1)*			100	ns
Clock Rise and Fall Time	*(Figure 1)*			5.0	μs
Output Delay, (t_{PD})			80	120	ns

Note 1: The clock input must be at a low level for DC storage. Minimum pulse width assumes 10 ns t_r and t_f.

AC Test Circuits and Switching Time Waveforms

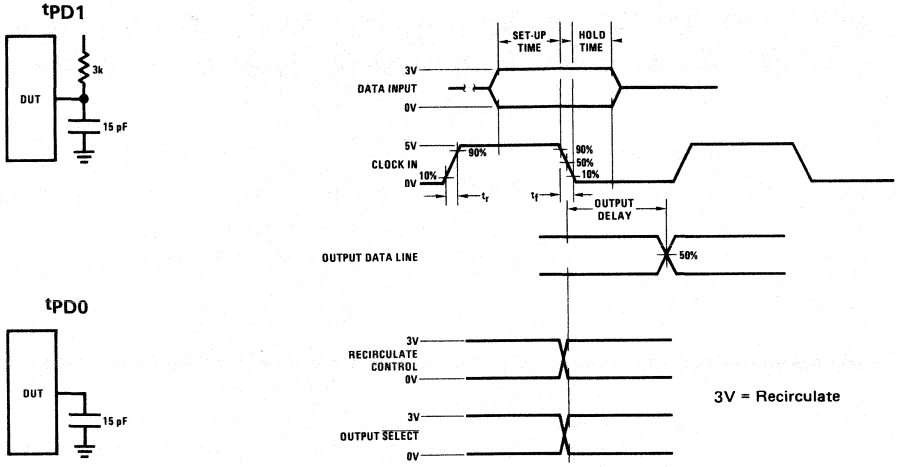


FIGURE 1

Typical Application

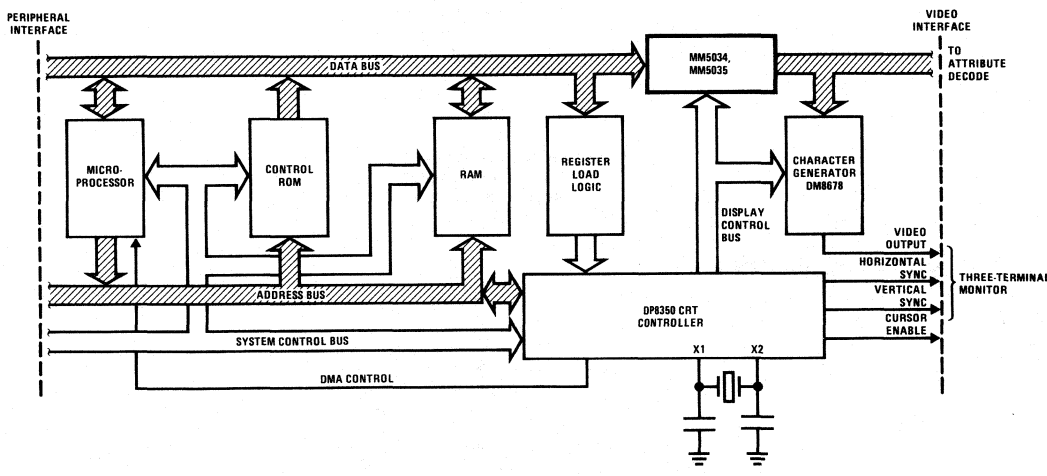


FIGURE 2. CRT System Diagram Using the MM5034, MM5035 as a Line Buffer with DMA

National Semiconductor

MM4052/MM5052 Dual 80-Bit Static Shift Register
MM4053/MM5053 Dual 100-Bit Static Shift Register

general description

The MM4052/MM5052 dual 80-bit and MM4053/MM5053 dual 100-bit static shift registers are monolithic integrated circuits utilizing P channel enhancement mode low threshold technology to achieve direct bipolar compatibility on the inputs and outputs. The devices require only a single phase clock.

features

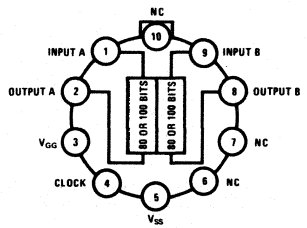
- Bipolar compatibility — +5, −12V operation; No pull-up or pull-down resistors needed
- High frequency operation — 1.6 MHz guarantee
- Single phase clock
- Improved drive capability — push-pull outputs

applications

- Static data buffer
- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

connection diagram

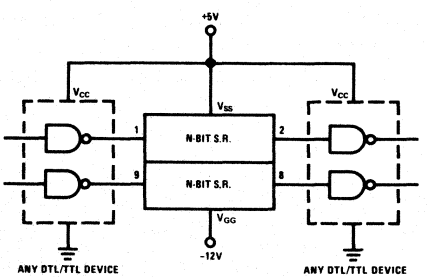
Metal Can Package



TOP VIEW

Order Number MM4052H, MM5052H, MM4053H or MM5053H
See NS Package H10A

typical application



absolute maximum ratings

Voltage @ Any Pin	V_{SS} +0.3V to V_{SS} −22V
Operating Temperature Range	
MM4052/MM4053	−55°C to +85°C (Ambient)
	−55°C to +125°C (Case)
MM5052/MM5053	0°C to +70°C (Ambient)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

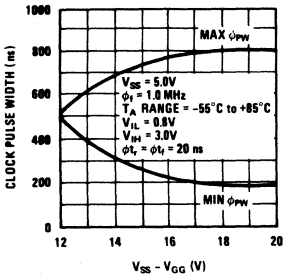
electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5% and V_{GG} = −12V ±10%, unless otherwise specified.

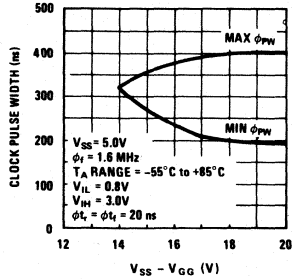
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 2.0			V
Logical Low Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C All other pins GND		.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1.0 MHz All other pins GND		3.0	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS}	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_{IN} = −20V, T_A = 25°C All other pins GND			1.0	μA
Clock Input Capacitance	V_{IN} = 0.0V, f = 1.0 MHz All other pins GND		22	28	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −500 μA	2.4V	4.8	V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA		−3.0	0.4	V
Logical High Level (V_{OH})	I_{SOURCE} = −10 μA	V_{SS} − 1.0	V_{SS}	V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 10 μA		V_{SS} − 12.0	V_{SS} − 7.0	V
Power Supply Current	T_A = 25°C ϕ_f = 1.6 MHz				
(I_{GG}) MM4052/MM5052	V_{GG} = V_{SS} − 17V $V_{\phi L}$ = V_{SS} − 17V		9.5	12.5	mA
(I_{GG}) MM4053/MM5053			12.0	16.0	mA
Propagation Delays from Clock					
Propagation Delay to a High (t_{pdH})	See waveform		200	300	ns
Propagation Delay to a Low (t_{pdL})	See waveform		200	300	ns
Clock Frequency (ϕ_f)	See operating curves	0		1.6	MHz
Clock Pulse Width (ϕ_{PW})	See operating curves $\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.25		10	μs
Clock Transition Times					
Risetime (ϕt_r)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			5	μs
Falltime (ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			5	μs
Data Input Setup Time (t_{ds})		80	50		ns
Data Input Hold Time (t_{dh})		20	0		ns

guaranteed performance characteristics

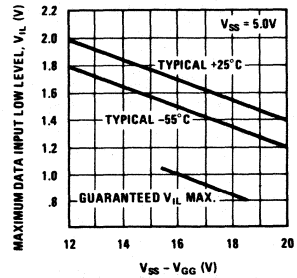
1.0 MHz Operating Curve



1.6 MHz Operating Curve

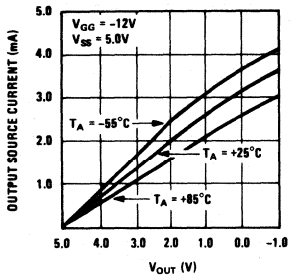


Maximum Data Input Low Level vs Supply Voltage

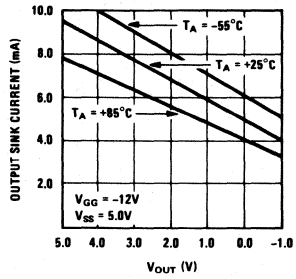


typical performance characteristics

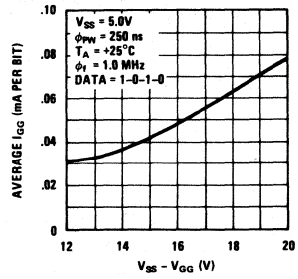
Data Output Source Current vs Data Output Voltage



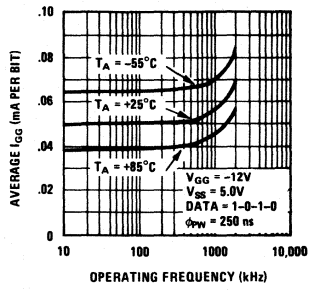
Data Output Sink Current vs Data Output Voltage



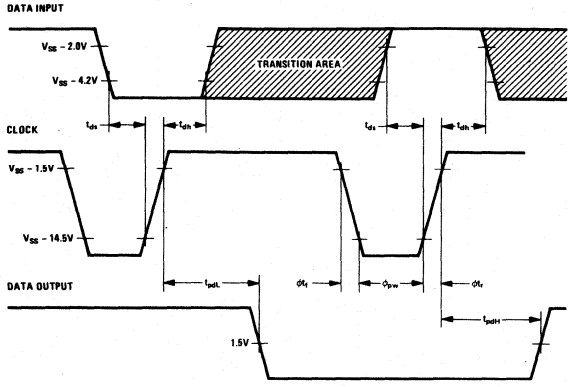
Power Supply Current



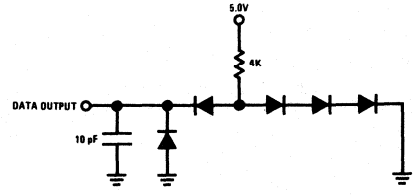
Power Supply Current



switching time waveforms



ac test circuit



National Semiconductor

MM5054 Dual 64/72/80-Bit Static Shift Register

general description

The MM5054 dual 80-bit static shift register is a monolithic MOS integrated circuit utilizing silicon gate low threshold technology to achieve complete bipolar compatibility. The device has input and output taps that also provide register lengths of 64 or 72 bits.

The single phase bipolar compatible clock lines may be driven by any conventional DTL or TTL circuit. The registers may be operated as a dual register by connecting the clock lines A and B together, or as two independent registers. Two clock control lines provide independent logical control of the shift register clock lines.

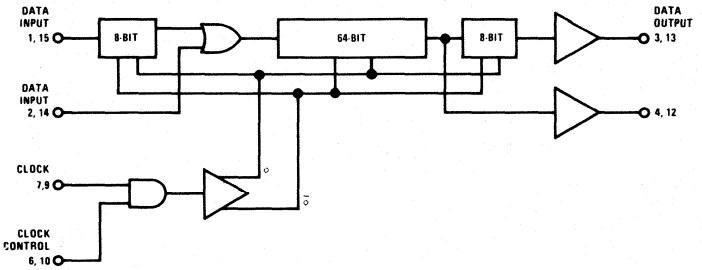
features

- Complete bipolar compatibility — DTL/TTL input/output and clock line compatibility without additional components
- Standard supplies — +5.0V, −12V
- High freq. operation — DC to 3.0 MHz typ
- Single phase clock — DTL/TTL compatible on-chip clock driver
- Low clock line capacitance — 8.0 pF max
- System flexibility — Split clock or common clock operation. Logical control of clock lines
- Low power dissipation — <600 μW/bit typ

applications

- Teletype data buffers
- Printer memory — 80, 128, 136, 144 bit lengths
- Telemetry and data sampling systems
- Serial memory storage

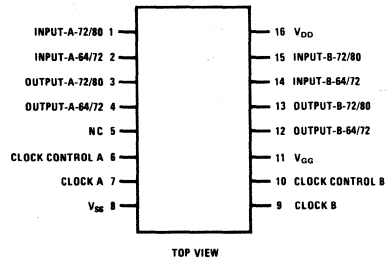
logic diagram



The unused data inputs and clock controls should be connected to V_{SS} to ensure proper operation.
Logic diagram shows 1/2 of the unit.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5054D
See NS Package D16C

Order Number MM5054N
See NS Package N16A

truth table

Positive Logic

CLOCK CONTROL	CLOCK
Low	Inhibited
High	Active

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 20V
Operating Ambient Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	600 mW @ 25°C

dc electrical characteristics

T_A within operating range, V_{GG} = −12V ±10%, V_{DD} = GND, V_{SS} = 5.0V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Clock Control, and Clock Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})				V_{SS} − 4.2	V
Input Leakages	V_{IN} = −10V, T_A = 25°C All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0V, f = 1.0 MHz All Other Pins GND (Note 1)		4.5	6.0	pF
Clock and Clock Control Capacitance	V_{IN} = 0V, f = 1.0 MHz (Note 1)		6.0	8.0	pF
Data Output Levels	(Figure 1)				
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA		0.15	0.4	V
Power Supply Current	ϕ_t = 1.5 MHz, T_A = 25°C				
(I_{GG} + I_{DD} = I_{SS}) I_{GG}	V_{SS} = 5.0V, V_{DD} = GND		7.0	10	mA
I_{DD}	V_{GG} = −12V		5.0	8.0	mA

ac electrical characteristics

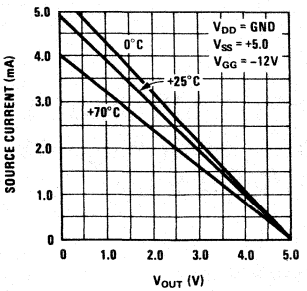
T_A within operating range, V_{GG} = −12V ±10%, V_{DD} = GND, V_{SS} = 5.0V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency (ϕ_f)	ϕt_r, $\phi t_f \leq$ 10 ns (Note 2)	DC	3.0	1.5	MHz
Clock Pulsewidth (ϕ_{PW})					
ϕ_{PW}	$\phi t_r = \phi t_f \leq$ 10 ns	0.25	0.180	10	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f \leq$ 10 ns	0.38			μs
Clock Transition Times					
Clock Risetime (ϕt_r)				500	ns
Clock Falltime (ϕt_f)				500	ns
Clock Control Setup Time (t_{CS})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	0			ns
Clock Control Hold Time (t_{ch})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	0			ns
Data Input Setup Time (t_{ds})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	60	30		ns
Data Input Hold Time (t_{dh})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	40	20		ns
Data Output Propagation Delay From Clock	(Figures 1 and 2) $\phi t_r = \phi t_f$ = 10 ns				
Delay to Output High Level (t_{pdH})			200	300	ns
Delay to Output Low Level (t_{pdL})			200	300	ns

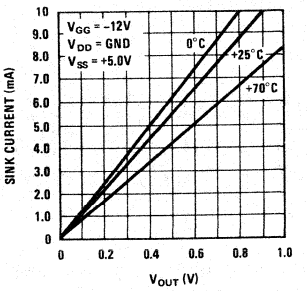
Note 1: Capacitance is guaranteed by periodic testing.
Note 2: For static operation clock must remain at V_{IL}.

typical performance characteristics

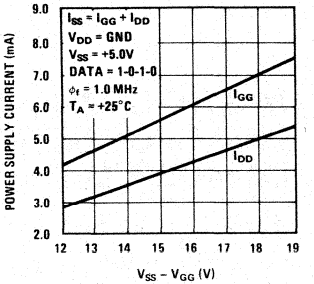
Typical Data Output Source Current vs Data Output Voltage



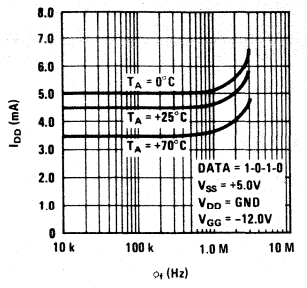
Typical Data Output Sink Current vs Data Output Voltage



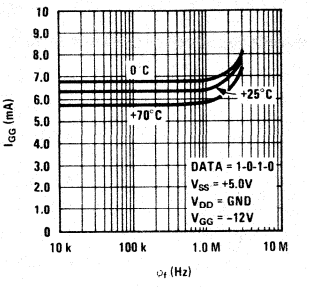
Typical Power Supply Current vs V_{GG}



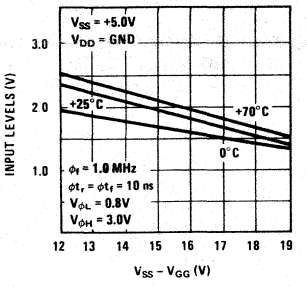
Typical I_{DD} vs Clock Frequency



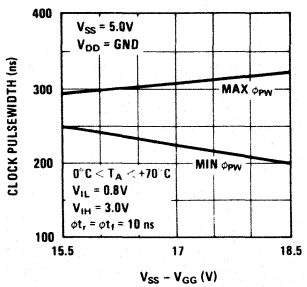
Typical I_{GG} vs Clock Frequency



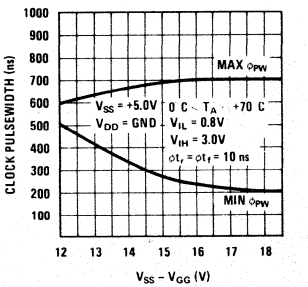
Typical Input Levels vs V_{GG}



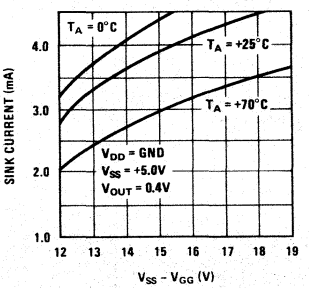
Typical 2.2 MHz Operating Curve



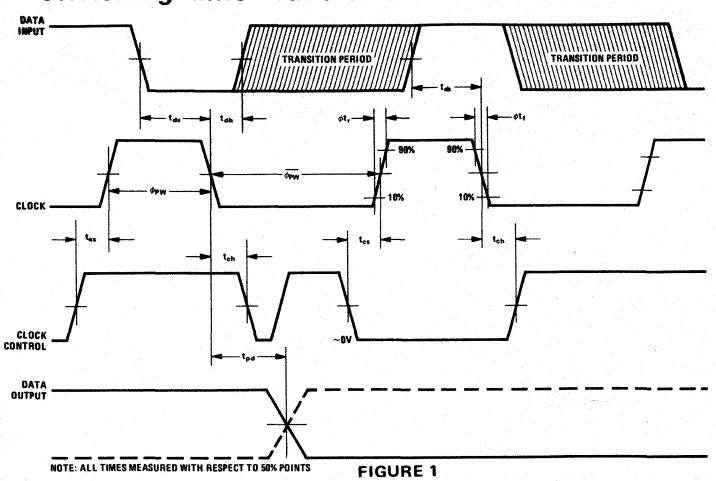
Typical 1.0 MHz Operating Curve



Typical Data Output Sink Current vs V_{GG}



switching time waveforms



NOTE: ALL TIMES MEASURED WITH RESPECT TO 50% POINTS

FIGURE 1

ac test circuit

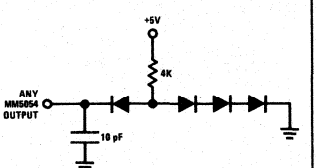


FIGURE 2

11

National Semiconductor

MM4055/MM5055 Quad 128-Bit Static Shift Register
MM4056/MM5056 Dual 256-Bit Static Shift Register
MM4057/MM5057 512-Bit Static Shift Register

general description

The MM4055/MM5055, MM4056/MM5056, MM4057/MM5057 512-bit static shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. They have a guaranteed operating frequency of 1.0 and 1.5 MHz respectively, and an on chip clock generator allows TTL level clock driver for complete TTL compatibility.

features

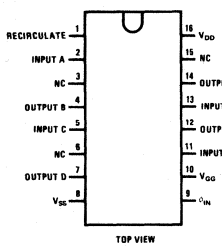
- Guaranteed operation
  - 1.5 MHz 0°C to +70°C
  - 1.0 MHz −55°C to +125°C
- Single TTL compatible clock, on chip clock generator
- Low clock capacitance 10 pF (typ)
- Operates from +5.0V, GND, and −12V
- Three configurations
  - MM4055/MM5055 Quad 128 bit
  - MM4056/MM5056 Dual 256 bit
  - MM4057/MM5057 Single 512 bit
- Internal recirculate

applications

- CRT displays
- Terminals
- Disk and drum replacements
- Buffer memory

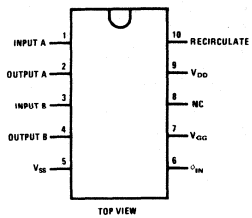
connection diagrams

Dual-In-Line Package



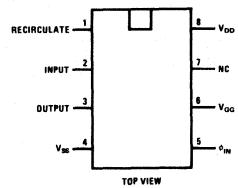
Order Number MM4055D or MM5055D
See NS Package D16C
Order Number MM5055N
See NS Package N16A

Dual-In-Line Package



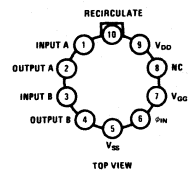
Order Number MM5056N
See NS Package N10B

Dual-In-Line Package



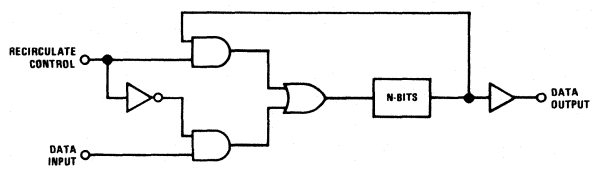
Order Number MM4057D or MM5057D
See NS Package D08C
Order Number MM5057N
See NS Package N08B

Metal Can Package



Order Number MM4056H or MM5056H
See NS Package H10A

logic diagram



absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ $T_A = 25°C$
Operating Temperature Range	
MM5055, MM5056, MM5057	0°C to 70°C
MM4055, MM4056, MM4057	−55°C to 125°C Case
Storage Temperature Range	−65°C to 160°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (MM4055, MM4056, MM4057)

$T_A = -55°C$ to $+125°C$, $V_{SS} = 5.0V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, $V_{DD} = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Recirculate and Clock Input Levels					
Logical High Level (V_{IH})		$V_{SS} - 1.0$		$V_{SS} + 0.3$	V
Logical Low Level (V_{IL})		$V_{SS} - 15$		$V_{SS} - 4.2$	V
Data, Recirculate and Clock Input Leakage	$V_{IN} = -10V$, $T_A = 25°C$ All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		4.5	6.0	pF
Recirculate Input Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		3.0	6.0	pF
Clock Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		10	14	pF
Data Output Levels					
Logical High Level (V_{OH})	$I_{SOURCE} = -0.5$ mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	$I_{SINK} = 1.6$ mA	V_{DD}		0.4	V
Power Supply Current	$T_A = 25°C$, $V_{GG} = -12V$, $V_{SS} = 5.0V$ $V_{DD} = 0V$, $\phi_{PW} = 230$ ns Data = 0-1-0-1 · · ·				
I_{GG}	$\phi_f \leq 0.1$ MHz		6.5	9.0	mA
	$\phi_f \leq 1.6$ MHz		10.5	15.5	mA
I_{DD} (Note 4)	$\phi_f \leq 0.1$ MHz		13	18	mA
	$\phi_f \leq 1.6$ MHz		15	20	mA
Clock Frequency (ϕ_f)	$\phi_{tr}, \phi_{tf} \leq 10$ ns (Note 5)		2.2	1.0	MHz
Clock Pulse Width					
(ϕ_{PW})	$\phi_{tr}, \phi_{tf} \leq 10$ ns (See ac Test Circuit)	0.400	0.280	10	μs
$(\overline{\phi_{PW}})$	$\phi_{tr}, \phi_{tf} \leq 10$ ns (See ac Test Circuit)	0.400	0.160	dc	μs
Data Input Setup Time (t_{ds})	$t_r, t_f \leq 10$ ns For Load Conditions See ac Test Circuit	260			ns
Data Input Hold Time (t_{dH})		120			ns
Recirculate Setup Time (t_{ds})		260			ns
Recirculate Hold Time (t_{dH})		120			ns
Data Output Propagation Delay					
Delay to High Level (t_{pdH})			350	700	ns
Delay to Low Level (t_{pdL})			350	700	ns

electrical characteristics (con't) (MM5055, MM5056, MM5057)

$T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, $V_{DD} = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Recirculate and Clock Input Levels					
Logical High Level (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 0.3$	V
Logical Low Level (V_{IL})		$V_{SS} - 15$		$V_{SS} - 4.2$	V
Data, Recirculate and Clock Input Leakage	$V_{IN} = -10V$, $T_A = 25°C$ All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		4.5	6.0	pF
Recirculate Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		3.0	6.0	pF
Clock Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		10	14	pF
Data Output Levels					
Logical High Level (V_{OH})	$I_{SOURCE} = -0.5$ mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	$I_{SINK} = 1.6$ mA	V_{DD}		0.4	V
Power Supply Current	$T_A = 25°C$, $V_{GG} = -12V$, $V_{SS} = 5.0V$ $V_{DD} = 0V$, $\phi_{PW} = 230$ ns Data = 0-1-0-1 • • •				
I_{GG}	$\phi_f \leq 0.1$ MHz		6.5	9.0	mA
	$\phi_f \leq 2.2$ MHz		13	19	mA
I_{DD} (Note 4)	$\phi_f \leq 0.1$ MHz		13	18	mA
	$\phi_f \leq 2.2$ MHz		15	20	mA
Clock Frequency (ϕ_f)	$\phi_{tr}, \phi_{tf} \leq 10$ ns (Note 5)		3.0	1.5	MHz
Clock Pulse Width					
(ϕ_{PW})	$\phi_{tr}, \phi_{tf} \leq 10$ ns	0.230	0.100	100	μs
(ϕ_{PW})	$\phi_{tr}, \phi_{tf} \leq 10$ ns	0.300	0.100	dc	μs
Data Input Setup Time (t_{ds})	$t_r, t_f \leq 10$ ns For Load Conditions See Test Circuit	110			ns
Data Input Hold Time (t_{dH})		40			ns
Recirculate Setup Time (t_{ds})		110			ns
Recirculate Hold Time (t_{dH})		40			ns
Data Output Propagation Delay					
Delay to High Level (t_{pdH})			250	345	ns
Delay to Low Level (t_{pdL})			250	345	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

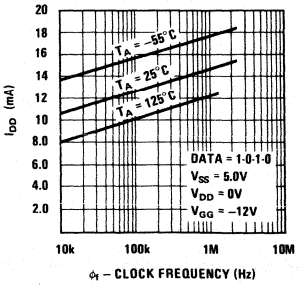
Note 3: Positive true logic notation is used:
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: Outputs not loaded when measuring I_{DD}. Add 1.6 mA to I_{DD} for each TTL load to compute worst case power.

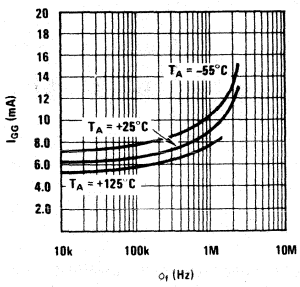
Note 5: For static operation clock must remain at V_{IL}.

typical performance characteristics

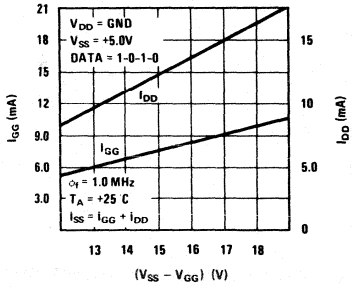
Typical I_{DD} vs Clock Frequency



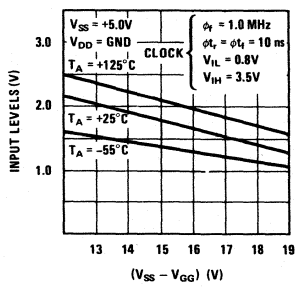
Typical I_{GG} vs Clock Frequency



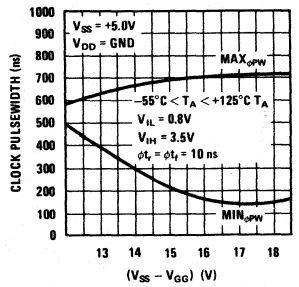
Typical Power Supply Current vs V_{GG}



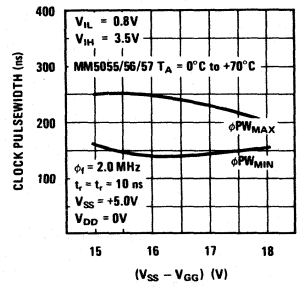
Typical Input Levels vs V_{GG}



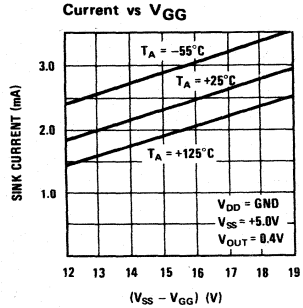
Typical 1.0 MHz Operating Curve



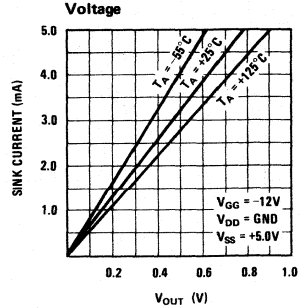
Typical 2.0 MHz Operating Curve



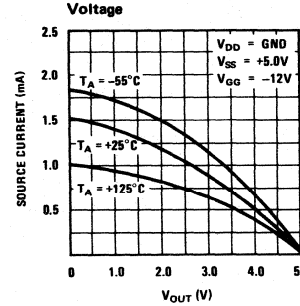
Typical Data Output Sink Current vs V_{GG}



Typical Output Sink Current vs Data Output Voltage

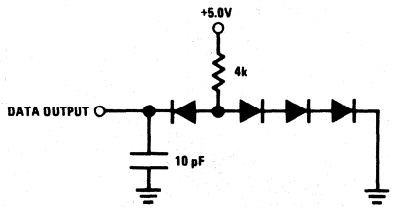


Typical Data Output Source Current vs Data Output Voltage

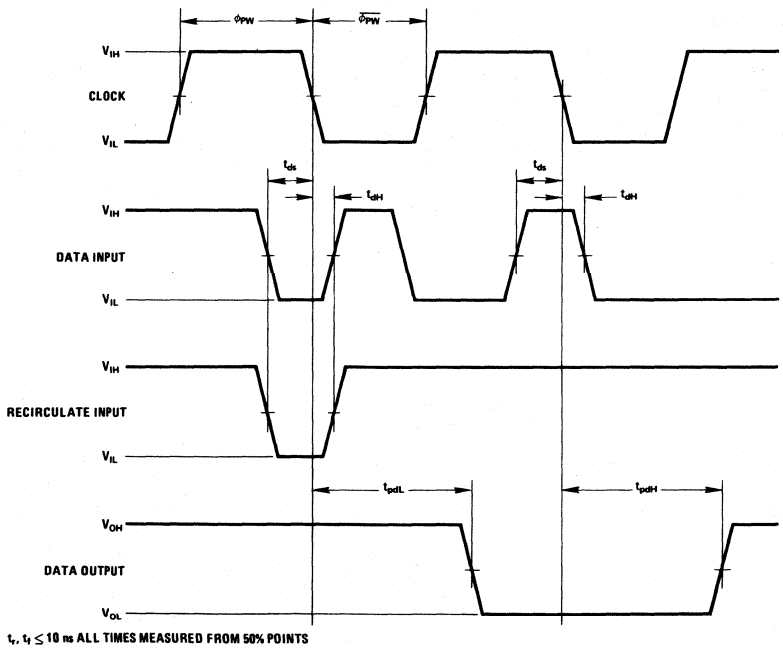


11

test circuit



switching time waveforms



$t_r, t_f \leq 10$ ns ALL TIMES MEASURED FROM 50% POINTS

MM5058 1024-Bit Static Shift Register

general description

The MM5058 is a monolithic 1024-bit static shift register utilizing a low threshold P-channel silicon gate technology to achieve bipolar compatibility. "Stream select" logic on the chip chooses between two inputs, facilitating external recirculate operation. This in addition to an internal clock-driver, thus providing a single external TTL/DTL clock, makes this device flexible and convenient to integrate into existing TTL/DTL or MOS systems.

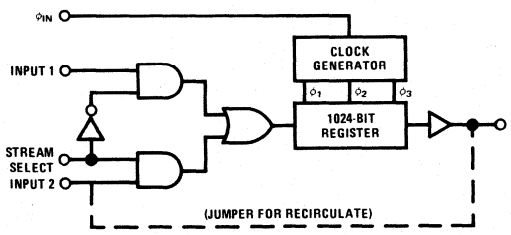
features

- Bipolar compatibility — All inputs, outputs, and clock interface directly with standard TTL/DTL circuits with no external components
- Single phase clock — On chip clock driver provides single TTL/DTL level clock with low input capacitance
- High frequency operation — DC to 1.5 MHz guaranteed
- Standard power supplies — +5.0V and −12V
- Small package — 8-pin mini DIP
- Low power consumption — 250μW/bit typ
- Stream select for easy external recirculate

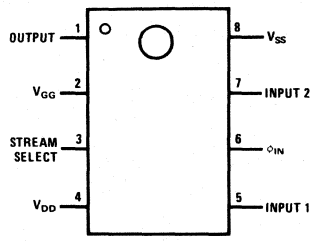
applications

- Sequential access memories
- Static buffer memories
- CRT refresh
- Delay lines
- Drum memory replacement

logic and connection diagrams



Dual-In-Line Package

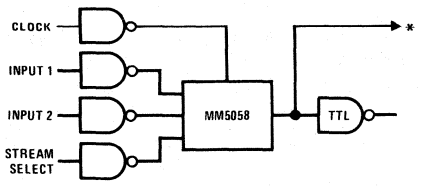


TOP VIEW

Order Number MM5058D
See NS Package D08C

Order Number MM5058N
See NS Package N08B

ac test circuit



*PROPAGATION DELAYS MEASURED AT MM5058 OUTPUT.

truth table

STREAM SELECT	FUNCTION
LOGIC "0"	INPUT 1
LOGIC "1"	INPUT 2

absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to -20V
Power Dissipation	535 mW @ T_A = 25°C
Operating Temperature Range	0°C to +70°C Ambient
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within specified operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Input Leakage (All Inputs)	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.05	0.5	μA
Input Capacitance (Note 2)	V_{IN} = 0V, f = 1.0 MHz (Note 1) All Other Pins (GND)		3.0	7.0	pF
Data Output Levels, TTL Load					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4	3.5		V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA	V_{DD}		0.4	V
Power Supply Current	DATA = 0-1-0-1				
I_{GG}	ϕ_f = 1.5 MHz Continuous Operation		8.0	13	mA
I_{SS}	DATA = 0-1-0-1 ϕ_f = 1.5 MHz Continuous Operation		38	60	mA

ac electrical characteristics

T_A within specified operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 10 ns		3.0	1.5	MHz
Clock Pulse Width					
ϕ_{PW}	$\phi t_r = \phi t_f$ = 10 ns	0.350	0.100	100	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f$ = 10 ns	0.250		DC	μs
Clock Pulse Transition (t_r, t_f)				1.0	μs
Data Input Setup Time (t_{DS})	$t_r = t_f \leq$ 10 ns See AC Test Circuit for Load Conditions	100			ns
Data Input Hold Time (t_{DH})		30			ns
Stream Select Setup Time (t_{SS})		150			ns
Stream Select Hold Time (t_{SH})		30			ns
Data Output Propagation Delay From ϕ_{IN}					
Delay to High Level (t_{pdH})			200	300	ns
Delay to Low Level (t_{pdL})			200	300	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

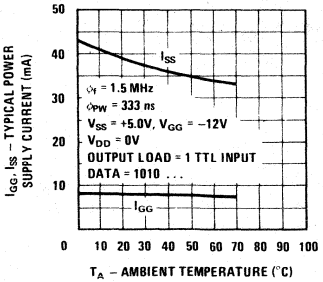
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level; Logic "0" = most negative voltage level.

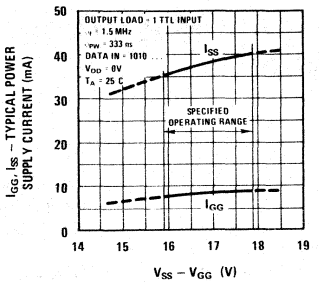
Note 4: Typical values apply for V_{SS} = 5.0V, V_{GG} = −12V, V_{DD} = 0V, and T_A = 25°C.

typical performance characteristics

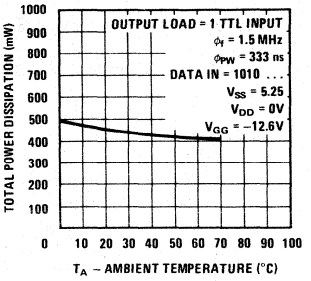
Typical Power Supply Current vs Temperature



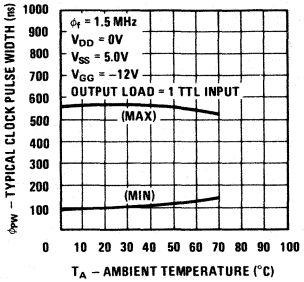
Typical Power Supply Current vs Supply Voltage



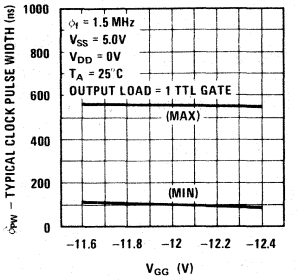
Guaranteed Power Consumption vs Temperature



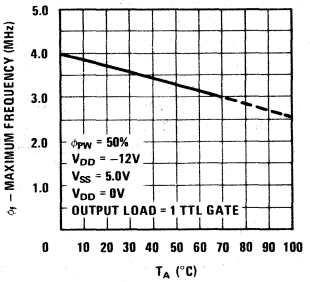
Typical Clock Pulse Width vs Ambient Temperature



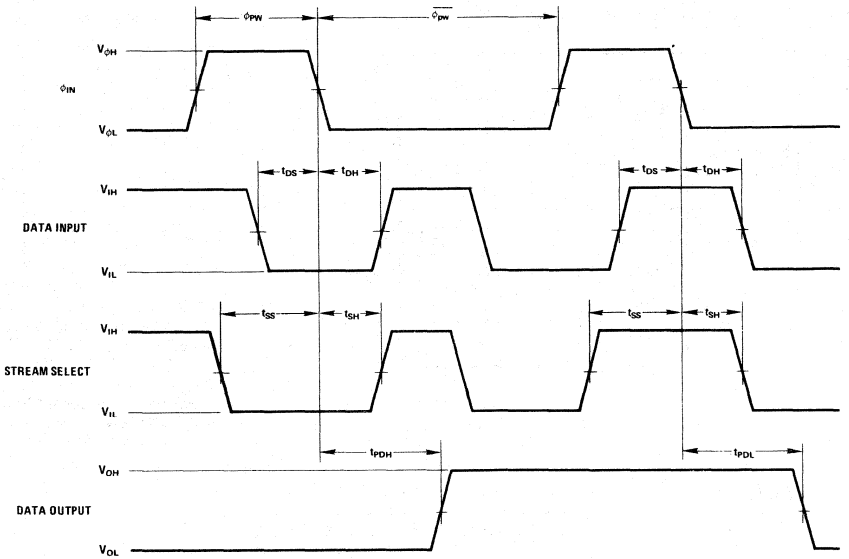
Typical Clock Pulse Width vs V_{GG}



Typical Maximum Frequency vs Ambient Temperature



switching time waveforms



NOTE 1: TIMES MEASURED AT 50% POINTS WITH t_r, $t_f \leq 10$ ns.
NOTE 2: FOR DC STORAGE CLOCK MUST REMAIN AT V_{OL}.

National Semiconductor

MM5060 Dual 144-Bit Mask Programmable Static Shift Register

general description

The MM5060 is a monolithic dual 144-bit static shift register/accumulator utilizing a silicon gate low threshold P-channel enhancement mode technology to achieve complete bipolar compatibility. The device can be programmed by metal mask option to custom lengths from 125 to 144-bits in one bit increments.

Standard Lengths:

MM5060AA
Dual 128-Bit Shift Register/Accumulator
MM5060AB
Dual 132-Bit Shift Register/Accumulator
MM5060AC
Dual 133-Bit Shift Register/Accumulator
MM5060AD
Dual 144-Bit Shift Register/Accumulator

Custom Lengths:

The programmed shift registers are assigned a letter code for each option. These are designated by a pair of letters after the number code but before the package designation such as MM5060AD/D which is a 0°C to +70°C dual 144-bit shift register/accumulator in an 8-lead cavity dual-in-line package. Pattern codes are assigned by National upon entry of order.

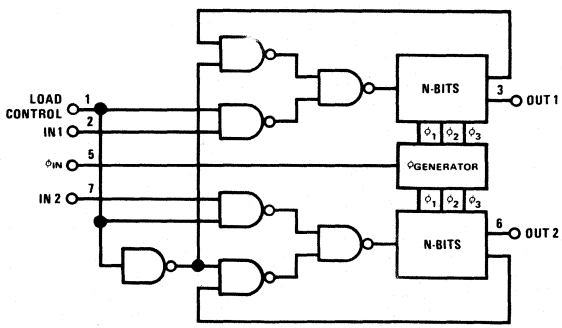
features

- Complete bipolar compatibility — input/output and clock input completely DTL/TTL compatible without additional components
- Standard Supplies +5V, −12V
- High frequency operation — DC to 3.0 MHz typical
- Single phase clock — DTL/TTL compatible on chip clock
- Low clock line capacitance 6.0 pF max.

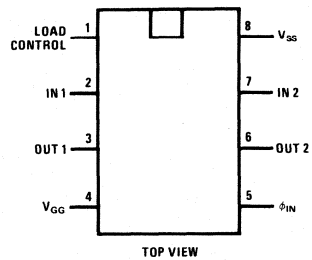
applications

- Printer memory — any length from 125 to 144-bits per line
- Telemetry systems and data sampling
- Serial memory storage

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5060AA/D, MM5060AB/D, MM5060AC/D, MM5060AD/D or MM5060XX/D
See NS Package D08C

Order Number MM5060AA/N, MM5060AB/N, MM5060AC/N, MM5060AD/N or MM5060XX/N
See NS Package N08B

truth table

LOAD CONTROL	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ T_A = 25°C
Operating Temperature Range	
MM5060	0°C to +70°C (Ambient)
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

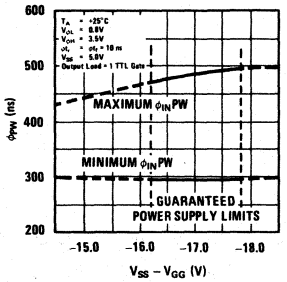
T_A within specified operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} −12.0V ±5%, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10.0		V_{SS} − 4.2	
Data Input Leakage	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.0	5.0	pF
Load Control Input Levels					
Logical High Level (V_H)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_L)		V_{SS} − 10.0		V_{SS} − 4.2	V
Load Control Input Leakage	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 10.0		V_{SS} − 4.2	V
Clock Input Leakage	V_ϕ = −10.0V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.5	6.0	pF
Data Output Levels TTL Load					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	3.0	3.5		V
Logical High Level MOS Load (V_{OH})	I_{SOURCE} = −0.01 mA	4.0	4.5		V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current (I_{GG})	T_A = 25°C, V_{GG} = −12V ϕ_{PW} = 300 ns, V_{SS} = +5.0V Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		20.0	24.0	mA
	ϕ_f = 1.0 MHz		21.0	25.0	mA
	ϕ_f = 1.5 MHz		22.0	26.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 10 ns, T_A = 25°C	DC	3.0	1.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r = \phi t_f$ = 10 ns, T_A = 25°C	0.300	0.100	100	μs
($\overline{\phi_{PW}}$)		0.200		DC	μs
Clock Pulse Transition (ϕt_r, ϕt_f)				1	μs
Data Input Setup Time (t_{ds})	T_A = 25°C, t_r, t_f = 10 ns	70			ns
Data Input Hold Time (t_{dh})	T_A = 25°C, t_r, t_f = 10 ns	50			ns
Load Control Setup (t_{ds})	T_A = 25°C, t_r, t_f = 10 ns	70			ns
Load Control Hold (t_{dh})	T_A = 25°C, t_r, t_f = 10 ns	50			ns
Data Output Propagation Delay from ϕ in	T_A = 25°C, t_r, t_f = 10 ns				
Delay to High Level (t_{pdH})			250	350	ns
Delay to Low Level (t_{pdL})			250	350	ns

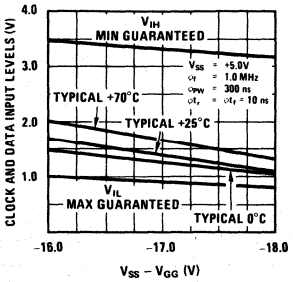
Note 1: Capacitance is guaranteed by periodic testing.

typical performance characteristics

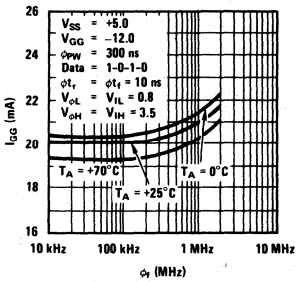
Guaranteed 1.5 MHz Operating Curve



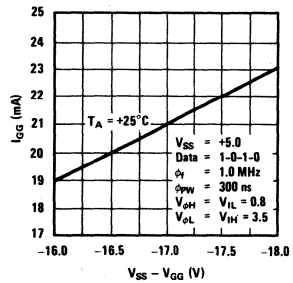
Guaranteed Input Voltage Levels vs Supply Voltage



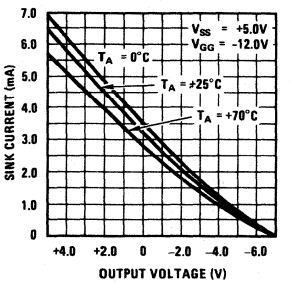
Typical I_{GG} vs Clock Frequency Under TTL Load



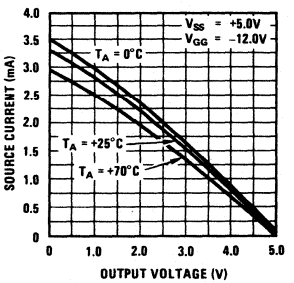
Typical Power Supply Current vs Voltage Under TTL Load



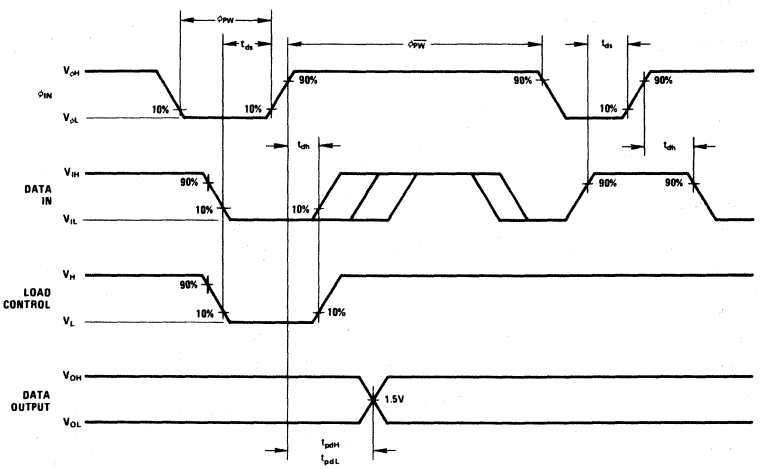
Typical Output Sink Current vs Output Voltage



Typical Output Source Current vs Output Voltage



switching time waveforms



Note: DC storage is accomplished during ϕ_{PW} time.

National Semiconductor

MM5061 Quad 100-Bit Static Shift Register

general description

The MM5061 quad 100-bit static shift register is a MOS monolithic integrated circuit using silicon gate technology to achieve bipolar compatibility. It has a guaranteed operating frequency of 1.5 MHz and an on-chip clock generator.

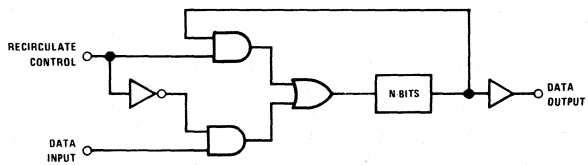
features

- Guaranteed 1.5 MHz operation
- Single TTL compatible clock on chip clock generator
- Low clock capacitance 10 typ, 14 max.
- Operates from +5V, GND, and -12V
- Configuration Quad 100-bit
- Internal recirculate

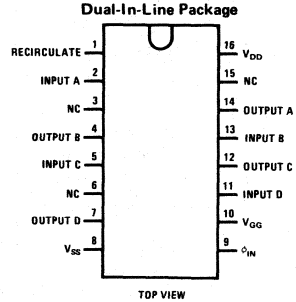
applications

- CRT displays
- Terminals
- Disk and drum replacements
- Buffer memory

logic and connection diagrams



Dual-In-Line Package

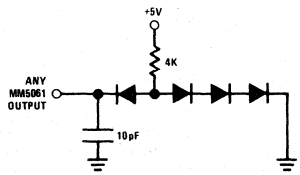


TOP VIEW

Order Number MM5061D
See NS Package D16C

Order Number MM5061N
See NS Package N16A

test circuit



truth table

RECIRCULATE CONTROL	FUNCTION
1	Data Recirculates
0	Register Accepts Input Data

absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ T_A = 25°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = −12V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Level					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance (Note 2)	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND		4.5	6.0	pF
Recirculate Input Levels					
Logical High Level (V_H)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_L)		V_{SS} − 10		V_{SS} − 4.2	V
Recirculate Input Leakage	V_{IN} = 10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Recirculate Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND		3.0	6.0	pF
Clock Input Levels					
Logical High Level (V_{OH})		V_{SS} - 1.0		V_{SS} + 0.3	V
Logical Low Level (V_{OL})		V_{SS} - 10.0		V_{SS} − 4.2	V
Clock Input Leakage	V_ϕ = −10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Clock Capacitance (Note 2)			10.0	14.0	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −3.0 mA	2.85		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current (I_{GG})	T_A = 25°C, V_{GG} = −12.0V, ϕ_{PW} = 160 ns V_{SS} = +5.0V, V_{OL} = 0.8V, Data = 0·1·0·1 V_{DD} = 0.0V				
	$\phi_f \leq$ 0.1 MHz		6.5	9.0	mA
	ϕ_f = 2.2 MHz		13.0	19.0	mA
(I_{DD})(Note 4)	$\phi_f \leq$ 0.1 MHz		13.0	18.0	mA
	$\phi_f \leq$ 2.2 MHz		15.0	20.0	mA
Clock Frequency ϕ_f	$\phi t_r = \phi t_f \leq$ 10 ns		3.0	1.5	MHz
Clock Pulse Width ϕ_{PW}	$\phi t_r = \phi t_f \leq$ 10 ns	0.230	0.100	10.0	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f \leq$ 10 ns	0.200		DC	μs
Data Input Setup Time (t_{dS})	t_r, $t_f \leq$ 10 ns For Load Conditions see Test Circuit	100			ns
Data Input Hold Time (t_{dH})		40			ns
Recirculate Setup (t_{dS})		100			ns
Recirculate Hold (t_{dH})		40			ns
Data Output Propagation Delay from ϕ					
Delay to High Level (t_{pdH})			250	350	ns
Delay to Low Level (t_{pdL})			250	350	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

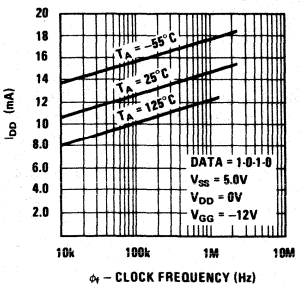
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level; Logic "0" = most negative voltage level.

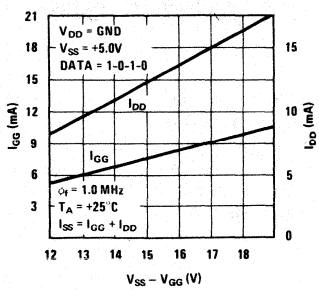
Note 4: Outputs not loaded when measuring I_{DD} therefore I_{DD} will increase by 1.6 mA for each TTL load (TTL "0" level output).

typical performance characteristics

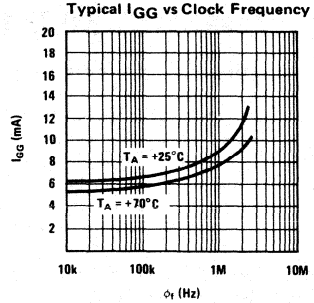
Typical I_{DD} vs Clock Frequency



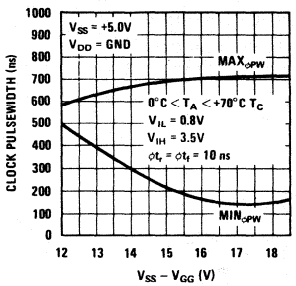
Typical Power Supply Current vs V_{GG}



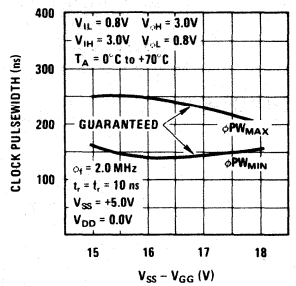
Typical I_{GG} vs Clock Frequency



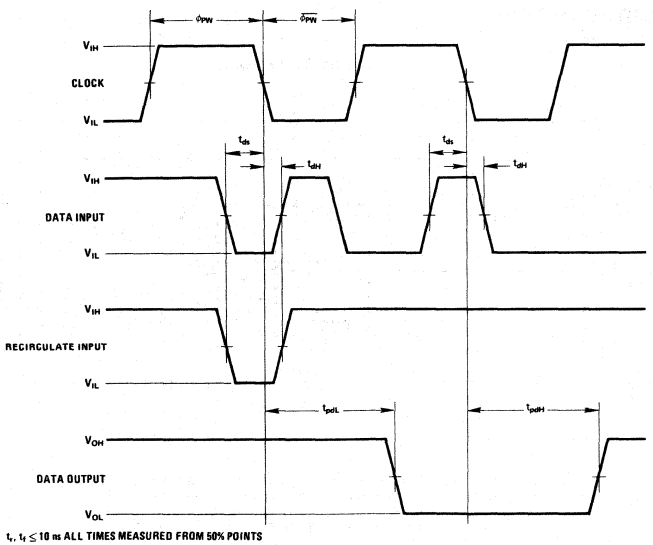
Guaranteed 1.0 MHz Operating Curve



Guaranteed 2.0 MHz Operating Curve



switching time waveforms



$t_r, t_f \leq 10$ ns ALL TIMES MEASURED FROM 50% POINTS

National Semiconductor

MM4104/MM5104 Dynamic Shift Register

general description

The MM4104/MM5104 360/359, 228/287, 40/32 bit dynamic shift register is a monolithic MOS integrated circuit utilizing p-channel enhancement mode low threshold technology to achieve bipolar compatibility. The register lengths are lengthened or shortened by hard wiring the length select line to V_{GG} or V_{SS}. The lengths available are: 40, 288, 328, 360, 400, 560, 688; or 32, 287, 319, 359, 391, 446, 678.

features

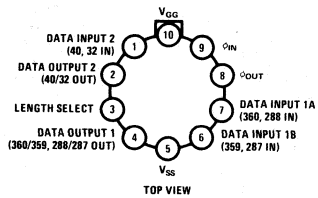
- DTL/TTL compatibility — +5V, −12V power supply. No pull-up or pull-down resistors required
- Multiple length registers — Electrically adjustable 360/359, 288/287, 40/32 bit registers
- Wide frequency range — 250 Hz min. guar. at 25°C; 2.5 MHz max. guar. over temp.

applications

- Data store
- CRT displays
- Business machine

connection diagram

Metal Can Package

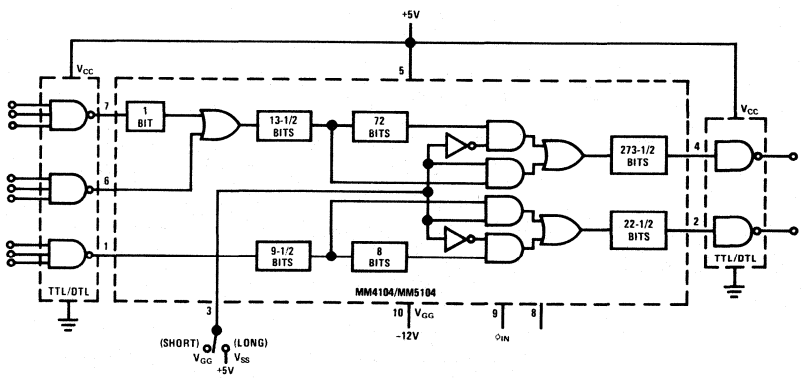


TOP VIEW

Order Number MM4104H or MM5104H
See NS Package H10A

typical applications

TTL/MOS Interface



Note: V_{GG} on pin 3 results in a 288-bit register between pin 7 and pin 4 and a 287-bit register between pins 6 and 4. The unused input (6 or 7) must be returned to V_{SS}. Also, there is a 32-bit register between pins 1 and 2.

V_{SS} on pin 3 results in a 360 bit register between pin 7 and pin 4 and a 359-bit register between pins 6 and 4. The unused input (6 or 7) must be returned to V_{SS}. Also, there is a 40-bit register between pins 1 and 2.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range MM4104	−55°C to 125°C
MM5104	−25°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

(T_A within operating temperature range, V_{SS} = +5.0V, ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} −4.2	V
Data Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		3.0	5.0	pF
Length Select Input Levels					
Logical HIGH Level (V_{LSH})		V_{SS}		V_{SS} + 0.3	V
Logical LOW Level (V_{LSL})		V_{SS} − 18.5		V_{GG}	V
Length Select Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Length Select Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		6.0	9.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} −18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		85	100	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.5	2.5	mA
	ϕ_f = 1 MHz		3.5	5.0	mA
	ϕ_f = 2.5 MHz		7.0	10.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	(Note 1)	10			ns
Clock Transition Time (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1	μs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit.				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

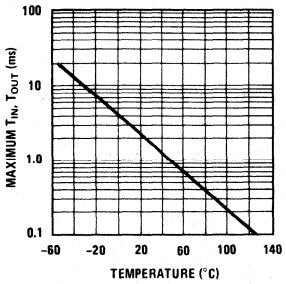
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

Note 2: The curves are guaranteed by testing at a high temperature point.

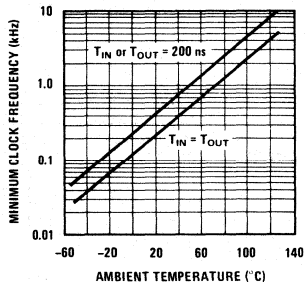
Note 3: Capacitance is guaranteed by periodic testing.

performance characteristics

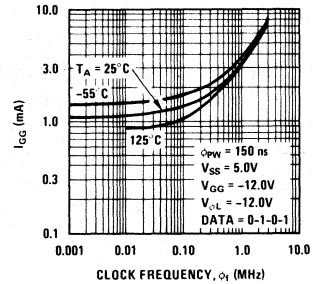
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Notes 1, 2)



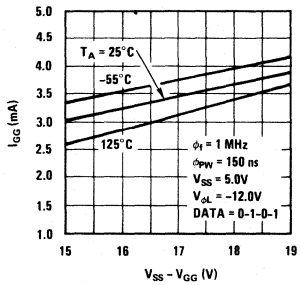
Guaranteed Minimum Clock Frequency vs Temperature (Notes 1, 2)



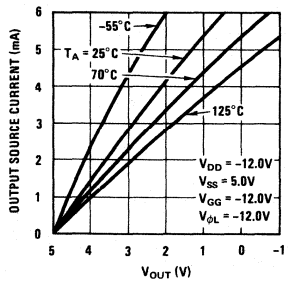
Typical Power Supply Current vs Clock Frequency



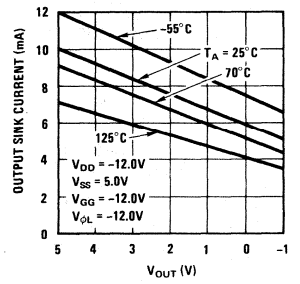
Typical Power Supply Current vs V_{GG}



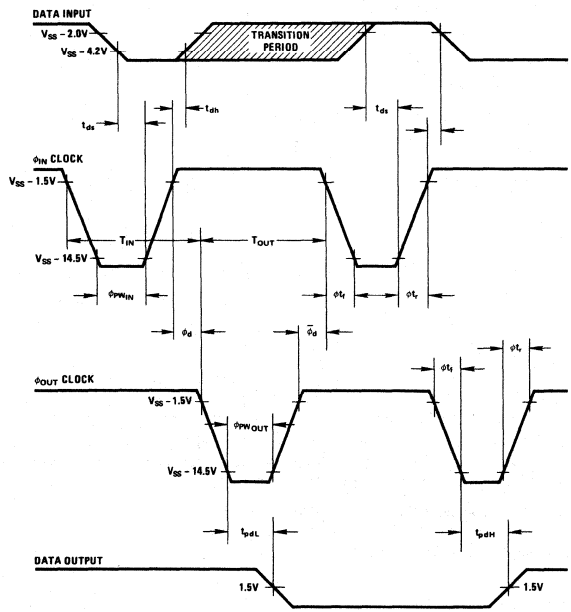
Typical Output Source Current vs Voltage



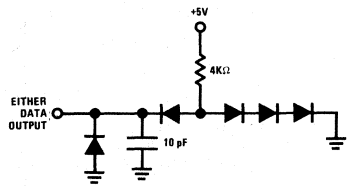
Typical Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Section 12

Memory Support Circuits

12

National offers a complete line of memory drivers, buffers, sense amps, voltage comparators, and other interface circuits. This section provides data on several frequently used interface devices. Refer to National's Interface Integrated Circuits Databook for additional data on our complete line of interface devices.

National offers a selection of memory support circuits to facilitate the interface of memory components in systems architecture. The memory support circuits were developed specifically to accommodate the addressing, clocking, data I/O, and control signals associated with memory systems application as shown in figure 1. Additional circuits are available to interface with data bus structured computers and microprocessors. For additional information contact National's Interface Product Marketing Manager.

FEATURES OF THE TTL LEVEL MOS DRIVERS

Figure 2 compares the switching response of the DS3628 with a 74S TTL gate. Two features can be observed from the switching waveforms: 1) the DS3628 is as fast as the 74S TTL driving TTL loads, and 2) the output high level (V_{OH}) of the DS3628 is higher than that of the 74S TTL.

In a memory system composed of MOS RAMs the load is capacitive and not resistive. Figure 3 compares the switching response of the DS3628 with a 74S TTL gate driving capacitive loads of 50 pF, 150 pF, and 300 pF. The switching waveforms show that the fall time of the DS3628 is as fast as or faster than those of the 74S TTL, but most obvious is the rise time of the DS3628 – much faster than that of the 74S TTL. In addition, the 74S has an objectionable glitch in its rise time. The output high (V_{OH}) level of the DS3628 is higher driving capacitance due to a bootstrap effect in the circuit.

The switching response of the circuits interfacing with a memory array is important since any delay subtracts from the overall memory access time. The switching response driving a capacitive load is more important; as an example, the address drivers might be expected to drive 420 pF in a memory containing 64 MOS RAMs with 5 pF input capacitance each plus 100 pF of board capacitance. The same is typical of clock signals, select signals, and read/write signals.

The input logic levels of MOS RAMs are generally higher than TTL gate levels (typically 400 mV higher). Therefore, the higher output high level (V_{OH}) of the DS3628 is preferable for noise immunity and switching overdrive.

The features of the DS3628 are typical of the other TTL level memory support circuits shown in the Selection Guide.

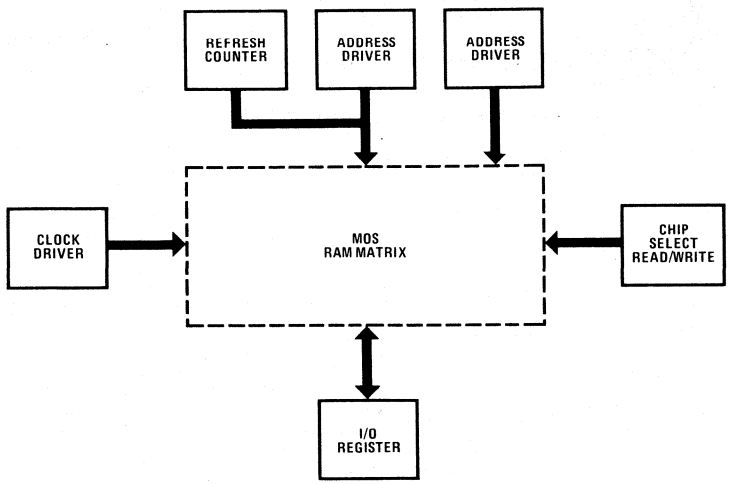


Figure 1. Memory System Block Diagram

DAMPING RINGING OF CLOCK SIGNALS

Ringing of clock signals in a system where the logic fan-out is less than 10 is not generally a big problem, but with higher fan-out the increased capacitive load associated with even a small amount of wiring inductance is a problem. When the capacitance is small the switching currents are small, but as the load increases the increased current through the inductance makes the effect of the inductance increase.

To reduce the associated ringing on the clock signals a resistor may be placed in series with the output of the clock driver to critically dampen the signal response. Many of the memory support circuits are available with this resistor in the output, such as the DS3649 which has a 15Ω dampening resistor, or the DS3679 which is functionally the same without a dampening resistor.

FALL-THROUGH LATCH

In many memory applications a holding register is required either for address or data I/O. Most commercially available registers have an objectionable propagation delay since the circuit's response is the sum of many gate delays. The address and data I/O paths are critical to the memory system access time and a faster register is preferred. The memory support circuits provide a selection of faster latches. These circuits are the DS3645/75 and the DS3647/77/147/177 series. These registers are faster since the latch function is in parallel instead of series with the signal path.

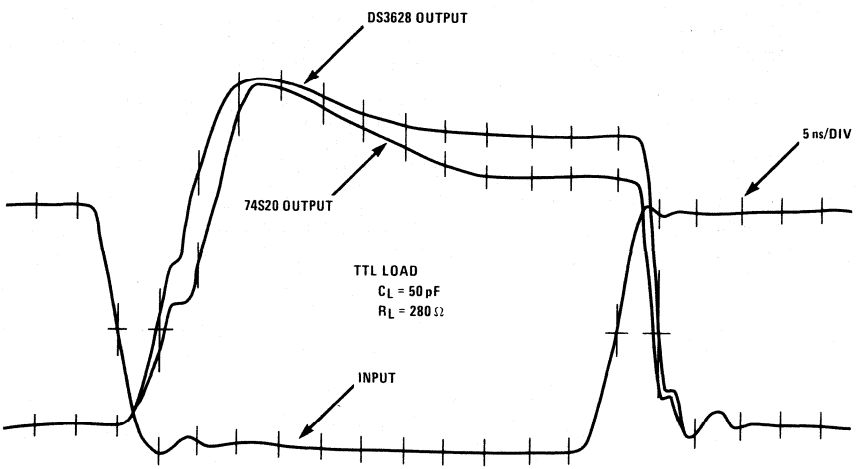


Figure 2. Switching Response with TTL Load

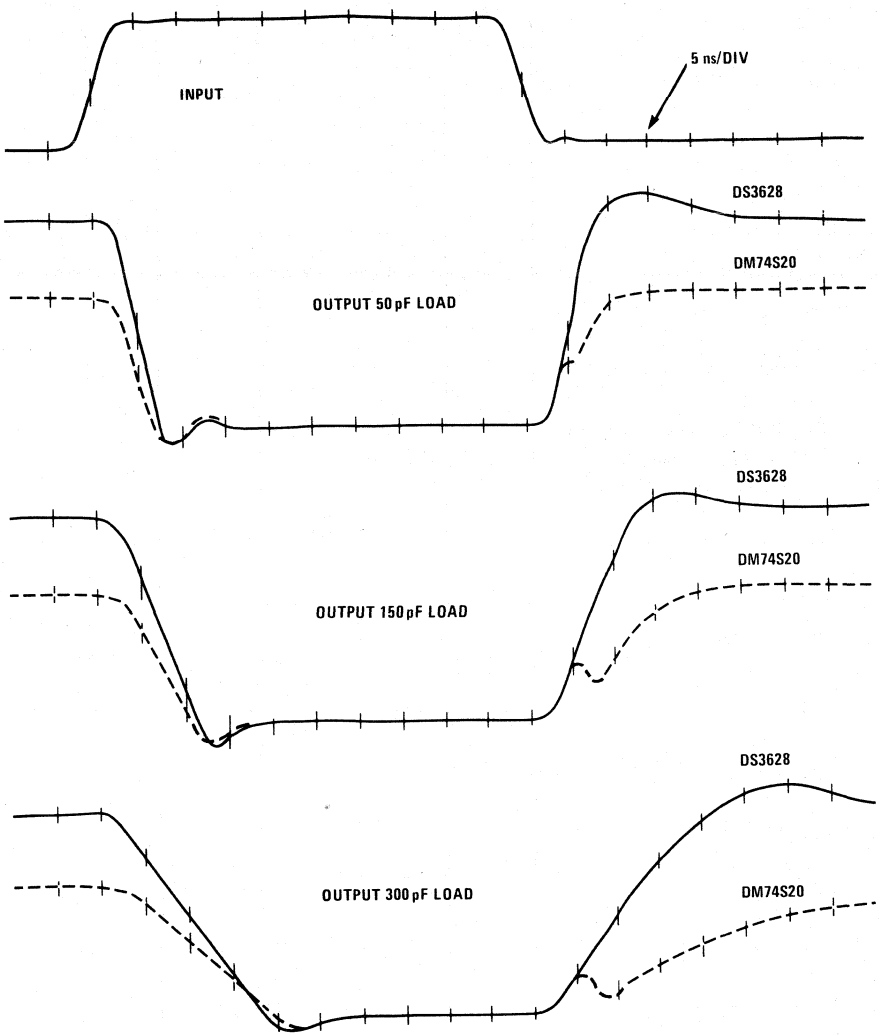


Figure 3. Switching Response with Capacitive Load

SELECTION GUIDE FOR 4k & 16k N-CHANNEL MOS MEMORY INTERFACE CIRCUITS

(Refer to 1978 Interface Databook for complete specifications)

Device Number and Name	5V Clock Drivers	12V Clock Drivers	4k RAM Address Drivers	16k RAM Address Drivers	Data I/O	Timing & Control Drivers
DS3628 Octal TRI-STATE® MOS Driver	•			•		•
DS3640, DS3670 Quad TRI-SHARE® Port Driver						•
DS3642, DS3672 Dual Bootstrapped MOS Clock Driver		•				
DS3643, DS3673 Quad Decoded MOS Clock Driver		•				
DS3644, DS3674 (3235, MC3460) Quad MOS Clock Driver		•				
DS3245 Quad MOS Clock Driver		•				
DS3645, DS3675 Hex TRI-STATE MOS Driver Latch			•			
DS3646, DS3676 6-Bit TRI-STATE MOS Refresh Counter/Driver			•			
DS3647, DS3677, DS36147, DS36177 Quad TRI-STATE MOS Memory I/O Register					•	
DS3648, DS3678 TRI-STATE MOS Multiplexer/Driver	•		•	•		•
DS3649, DS3679 Hex TRI-STATE MOS Driver	•		•			•
DS36149, DS36179 Hex MOS Driver	•		•			•
DS75322, DS3622 Dual TTL-to-MOS Driver		•				
DS75361 Dual TTL-to-MOS Driver		•				
DS75362 Dual TTL-to-MOS Driver		•				
DS75364 Dual TTL-to-MOS Driver		•				
DS75365 Quad TTL-to-MOS Driver		•				
DP8304B 8-Bit Bidirectional Transceiver					•	
DP8216, DP8226 4-Bit Bidirectional Transceiver					•	
DS8T26, DS8T28 Quad TRI-STATE Bus Driver					•	
DP8212 8-Bit Input/Output Port					•	
CD4024B 7-Stage Ripple-Carry Binary Counter/Divider				•		

DS1628/DS3628 Octal TRI-STATE® MOS Driver

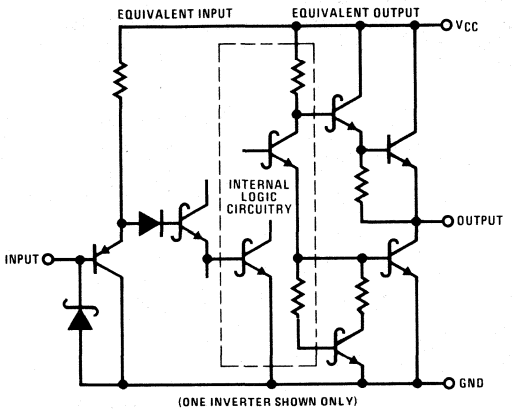
General Description

The DS1628/DS3628 are octal Schottky memory drivers with TRI-STATE® outputs designed to drive high capacitive loads associated with MOS memory systems. The drivers' output (V_{OH}) is specified at 3.4 V to provide additional noise immunity required by MOS inputs. A PNP input structure is employed to minimize input currents. The circuit employs Schottky-clamped transistors for high speed. A NOR gate of two inputs, DIS1 and DIS2, controls the TRI-STATE mode.

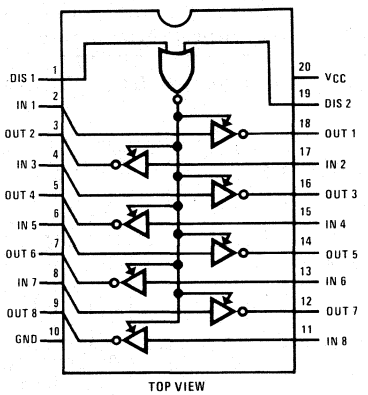
Features

- High speed capabilities
  - typ 5 ns driving 50 pF & 8 ns driving 500 pF
- TRI-STATE outputs
- High V_{OH} (3.4 V min)
- High density
  - eight drivers and two disable controls for TRI-STATE in a 20-pin package
- PNP inputs reduce DC loading on bus lines
- Glitch-free power up/down

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

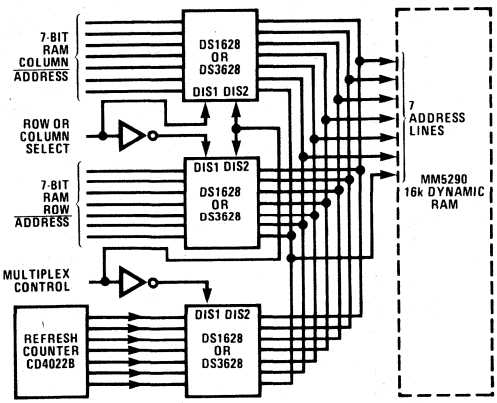
Order Number DS1628J or DS3628J
See NS Package J20B
Order Number DS3628N
See NS Package N20A

Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
H	H	X	Z
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = high level
L = low level
X = don't care
Z = high impedance (off)

Typical Application



National Semiconductor

DS1640/DS3640, DS1670/DS3670 Quad MOS TRI-SHARE™ Port Drivers

general description

The DS1640/DS3640 and DS1670/DS3670 are quad MOS TRI-SHARE port drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input current, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay.

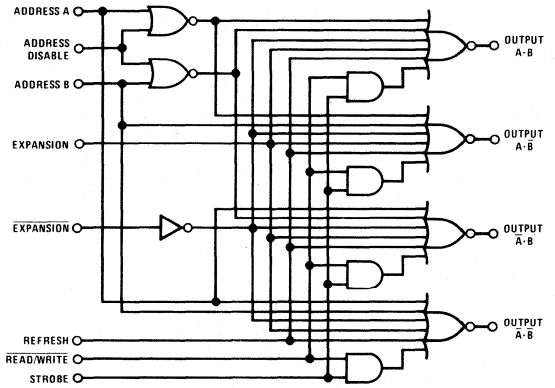
The DS1640/DS3640 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1670/DS3670 has a direct, low impedance output source for use with or without an external resistor.

The DS1640/DS1670 has two address inputs which decode to one-of-four-high outputs. Provisions are made for address expansion. For example, two packages may be used to implement a three-input, eight-output decoder. Also included is a refresh control, read/write, and strobe input. These functions are required by the MM5270 4k TRI-SHARE MOS RAM.

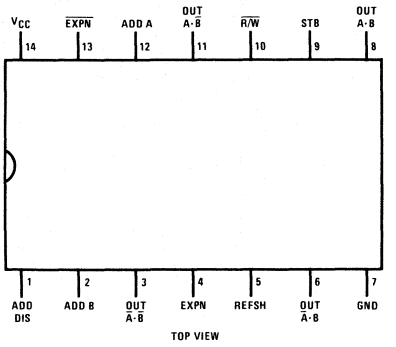
features

- TRI-SHARE port driver for MM5270 RAM
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- Built-in damping resistor (DS1640/DS3640)

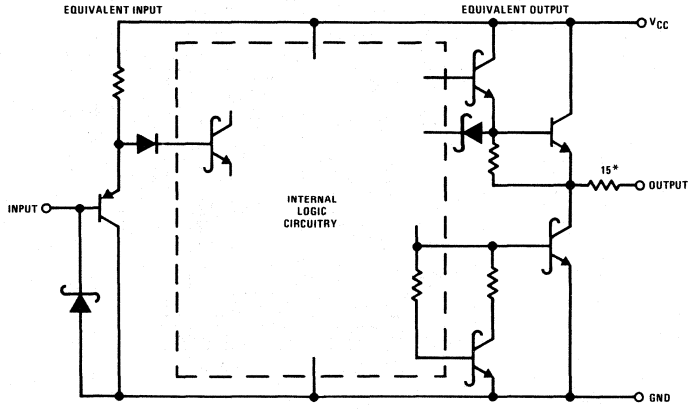
logic and connection diagrams



Dual-In-Line Package



schematic diagram



Order Number DS1640J, DS3640J, DS1670J or DS3670J
See NS Package J14A

Order Number DS3640N or DS3670N
See NS Package N14A

*DS1640/DS3640 only

DS1642/DS3642, DS1672/DS3672
Dual Bootstrapped MOS Clock Drivers

general description

The DS1672 is a dual bipolar-to-MOS clock driver designed to provide high output current and voltage capabilities necessary for driving high capacitance (up to 500 pF) MOS memory systems. The circuit needs only one power supply, (12V typical). This feature greatly reduces high stand-by power levels and at the same time simplifies system deisgn.

The circuit also features output bootstrapping, eliminating the need for an additional supply to provide a higher voltage to the output stage. The function is accomplished by connecting a small value capacitor (typically 200 pF) from the output to the bootstrap pin on each driver.

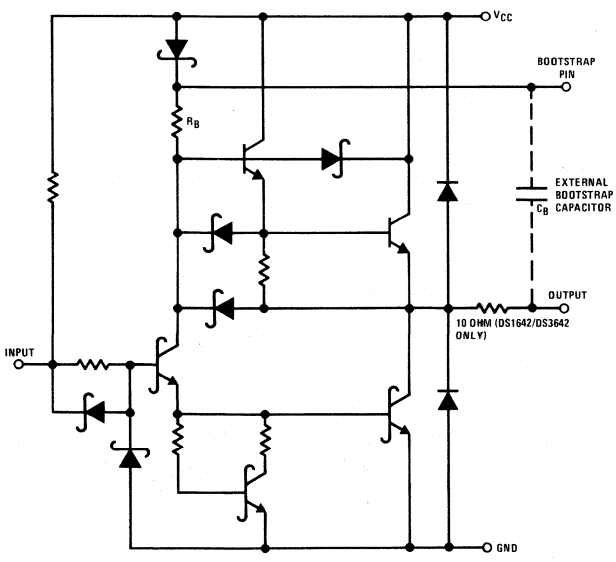
The circuit has Schottky-clamped transistor logic for minimum propagation delay. Typical stand-by power (output low) is 48 mW per driver. A fail-safe condition is provided in the circuit, so if the input is opened the output assumes the logic "0" state.

The DS1642/DS3642 has a 10 Ω resistor in series with each output to dampen transients caused by the fast-switching output. The DS1672/DS3672 has a direct low impedance output for use with or without an external resistor.

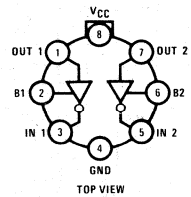
features

- High output voltage capability 13.2V
- TTL/DTL compatible inputs
- High speed operation
- Bootstrapping eliminates extra supplies—reduces power
- Low stand-by power 48 mW/driver
- Built-in 10 Ω damping resistor (DS1642/DS3642)

schematic and connection diagrams

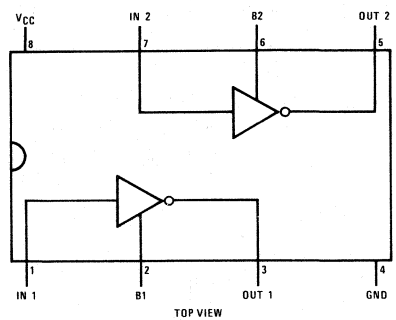


Metal Can Package



Order Number DS1642H, DS1672H, DS3642H or DS3672H
See NS Package H08C

Dual-In-Line Package



Order Number DS3642N or DS3672N
See NS Package N08B

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National Semiconductor

DS3643, DS3673 Decoded Quad MOS Clock Drivers

general description

The DS3643 and DS3673 are quad bipolar-to-MOS decoder/clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features full decoding of input address lines from two inputs to one of four outputs. Also featured is the capability of expanding to three inputs to one of eight outputs with the use of the Expansion and $\overline{\text{Expansion}}$ inputs. Also included are clock and refresh inputs.

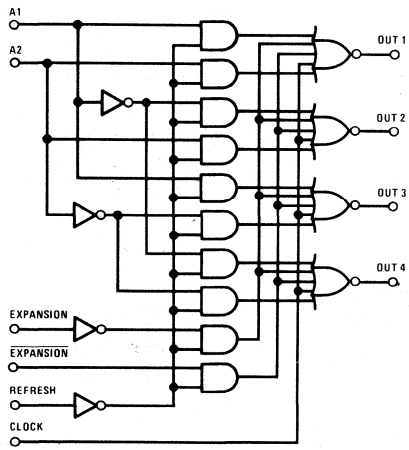
The circuit was designed for driving large capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

The DS3643 has a 10 Ω damping resistor in series with each output to dampen transients caused by the fast switching output, while the DS3673 has a direct, low impedance output, for use with or without an external resistor.

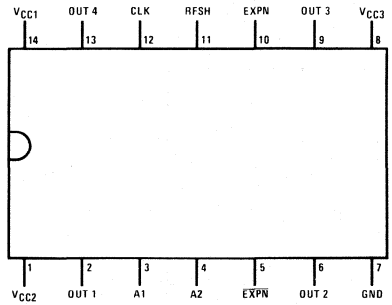
features

- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize input loading
- Full logic decoding for either two inputs to one of four outputs or three inputs to one of eight outputs
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Built-in damping resistors (DS3643)

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3643J or DS3673J
See NS Package J14A

Order Number DS3643N or DS3673N
See NS Package N14A

truth table

INPUTS						OUTPUTS			
CLOCK	REFRESH	EXPANSION	$\overline{\text{EXPANSION}}$	A_2	A_1	OUT 1	OUT 2	OUT 3	OUT 4
1	X	X	X	X	X	0	0	0	0
0	1	X	X	X	X	1	1	1	1
0	0	1	0	0	0	1	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0	1	0
0	0	1	0	1	1	0	0	0	1
0	0	1	1	X	X	0	0	0	0
0	0	0	1	X	X	0	0	0	0
0	0	0	0	X	X	0	0	0	0

X = don't care state

National Semiconductor

DS1644/DS3644, DS1674/DS3674 Quad TTL-MOS Clock Drivers

general description

The DS1644/DS3644 and DS1674/DS3674 are quad bipolar-to-MOS clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs thereby minimizing input loading.

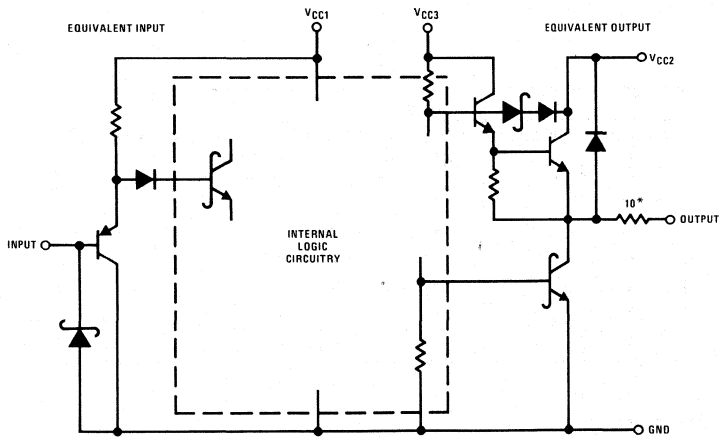
The circuit may be connected to provide a 12V clock output amplitude as required by 4k RAMs or a 5V clock output amplitude as required by 16k RAMs.

The DS1644/DS3644 contains a 10Ω resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS1674/DS3674 has a direct, low impedance output for use with or without an external damping resistor.

features

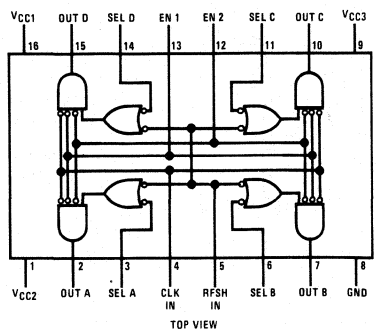
- TTL/DTL compatible inputs
- 12V clock or 5V clock driver
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS1644/DS3644)

schematic and connection diagrams



* DS1644/DS3644 only

Dual-In-Line Package



Order Number DS3644J or DS3674J
See NS Package J16A

Order Number DS3644N or DS3674N
See NS Package N16A

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National Semiconductor

DS36144, DS36174 Quad TTL-MOS Clock Drivers

general description

The DS36144 and DS36174 are quad bipolar-to-MOS clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs thereby minimizing input loading.

The DS36144 contains a 10 Ω resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS36174 has a direct, low impedance output for use with or without an external damping resistor.

features

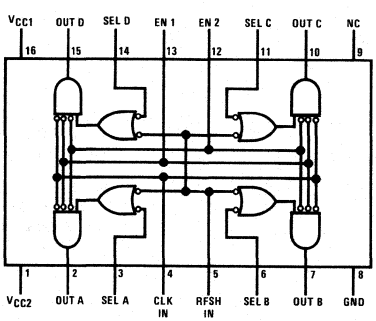
- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- Two supply operation (5V and 12V)
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with DS3644, DS3674, MC3460 andMC3235
- Built-in damping resistors (DS36144)

truth table

INPUT					OUTPUT
ENABLE 1	ENABLE 2	SELECT INPUT	CLOCK INPUT	REFRESH INPUT	
1	X	X	X	X	0
X	1	X	X	X	0
X	X	X	1	X	0
X	X	1	X	1	0
0	0	0	0	X	1
0	0	X	0	0	1

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DS36144J or DS36174J
See NS Package J16A

Order Number DS36144N or DS36174N
See NS Package N16A

DS1645/DS3645, DS1675/DS3675
Hex TRI-STATE® TTL-MOS Latches/Drivers

general description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latches/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs which allow bus operation.

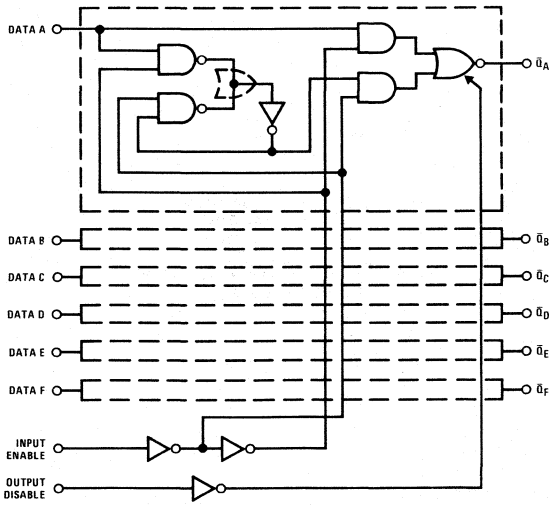
The DS1645/DS3645 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

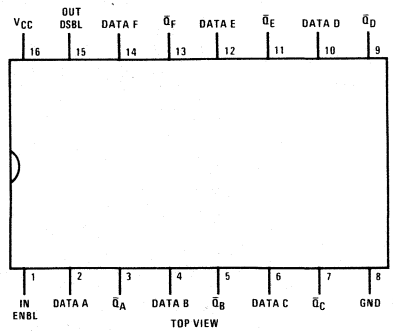
features

- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

logic and connection diagrams



Dual-In-Line Package



Order Number DS1645J, DS1675J, DS3645J or DS3675J
See NS Package J16A

Order Number DS3645N or DS3675N
See NS Package N16A

truth table

INPUT ENABLE	OUTPUT DISABLE	DATA	OUTPUT	OPERATION
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = Don't care
Hi-Z = TRI-STATE mode

National Semiconductor

DS1646/DS3646, DS1676/DS3676 6-Bit TRI-STATE® TTL-MOS Refresh Counters/Drivers

General Description

The DS1646/DS3646 and DS1676/DS3676 are 6-bit refresh counters with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI STATE® outputs allow it to be used on common data buses.

The DS1646/DS3646 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1676/DS3676 has a direct, low impedance output, for use with or without an external resistor.

The counter uses as its input the RAM clock signal, and with each clock input, it advances the count by one, generating a new refresh address. It also contains an initialize input to preset counter outputs to logic "0".

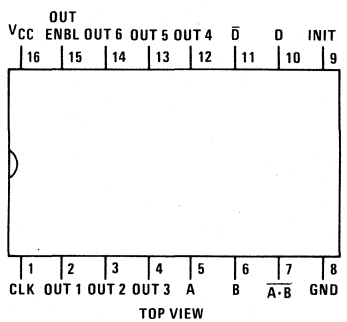
Uncommitted pins in the package are used for a 2-input NAND gate and an inverter gate, both of which have capacitive drive outputs.

Features

- 4k RAM dynamic refresh counter
- TRI-STATE outputs
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driver outputs (500 pF)
- Built-in damping resistor (DS1646, DS3676)
- Extra gates provided
- Initialize input clears counters
- Positive edge clock

Connection Diagram

Dual-In-Line Package

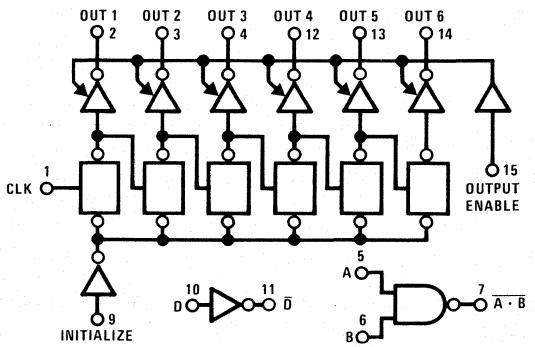


TOP VIEW

Order Number DS1646J, DS1676J, DS3646J or DS3676J
See NS Package J16A

Order Number DS3646N or DS3676N
See NS Package N16A

Block Diagram



National Semiconductor

DS1647/DS3647, DS1677/DS3677, DS16147/DS36147, DS16177/DS36177 Quad TRI-STATE® MOS Memory I/O Registers

general description

The DS1647/DS3647 series are 4-bit I/O buffer registers intended for use in MOS memory systems. The circuits employ a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. The circuits use Schottky-clamped transistor logic for minimum propagation delay and employ PNP input transistors so that input currents are low, allowing large fan-out to these circuits needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

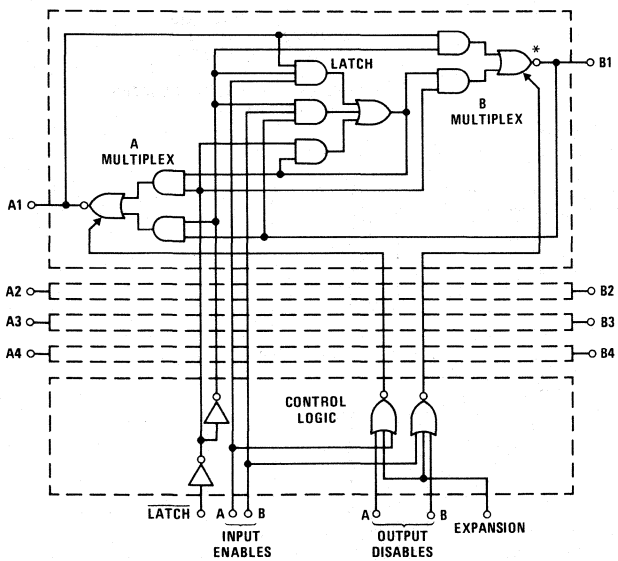
The "B" port outputs in the DS16147/DS36147 and DS16177/DS36177 are open collectors, and in the DS1647/DS3647 and DS1677/DS3677 they are TRI-STATE. The "B" port outputs are also designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA. The "A" port outputs in all four types are TRI-STATE.

Data going from port "A" to port "B" is inverted in the DS1647/DS3647 and DS16147/DS36147 and is not inverted in the DS1677/DS3677 and DS16177/DS36177. Data going from port "B" to port "A" is inverted in all four types.

features

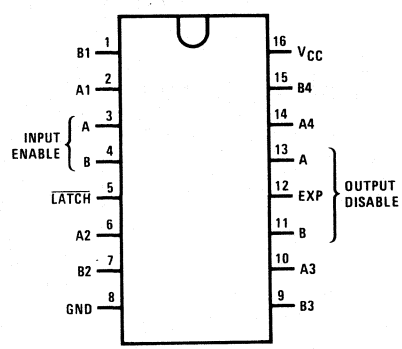
- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL/DTL compatible
- Transmission line driver output

logic and connection diagrams



*Inverting DS1647/DS3647 and DS16147/DS36147 only

Dual-In-Line Package



TOP VIEW

Order Number DS1647J, DS3647J, DS1677J, DS3677J, DS16147J, DS36147J, DS16177J or DS36177J
See NS Package J16A

Order Number DS3647N, DS3677N, DS36147N or DS36177N
See NS Package N16A

12

National Semiconductor

DS1648/DS3648, DS1678/DS3678 TRI-STATE® MOS Multiplexers/Drivers

general description

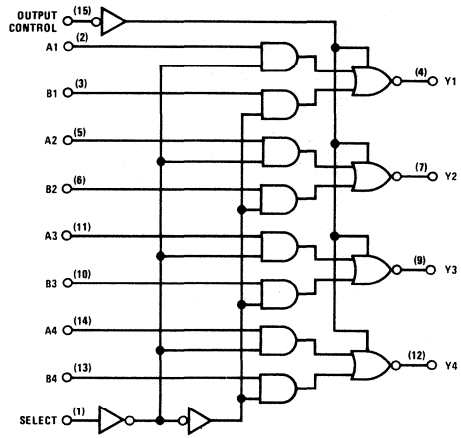
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

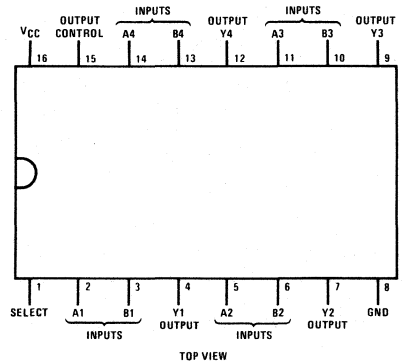
features

- TRI-STATE outputs interface directly with system bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- DTL and TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

logic and connection diagrams



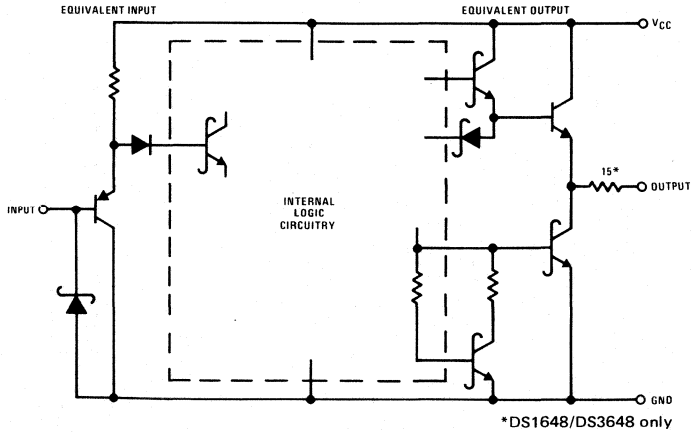
Dual-In-Line Package



Order Number DS1648J, DS3648J, DS1678J or DS3678J
See NS Package J16A

Order Number DS3648N or DS3678N
See NS Package N16A

schematic diagram



*DS1648/DS3648 only

National Semiconductor

DS1649/DS3649, DS1679/DS3679 Hex TRI-STATE® TTL-MOS Drivers

general description

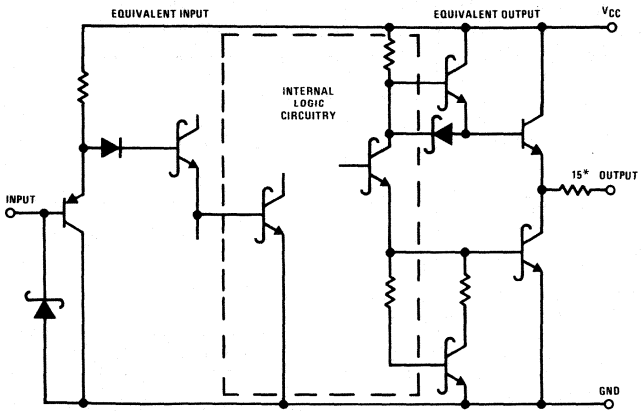
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

schematic diagram



*DS1649/DS3649 only

truth table

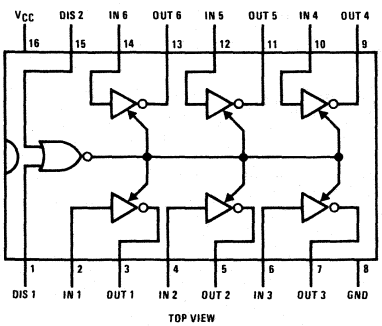
DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

X = Don't care

Hi-Z = TRI-STATE mode

connection diagram

Dual-In-Line Package

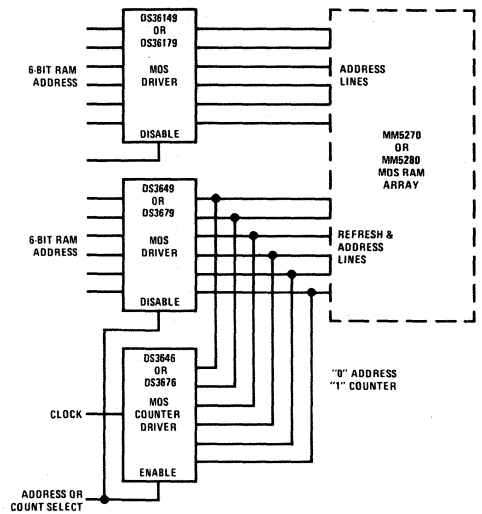


TOP VIEW

Order Number DS1649J, DS3649J, DS1679J or DS3679J
See NS Package J16A

Order Number DS1649N, DS3649N, DS1679N or DS3679N
See NS Package N16A

typical application



12

National Semiconductor

DS16149/DS36149, DS16179/DS36179 Hex MOS Drivers

general description

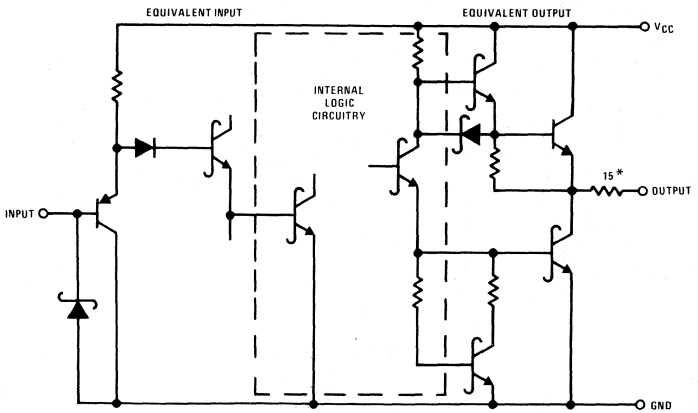
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

schematic diagram



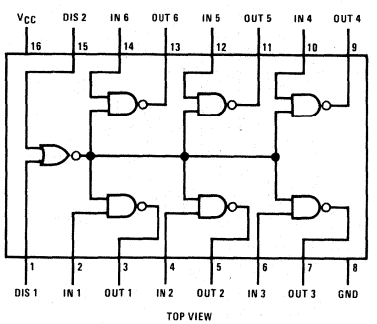
*DS16149/DS36149 only.

Order Number DS16149J, DS36149J, DS16179J or DS36179J
See NS Package J16A

Order Number DS36149N or DS36179N
See NS Package N16A

connection diagram

Dual-In-Line Package



TOP VIEW

truth table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

DS75322 Dual TTL-MOS Driver
DS3622 Dual Fail-Safe TTL-MOS Driver

General Description

The DS75322 is a dual TTL-MOS high speed driver. The input structure of the device is TTL and DTL compatible. A common strobe input is provided for gating the outputs to the low state. The outputs provide high current and high voltage levels ideal for driving MOS circuits. The DS75322 specifically meets the requirements for driving N-channel RAMs where low power dissipation is desirable when the driver is in the low state.

The DS3622 provides output fail-safe protection. Powering down V_{CC1} activates the fail-safe circuit, forcing the outputs to the low state. The fail-safe feature eliminates output glitches that may occur in systems that power down V_{CC1}. Functionally, the DS3622 and the DS75322 are identical.

The DS75322, DS3622 require 2 external PNP transistors per package.

The DS75322, DS3622 are characterized for operation from 0°C to +70°C.

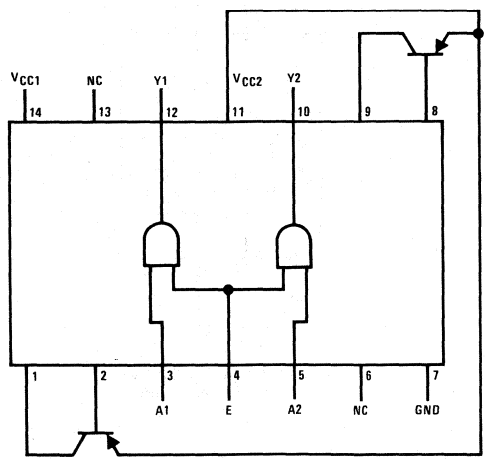
The DS75322 and the DS3622 are ideal for driving the UPD411D, MM5280 and the MM5270 4k RAMs.

Features

- Dual positive-logic and TTL-MOS driver
- TTL and DTL compatible inputs
- High voltage/current outputs
- Operates from standard bipolar and MOS supplies
- High speed switching
- Input and output clamping diodes
- Separate driver address inputs with common strobe
- V_{OH} and V_{OL} compatible with 4k RAMs and other popular MOS RAMs
- No current (leakage only) when outputs are in low state (DS75322)
- Outputs forced to low state with loss of V_{CC1} (DS3622)

Connection Diagram

Dual-In-Line Package



Positive Logic Y = AE
Recommended PNP Transistors
2N5910, 2N5771

TOP VIEW

Order Number DS75322J or DS3622J
See NS Package J14A

Order Number DS75322N or DS3622N
See NS Package N14A

National Semiconductor

DS75361 Dual TTL-MOS Driver

general description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280

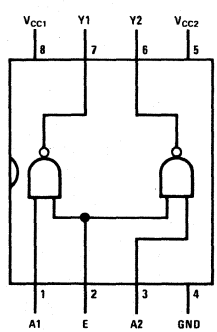
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL and DTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DS75361N-8
See NS Package N08B

DS75362 Dual TTL-MOS Driver

general description

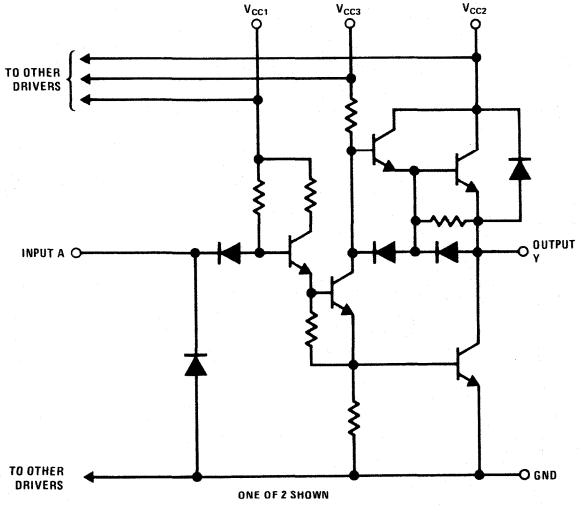
The DS75362 is a dual monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75362 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

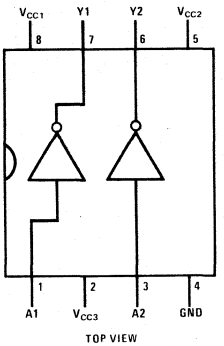
features

- Dual positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

schematic and connection diagrams



Dual-In-Line Package



Order Number DS75362N-8
See NS Package N08B

12

National Semiconductor

DS75364 Dual MOS Clock Driver

general description

The DS75364 is a dual MOS driver and interface circuit that operates with either current source or voltage source input signals. The device accepts signals from TTL levels or other logic systems and provides high current and high voltage output levels suitable for driving MOS circuits. It may be used to drive address, control and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The DS75364 operates from standard MOS and bipolar supplies, and has been optimized for operation with V_{CC1} supply voltage from 12–20V positive with respect to V_{EE}, and with nominal V_{CC2} supply voltage from 3–4V more positive than V_{CC1}. However, it is designed so as to be useable over a much wider range of V_{CC1} and V_{CC2}. In some applications the V_{CC2} power supply can be eliminated by connecting the V_{CC2} pin to the V_{CC1} pin.

Inputs of the DS75364 are referenced to the V_{EE} terminal and contain a series current limiting resistor. The device will operate with either positive input current signals or input voltage signals which are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12V to −15V with the inputs to be driven from TTL levels or other positive voltage levels. The required negative level shifting may be done with an external PNP transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

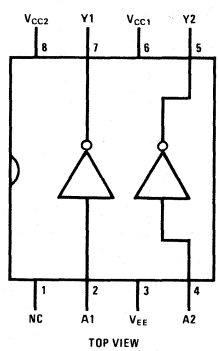
The DS75364 is characterized for operation over the 0°C to +70°C temperature range.

features

- Versatile interface circuit for use between TTL levels and level shifted high current, high voltage systems
- Inputs may be level shifted by use of a current source or capacitive coupling or driven directly by a voltage source
- Capable of driving high capacitance loads
- Compatible with many popular MOS RAMs and MOS shift registers
- V_{CC1} supply voltage variable over wide range to 22V maximum with respect to V_{EE}
- V_{CC2} pull-up supply voltage pin available
- Operates from standard bipolar and/or MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DS75364N-8
See NS Package N08B

DS75365 Quad TTL-MOS Driver

general description

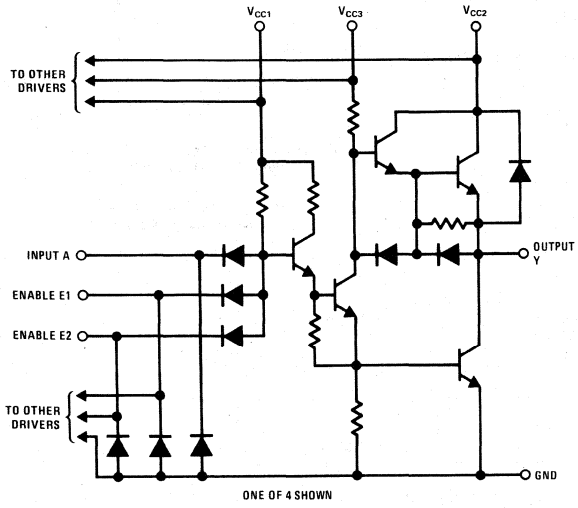
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

features

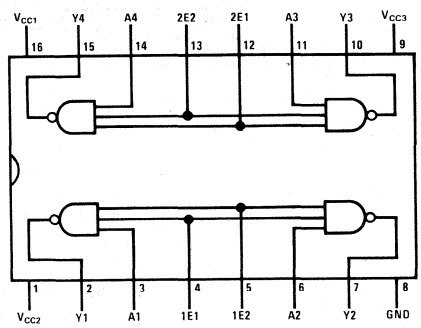
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

schematic and connection diagrams



ONE OF 4 SHOWN

Dual-In-Line Package



TOP VIEW

Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

Order Number DS75365J
See NS Package J16A

Order Number DS75365N
See NS Package N16A

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National Semiconductor

DP7304B/DP8304B 8-Bit TRI-STATE® Bidirectional Transceiver

General Description

The DP7304B/DP8304B are 8-bit TRI-STATE® Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16 mA drive capability on the A ports and 48 mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

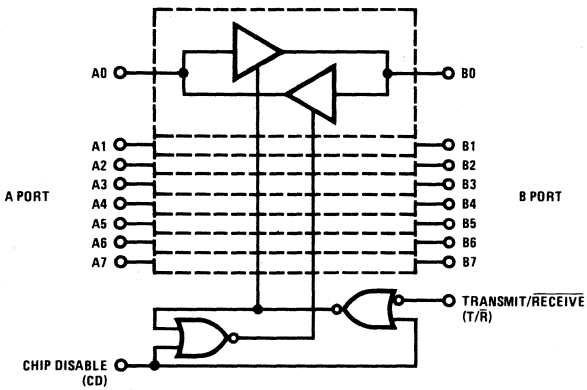
Transmit/$\overline{\text{Receive}}$ inputs determine the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a TRI-STATE condition.

The output high voltage (V_{OH}) is specified at V_{CC} − 1.15 V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

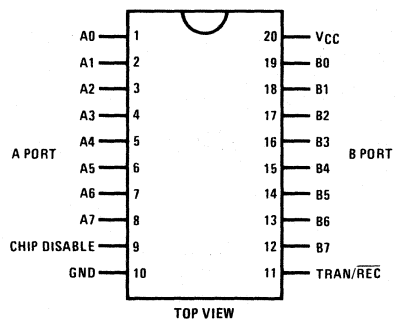
Features

- 8-Bit Bidirectional Data Flow Reduced System Package Count
- Bidirectional TRI-STATE Inputs/Outputs Interface with Bus-Oriented Systems
- PNP Inputs Reduce Input Loading
- Output High Voltage Interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF Bus Drive Capability
- Pinouts Simplify System Interconnections
- Transmit/$\overline{\text{Receive}}$ and Chip Disable Simplify Control Logic
- Compact 20-Pin Dual-In-Line Package
- Low I_{CC} Power (8 mA per bidirectional bit)
- Bus Port Glitch Free Power Up/Down

Logic and Connection Diagrams



Dual-In-Line Package



Order Number DP7304J or DP8304J
See NS Package J20B

Order Number DP8304N
See NS Package N20A

Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

DP8216, DP8216M, DP8226, DP8226M
4-Bit Bidirectional Bus Transceivers

General Description

The DP8216/DP8216M and DP8226/DP8226M are 4-bit bidirectional bus drivers for use in bus oriented applications. The non-inverting DP8216/DP8216M and inverting DP8226/DP8226M drivers are provided for flexibility in system design.

Each buffered line of the four-bit driver consists of two separate buffers that are TRI-STATE® to achieve direct bus interface and bidirectional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB); this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50 mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bidirectional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The CS input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "low" the device is enabled and the direction of the data flow is determined by the DIEN input.

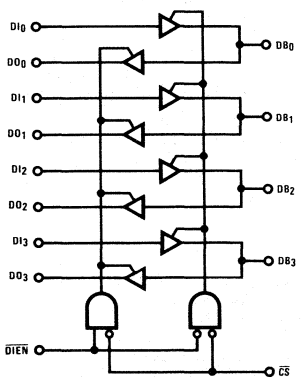
The DIEN input controls the direction of data flow, which is accomplished by forcing one of the pair of buffers into its high-impedance state and allowing the other to transmit its data. A simple two-gate circuit is used for this function.

Features

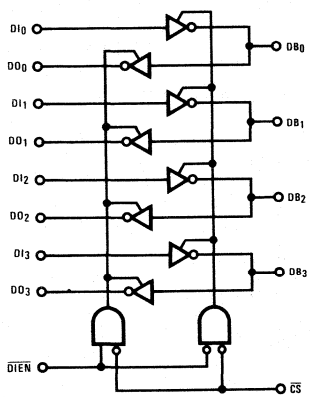
- Data bus buffer driver for 8080 type CPUs
- Low input load current – 0.25 mA maximum
- High output drive capability for driving system data bus – 50 mA at 0.5 V
- Power up-down protection
- DP8216/DP8216M have non-inverting outputs
- DP8226/DP8226M have inverting outputs
- Output high voltage compatible with direct interface to MOS
- TRI-STATE outputs
- Advanced Schottky processing
- Available in military and commercial temperature ranges

Logic and Connection Diagrams

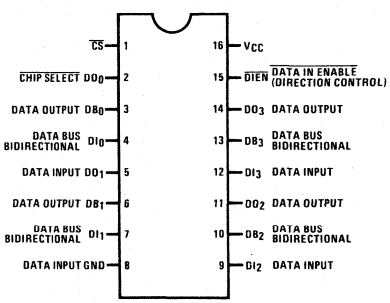
DP8216/DP8216M



DP8226/PD8226M



Dual-In-Line Package



Order Number DP8216J, DP8226J, DP8216MJ or DP8226MJ
See NS Package J16A

12

National Semiconductor

DS8T26A, DS8T26AM, DS8T28, DS8T28M
4-Bit Bidirectional Bus Transceivers

General Description

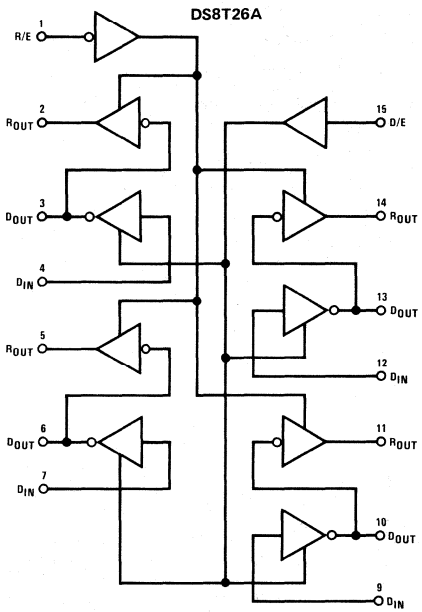
The DS8T26A, DS8T28 consists of 4 pairs of TRI-STATE® logic elements configured as quad bus drivers/receivers along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the DS8T26A, DS8T28 from conventional multi-IC implementations. In addition, the DS8T26A, DS8T28's ultra high speed while driving heavy bus capacitance (300 pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

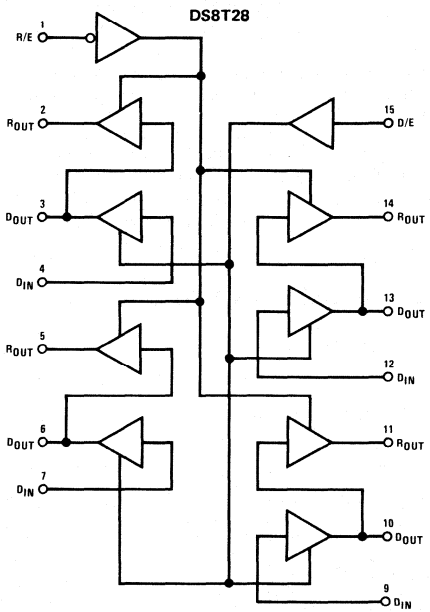
Both the driver and receiver gates have TRI-STATE outputs and low current PNP inputs. PNP inputs reduce input loading to 200 μA maximum.

Features

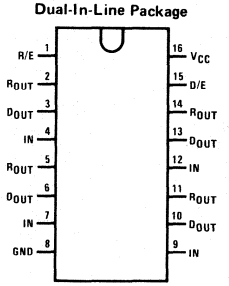
- Inverting outputs in the DS8T26A
- Non-inverting outputs in the DS8T28
- TRI-STATE outputs
- Low current PNP inputs
- Fast switching times (20 ns)
- Advanced Schottky processing
- Driver glitch free power up/down
- Non-overlapping TRI-STATE

Logic and Connection Diagrams





Dual-In-Line Package



TOP VIEW

Order Number DS8T26AJ, DS8T26AMJ, DS8T28J or DS8T28MJ
See NS Package J16A

Order Number DS8T26AN, DS8T26AMN, DS8T28N or DS8T28MN
See NS Package N16A

DP8212, DP8212M 8-Bit Input/Output Port

general description

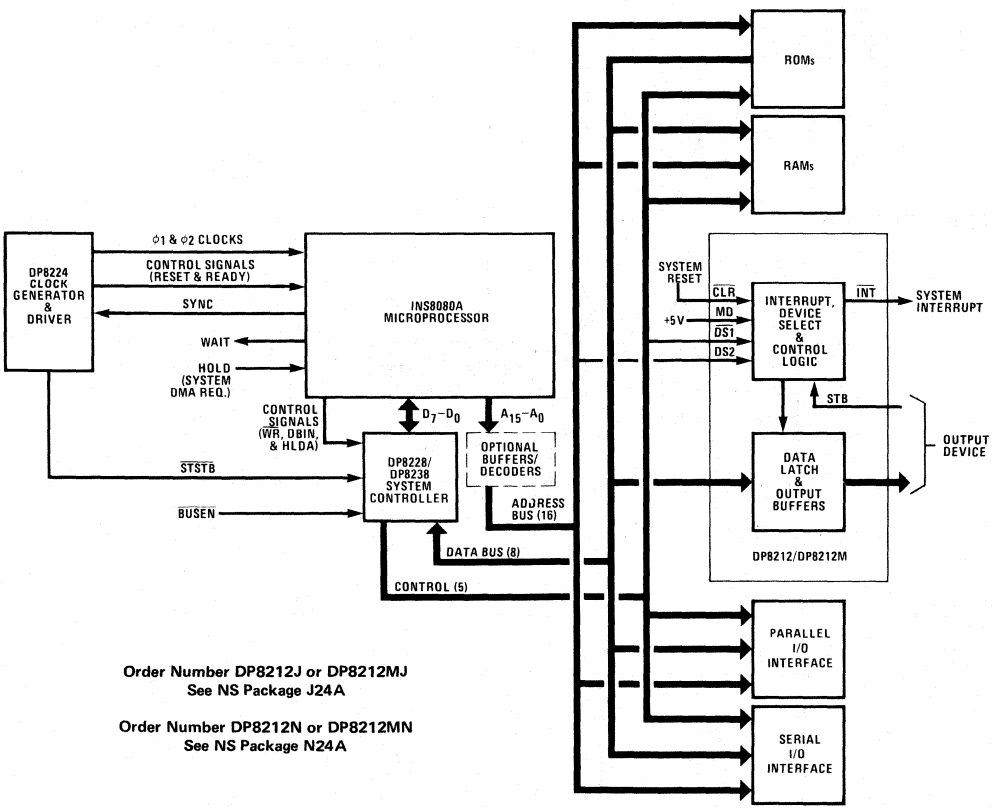
The DP8212/DP8212M is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's N8080 microcomputer family. The DP8212/DP8212M can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The DP8212/DP8212M includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

features

- 8-Bit Data Latch and Buffer
- Service Request Flip-flop for Generation and Control of Interrupts
- 0.25mA Input Load Current
- TRI-STATE TTL Output Drive Capability
- Outputs Sink 15mA
- Asynchronous Latch Clear
- 3.65V Output for Direct Interface to INS8080A
- Reduces System Package Count by Replacing Buffers, Latches, and Multiplexers in Microcomputer Systems

N8080A microcomputer family block diagram



Order Number DP8212J or DP8212MJ
See NS Package J24A

Order Number DP8212N or DP8212MN
See NS Package N24A

National Semiconductor

CD4024BM, CD4024BC 7-Stage Ripple Carry Binary Counter

general description

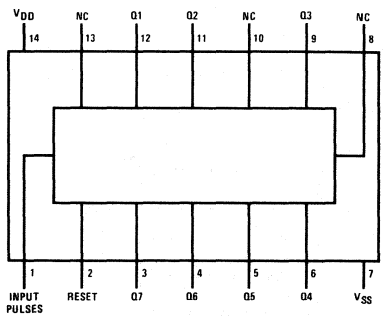
The CD4024BM/CD4024BC is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The counter is reset to its logical "0" state by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ High speed	12 MHz (typ) input pulse rate $V_{DD} - V_{SS} = 10V$
■ Fully static operation	

connection diagram

Dual-In-Line Package

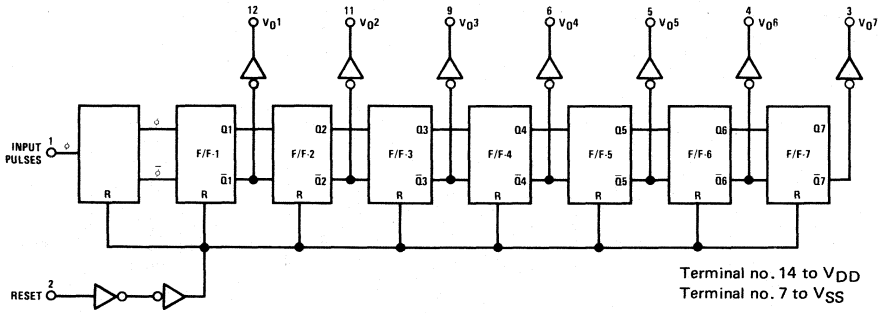


TOP VIEW

Order Number CD4024DMJ or CD4024BCJ
See NS Package J14A

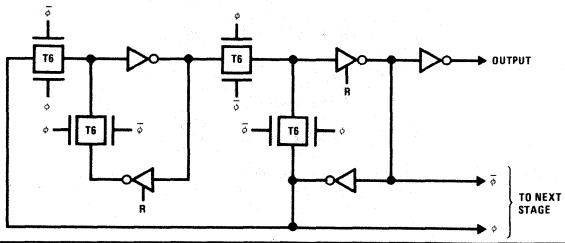
Order Number CD4024DMN or CD4024BCN
See NS Package N14A

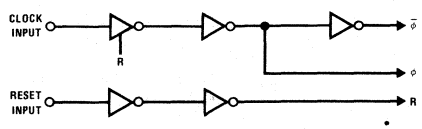
logic diagram



Terminal no. 14 to V_{DD}
Terminal no. 7 to V_{SS}

schematic diagram





Input Logic

Flip-flop logic (1 of 7 identical stages).

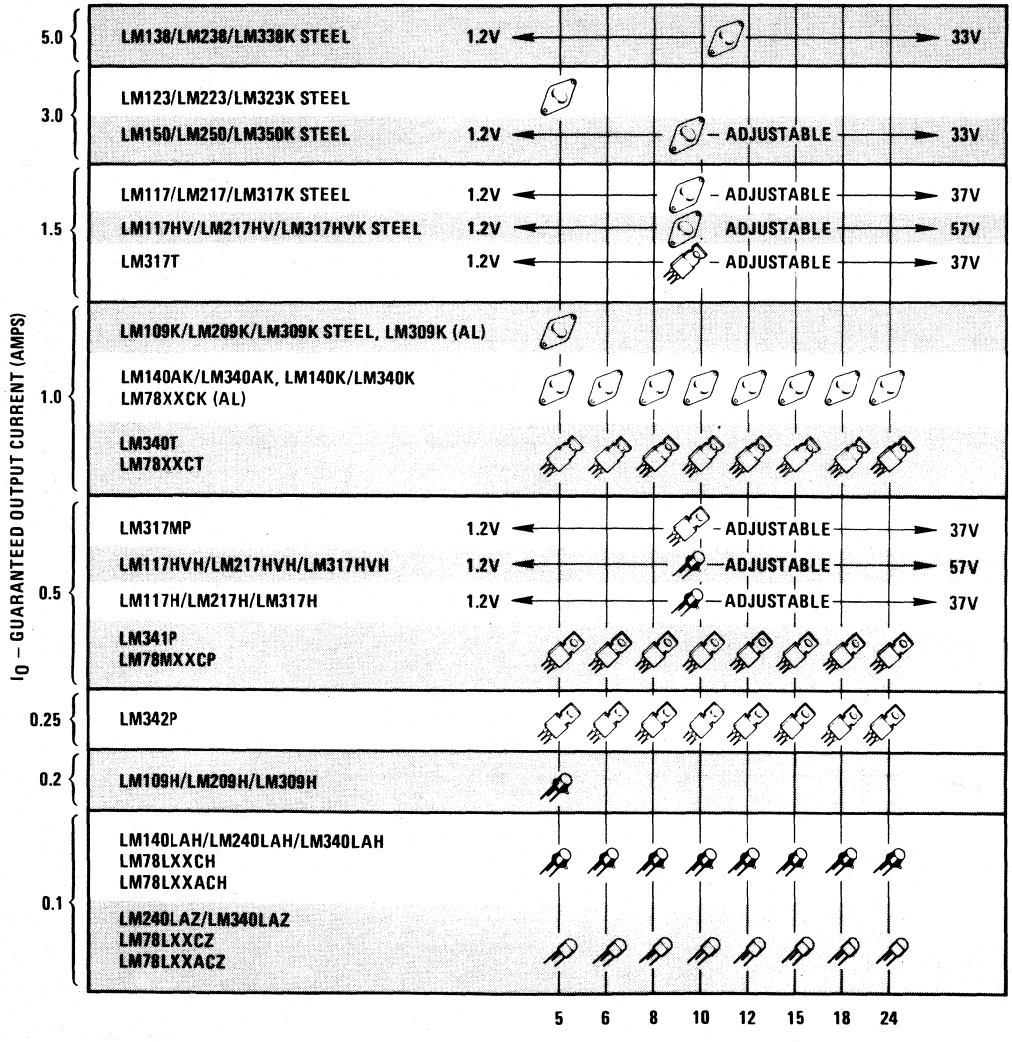
3-TERMINAL POSITIVE

Output Current (A)	Device	Available V_{OUT} (V)	V_{OUT} Tol. (±%)	Regulation		V_{IN} (V) Max	Ripple Rejection (dB)
				Line (Note 1) % V_{OUT}/V_{IN}	Load (Note 2) % V_{OUT}		
5	LM138, LM238	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM338	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
3	LM150, LM250	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM350	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM123K, LM223K	5	6	0.01	0.5	20	75
	LM323K	5	4	0.01	0.5	20	75
1.5	LM117, LM217	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM117HV, LM217HV	1.2 to 57 (Adjustable)	N/A	0.01	0.1	60	80
	LM317HV	1.2 to 57 (Adjustable)	N/A	0.01	0.1	60	80
	LM109K, LM209K	5	6	0.004	1.0	35	80
	LM309K	5	4	0.004	1.0	35	80
	LM140K	5, 6, 8, 10, 12, 15, 18, 24	4	0.02	0.5	35, 40 (24V)	66–80
	LM140AK	5, 6, 8, 10, 12, 15, 18, 24	2	0.002	0.1	35, 40 (24V)	66–80
	LM340	5, 6, 8, 10, 12, 15, 18, 24	4	0.02	0.5	35, 40 (24V)	66–80
	LM340A	5, 6, 8, 10, 12, 15, 18, 24	2	0.002	0.1	35, 40 (24V)	66–80
	LM78XXC	5, 6, 8, 10, 12, 15, 18, 24	4	0.03	0.5	35, 40 (24V)	66–80
0.5	LM117H, LM217H	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317H	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM117HVH, LM217HVH	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317HVH	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317M	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM341	5, 6, 8, 10, 12, 15, 18, 24	4	0.02	0.5	35, 40 (24V)	
	LM78MXX	5, 6, 8, 10, 12, 15, 18, 24	4	0.03	0.5	35, 40 (24V)	
0.25	LM342	5, 6, 8, 10, 12, 15, 18, 24	4	0.03	0.5	35, 40 (24V)	53–64
0.20	LM109H, LM209H	5	6	0.004	0.4	35	80
	LM309H	5	4	0.004	0.4	35	80
0.10	LM140L, LM240L	5, 6, 8, 10, 12, 15, 18, 24	2	0.02	0.25	35, 40 (24V)	48–62
	LM340L	5, 6, 8, 10, 12, 15, 18, 24	2	0.02	0.25	35, 40 (24V)	48–62
	LM78LXXA	5, 6, 8, 10, 12, 15, 18, 24	4	0.03	0.25	35, 40 (24V)	45–60

Note 1: Line regulation is the change in output voltage for a change in input voltage.

Note 2: Load regulation is the change in output voltage due to a change in load current from no load to full load.

3-TERMINAL POSITIVE



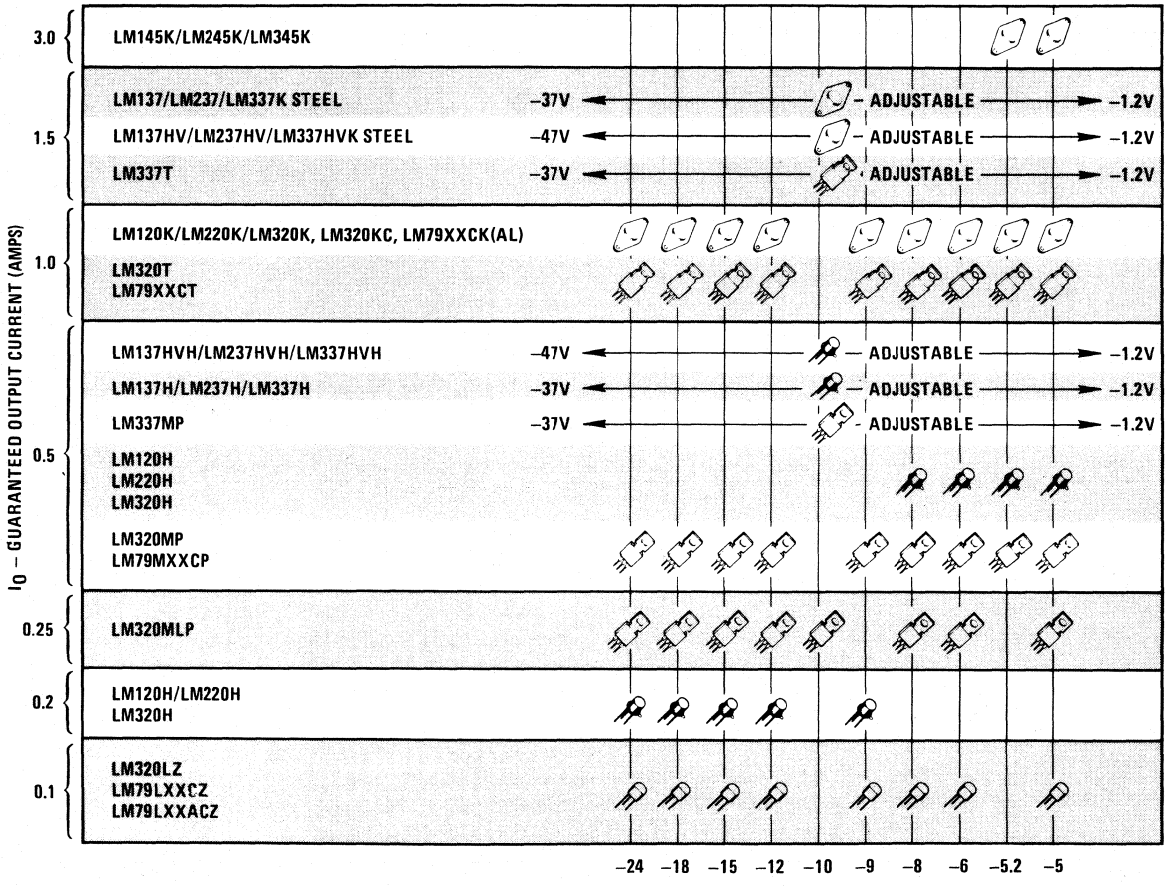
	PACKAGE DESIGNATOR	PACKAGE TYPE
	K KC K STEEL	TO-3* HERMETIC
	T	TO-220 PLASTIC
	P	TO-202 PLASTIC
	H	TO-5, TO-39 HERMETIC
	Z	TO-99 PLASTIC

*All devices with TO-3 package designators (K or K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (AL) aluminum TO-3 package. All KC designated devices are supplied in aluminum TO-3.

3-TERMINAL NEGATIVE

Output Current (A)	Device	Available V_{OUT} (V)	V_{OUT} Tol. (±%)	Regulation		V_{IN} (V) Max	Ripple Rejection (dB)
				Line (Note 1) % V_{OUT}/V_{IN}	Load (Note 2) % V_{OUT}		
3	LM145K, LM245K	−5.0, −5.2	2	0.008	0.6	20	68
	LM345K	−5.0, −5.2	4	0.008	0.6	20	68
1.5	LM137, LM237	−1.2 to −37 (Adjustable)	N/A	0.006	0.3	40	77
	LM337	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM137HV, LM237HV	−1.2 to −47 (Adjustable)	N/A	0.006	0.3	50	77
	LM337HV	−1.2 to −47 (Adjustable)	N/A	0.007	0.3	50	77
	LM120K, LM220K	−5, −5.2, −6, −8, −9	2	0.02	0.3	25	64
		−12, −15, −18, −24				35 (9V, 12V)	80
						40 (15V, 18V)	75
						42 (24V)	70
	LM320K	−5, −5.2, −6, −8, −9,	4	0.02	0.3	25	64
		−12, −15, −18, −24				35 (9V, 12V)	80
						40 (15V, 18V)	75
						42 (24V)	70
	LM320T	−5, −5.2, −6, −8, −9	4	0.02	0.3	25	64
		−12, −15, −18, −24				35 (9V, 12V, 15V, 18V)	75–80
						40 (24V)	70
	LM79XXC	−5, −5.2, −6, −8, −9	4	0.03	0.4	35, 40 (24V)	66–70
		−12, −15, −18, −24					
0.5	LM137H, LM237H	−1.2 to −37 (Adjustable)	N/A	0.006	0.3	40	77
	LM337H	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM137HVH, LM237HVH	−1.2 to −47 (Adjustable)	N/A	0.006	0.3	50	77
	LM337HVH	−1.2 to −47 (Adjustable)	N/A	0.007	0.3	50	77
	LM337M	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM120H, LM220H	−5.0, −5.2, −6, −8	2	0.02	0.6	25	64
	LM320H	−5.0, −5.2, −6, −8	4	0.02	0.6	25	64
	LM320M	−5, −5.2, −6, −8	4	0.02	0.6	25	60–64
		−9, −12, −15, −18, −24	4			35, (9V, 12V, 15V, 18V)	70–80
						40 (24V)	
	LM79MXX	−5, −6, −8, −12, −15, −24	4	0.03	0.7	35, 40 (24V)	58–60
0.25	LM320ML	−5, −6, −8, −10,	4	0.01	0.5	35, 40 (24V)	50–60
		−12, −15, −18, −24					
0.20	LM120H, LM220H	−9, −12	2	0.02	0.1	35 (9V, 12V)	70–80
	LM320H	−15, −18, −24	4	0.02	0.1	40 (15V, 18V)	
						42 (24V)	
0.10	LM320L	−5, −6, −8, −9	4	0.01	0.5	35, 40 (24V)	60–65
		−12, −15, −18, −24					
	LM79LXXA	−5, −12, −15, −18, −24	4	0.02	0.6	35, 40 (24V)	50–55

3-TERMINAL NEGATIVE



	PACKAGE DESIGNATOR	PACKAGE TYPE
	K KC K-STEEL	TO-3* HERMETIC
	T	TO-220 PLASTIC
	P	TO-202 PLASTIC
	H	TO-5, TO-39 HERMETIC
	Z	TO-99 PLASTIC

*All devices with TO-3 package designators (K or K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (AL) aluminum TO-3 package. All KC designated devices are supplied in aluminum TO-3.

Section 13

Physical Dimensions

13

PACKAGES

DUAL-IN-LINE PACKAGES

(N) Devices ordered with "N" suffix are supplied in molded dual-in-line package. Molding material is EPOXY B2, a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is Alloy 42 with a hot solder dipped surface to allow for ease of solderability.

(J) Devices ordered with the "J" suffix are supplied in either the 14-pin, 16-pin, or 24-pin ceramic dual-in-line package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

(D) Devices ordered with the "D" suffix are supplied in glass/metal dual-in-line package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.

(Q) Devices ordered with the "Q" suffix are supplied in a glass/metal dual-in-line with a quartz window.

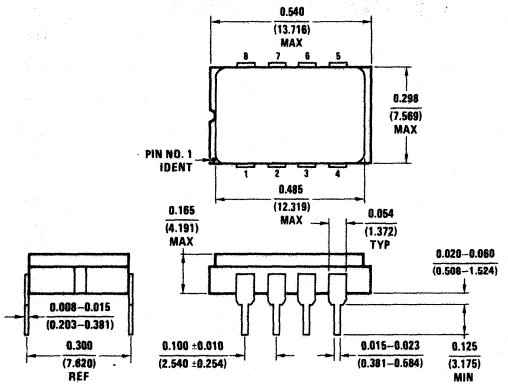
METAL CAN PACKAGES

(H) Devices ordered with the "H" suffix are supplied in either 4-pin TO-72 style, 8-pin or 10-pin TO-5 style metal can package. The cap is chrome-plated kovar and the leads are gold-plated kovar.

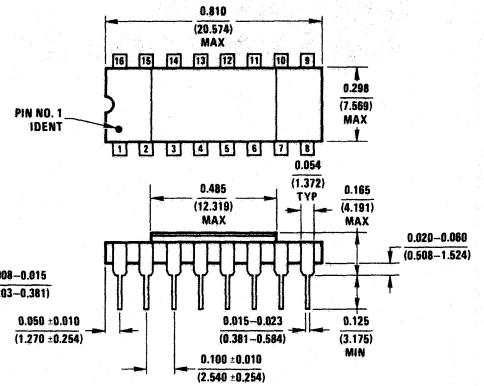
FLAT PACKAGES

(F) Devices ordered with the "F" suffix are supplied in the 14-pin, glass/metal flat package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.

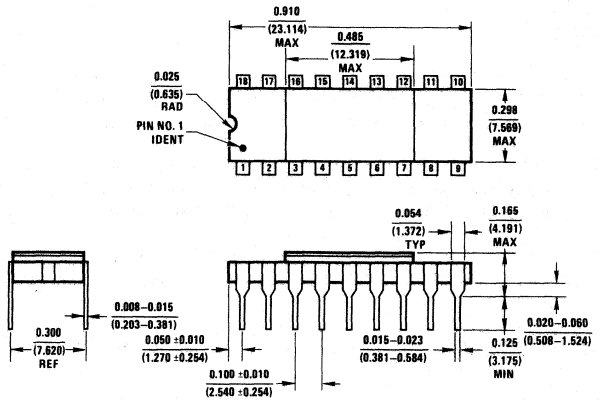
Note. All dimensions expressed as $\frac{\text{inches}}{\text{(millimeters)}}$



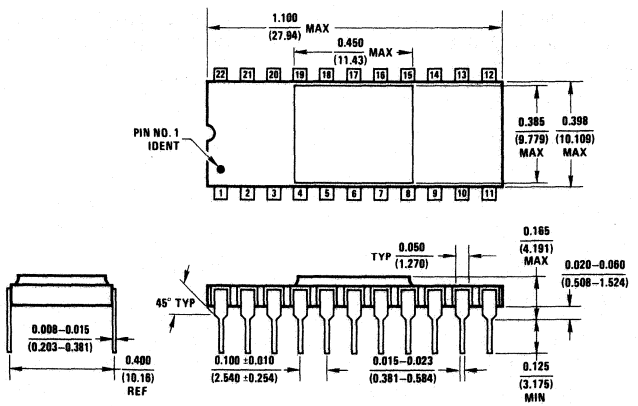
NS Package D08C
8-Lead Cavity DIP (D)



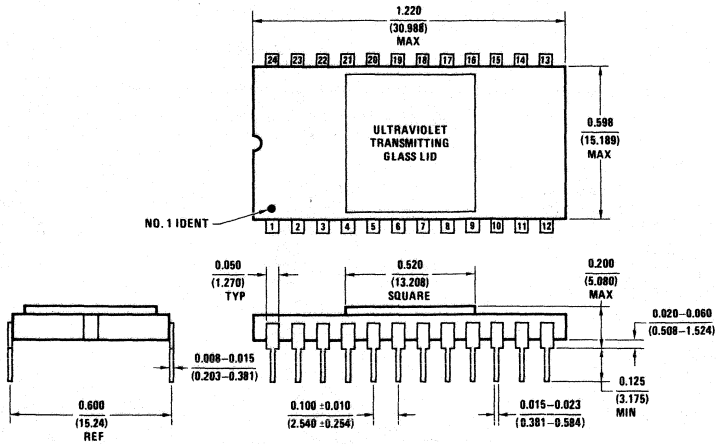
NS Package D16C
16-Lead Cavity DIP (D)



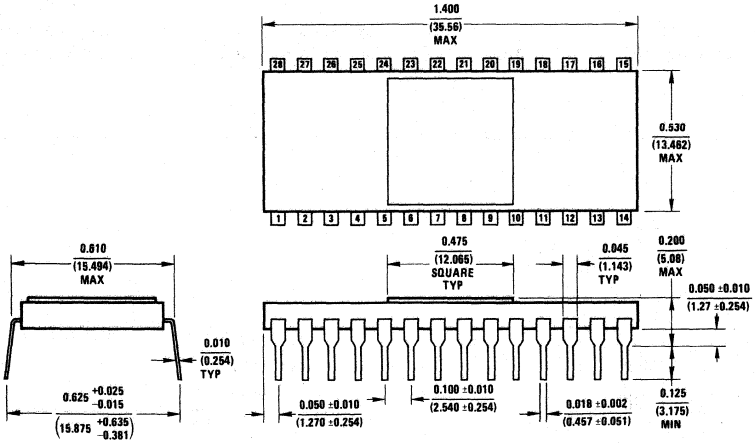
NS Package D18A
18-Lead Cavity DIP (D)



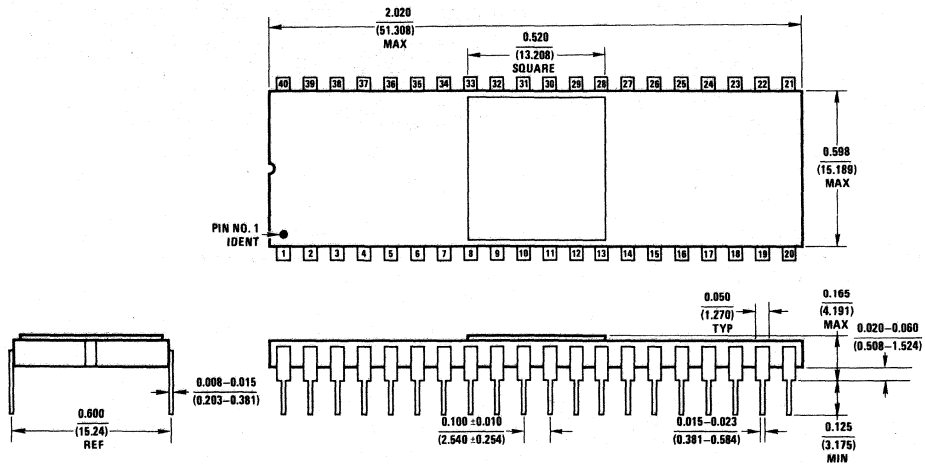
NS Package D22B
22-Lead Cavity DIP (D)



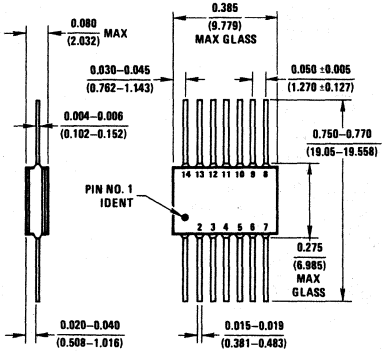
NS Package D24C
24-Lead Cavity DIP (D)



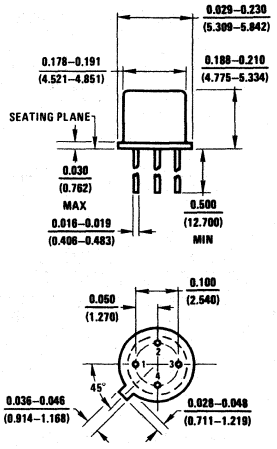
NS Package D28A
28-Lead Cavity DIP (D)



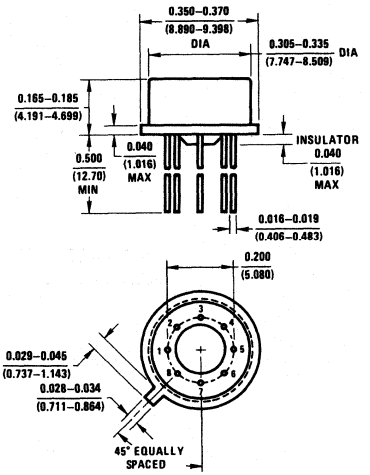
NS Package D40C
40-Lead Cavity DIP (D)



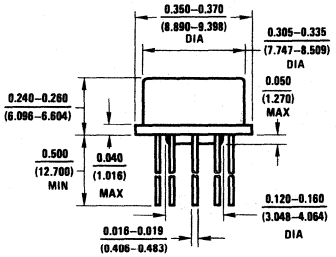
NS Package F14B
14-Lead Flat Package (F)



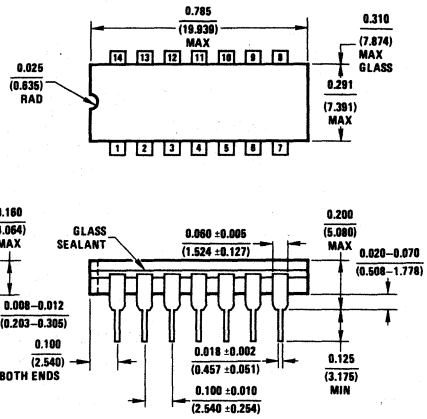
NS Package H04C
4-Lead TO-72 Metal Can Package (H)



NS Package H08C
8-Lead TO-5 Metal Can Package (H)

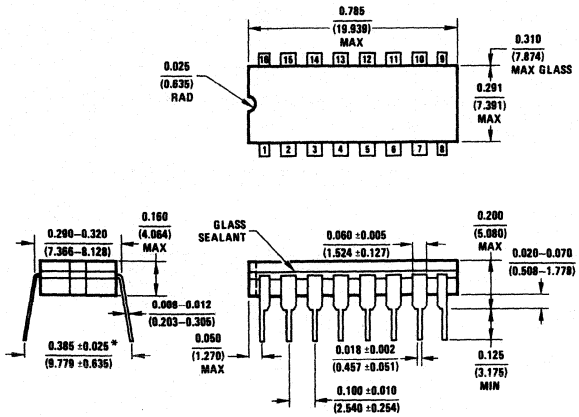


NS Package H10A
10-Lead TO-5 Metal Can Package (H)
(High Profile)

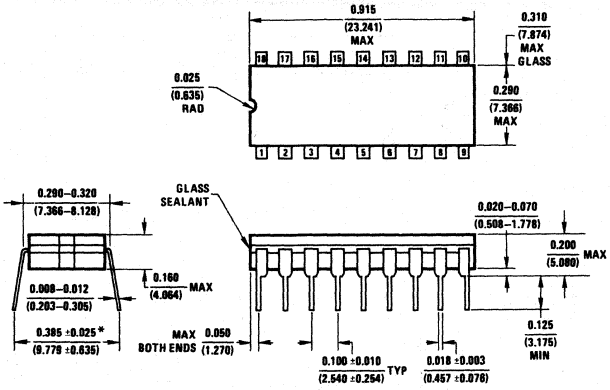


NS Package J14A
14-Lead Cavity DIP (J)

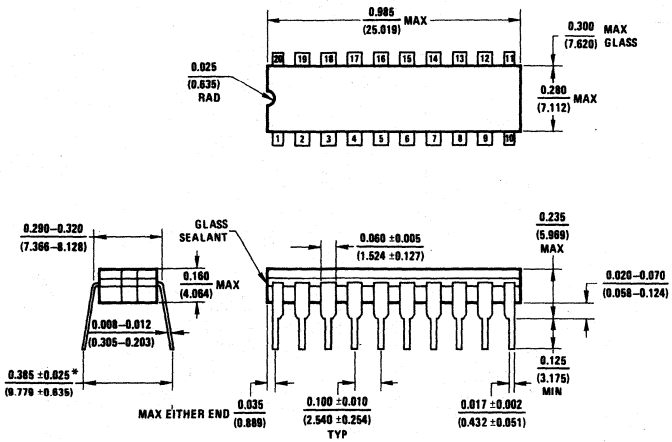
* If parts are burned-in, they will be formed to $\dfrac{0.325^{+0.025}_{-0.015}}{\left(8.255^{+0.635}_{-0.381}\right)}$



NS Package J16A
16-Lead Cavity DIP (J)

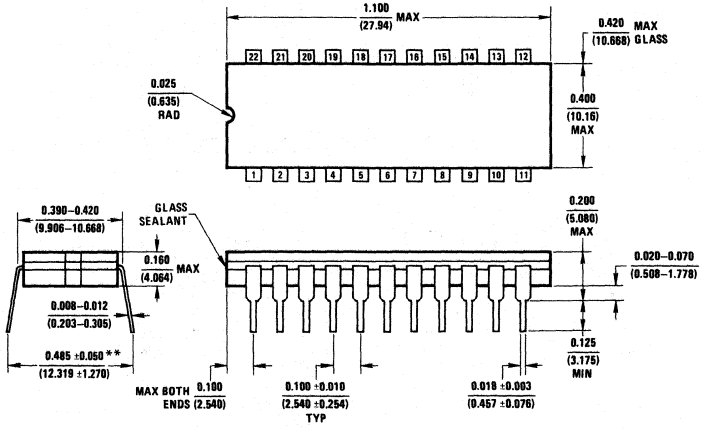


NS Package J18A
18-Lead Cavity DIP (J)

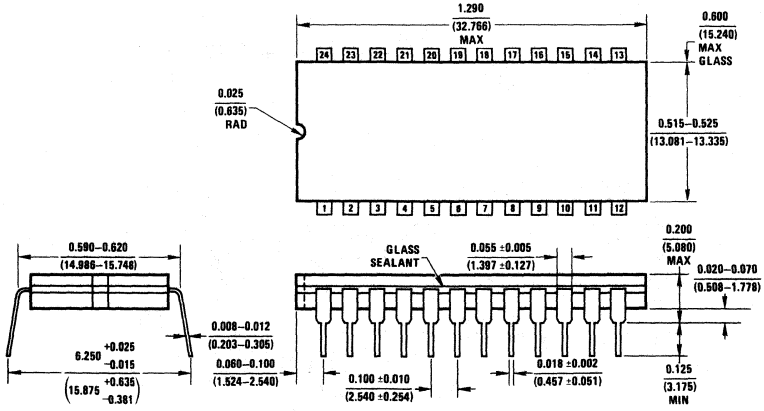


NS Package J20B
20-Lead Cavity DIP (J)

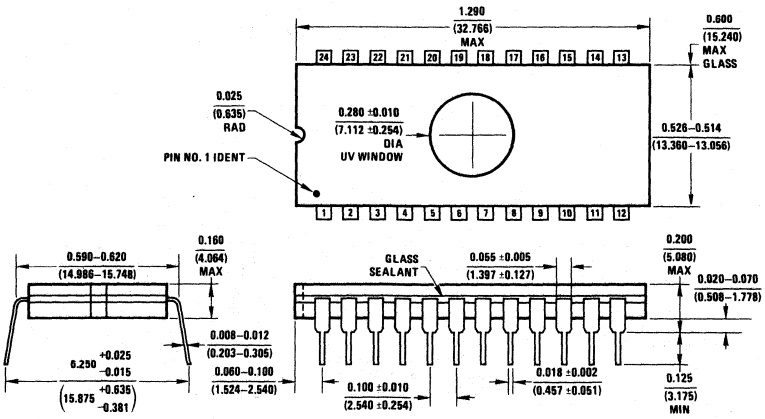
*If parts are burned-in, they will be formed to $\dfrac{0.325^{+0.025}_{-0.015}}{\left(8.255^{+0.635}_{-0.381}\right)}$



NS Package J22A
22-Lead Cavity DIP (J)

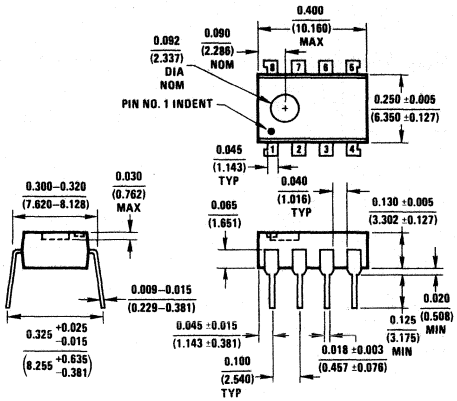


NS Package J24A
24-Lead Cavity DIP (J)

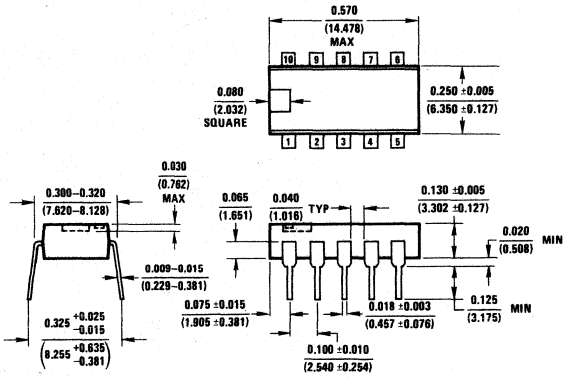


NS Package J24CQ
24-Lead UV Window Cavity DIP (JQ)

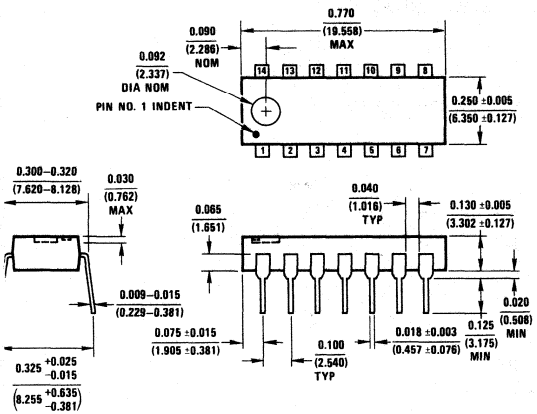
** If parts are burned-in, they will be formed to $\dfrac{0.425\ ^{+0.025}_{-0.015}}{\left(10.795\ ^{+0.635}_{-0.381}\right)}$



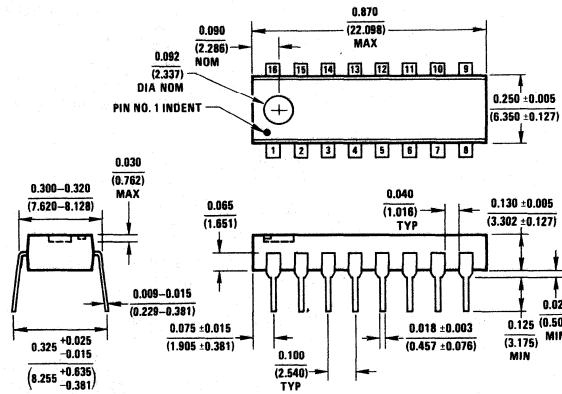
NS Package N08A
8-Lead Molded DIP (N)



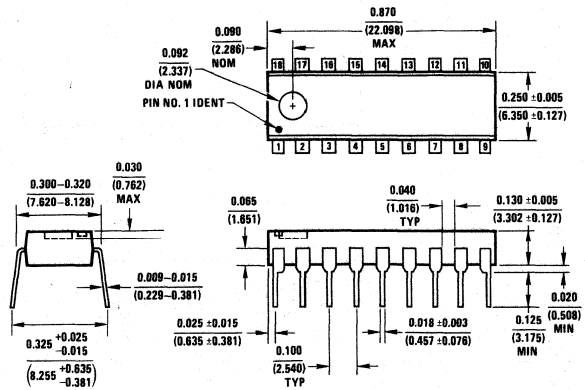
NS Package N10B
10-Lead Molded DIP (N)



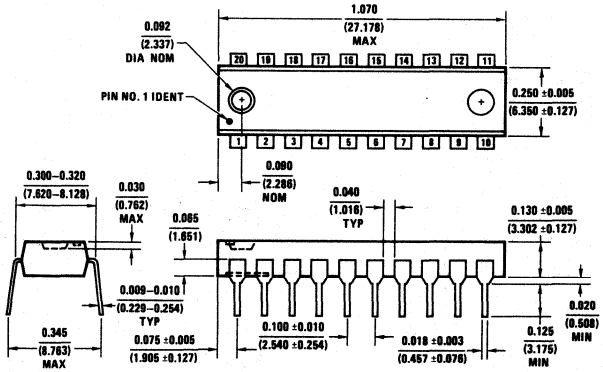
NS Package N14A
14-Lead Molded DIP (N)



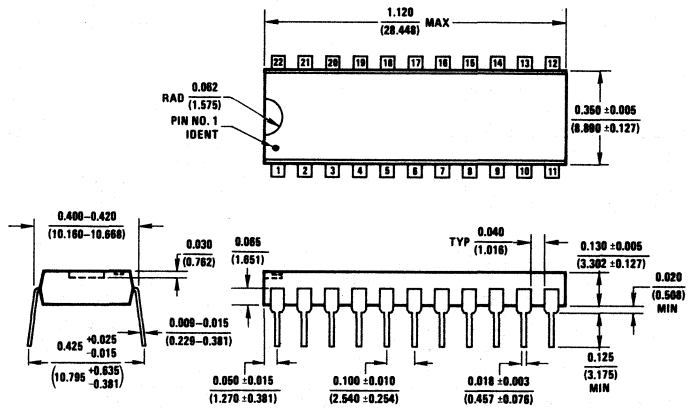
NS Package N16A
16-Lead Molded DIP (N)



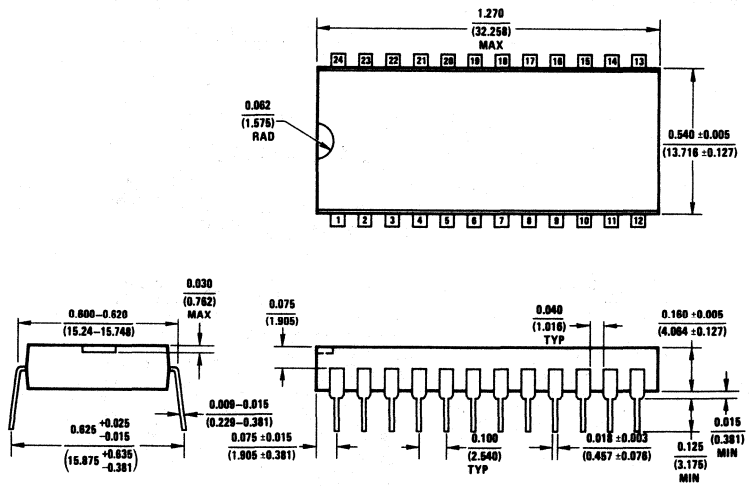
NS Package N18A
18-Lead Molded DIP (N)



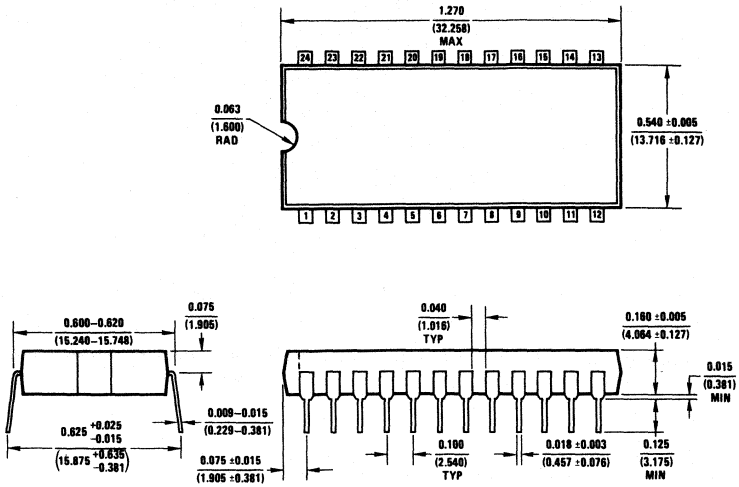
NS Package N20A
20-Lead Molded DIP (N)



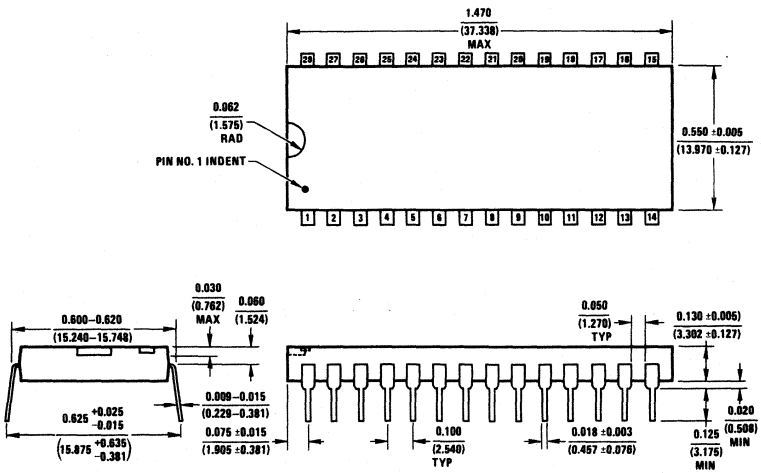
NS Package N22A
22-Lead Molded DIP (N)



NS Package N24A
24-Lead Molded DIP (N)



NS Package N24B
24-Lead Molded DIP (N)



NS Package N28A
28-Lead Molded DIP (N)